

Experimental Results on Tracking Performance of the MTDD Costas Loop With UQPSK Signal

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The carrier tracking performance of the breadboard Costas Loop of the Multimegabit Telemetry Demodulator Detector System was tested with unbalanced quadriphase shift keying (UQPSK) signals. An S-band UQPSK modulator has been built for the tests. The experimental results are very close to the theoretical rms phase error calculations.

The test and analysis show that the rms phase error for UQPSK signals is less than 5 deg at the design point if the I-to-Q channel power ratio is larger than 6 dB.

I. Introduction

To accommodate a megabit rate of telemetry data from future deep space missions, e.g., Venus Orbiting Image Radar (VOIR), a Costas Loop is being developed for the DSN as a part of the Multimegabit Telemetry Demodulator and Detector (MTDD) System (Refs. 1 and 2). So far, considerable attentions have been made to verify the carrier tracking performance of the MTDD Costas Loop with a suppressed carrier binary phase shift keying (BPSK) signal (Refs. 3 and 4). However, tracking performance of the loop has not been verified using an unbalanced quadriphase shift keying (UQPSK) until the present work.

Even though the MTDD Costas Loop was designed primarily for BPSK signalling (Refs. 1 through 5), the UQPSK signalling was considered to accommodate both a ranging signal on the quadrature channel and high-rate telemetry data on the in-phase channel (Ref. 2). Another option is the transmission of a separate telemetry data signal on the quadrature channel. The VOIR, a possible first user of the MTDD system, does not have any ranging requirement, nor is there any definite plan to use

UQPSK signalling. However, the intrinsic tracking capability of the Costas Loop for UQPSK should be verified before its implementation in DSN stations.

The breadboard Costas Loop (Refs. 1, 3, and 4) was used in conjunction with the Block III receiver in the Telecommunication Development Laboratory (TDL). An S-band UQPSK modulator has been built and used in the tests.

II. Test Configurations

Figure 1 shows the configuration used to test the tracking performance of the Costas Loop with a UQPSK signal. This test setup is exactly the same as that used for the BPSK tracking performance test (Ref. 3) except that the input signal is here supplied by the UQPSK modulator. The TDL telemetry simulator provided the high-rate, in-phase channel data stream (PN signal), and the HP8006 word generator was used to supply Q-channel data.

The rms phase jitter measurements were obtained in exactly the same manner as those described in Ref. 3. The Doppler

extractor receives the exciter output signal (reference signal) and the VCO output signal and provides basically the phase error signal.

The analog phase error signal is converted to a digital form through the control of an Altair 8800 microcomputer. The digitized phase error is processed by a Modcomp II minicomputer, and a printer interfaced with the Modcomp II provides the rms phase jitter measurements.

Figure 2 shows a more detailed Costas Loop interface with the TDL Block III receiver.

Figure 3 is the block diagram of the S-band UQPSK modulator. The reference S-band signal is fed to a 90-deg hybrid through an isolator, which in turn generates I and Q channel carriers. On the other hand, the interface unit provides balanced data (logic '1' and '0' have the same magnitude of voltage level) from either transistor-transistor logic or a balanced-type data generator. The attenuators in I and Q channels can select the I and Q channel power ratio. The selected levels of the I and Q channel data are mixed with the respective carriers. Those two modulated carriers are summed to produce a UQPSK signal. Of course, a balanced QPSK signal can also be generated with the modulator. However, it is not used for a balanced QPSK signalling since the present Costas Loop cannot track a balanced QPSK signal. The modulator was aligned using a network analyzer. All four possible vectors observed in the network analyzer were calibrated within 1.5 deg in-phase and 0.1 dB in amplitude from an ideal modulator condition. The measured carrier suppression was larger than 35 dB.

III. Tracking Performance of UQPSK Signal

The tests performed are intended to verify the tracking performance of the breadboard Costas Loop for various conditions.

The rms phase jitter is expected to be a function of total signal power-to-noise density, the I-to-Q channel data rate ratio, and the I-to-Q channel power ratio (Refs. 6 and 7). Since the breadboard Costas Loop was designed to have appropriate arm filters and loop filters for 100-, 250-, 500-kbps and 1-Mbps data rates, the rms phase jitters for the above I channel data rates are supposed to be the same if other parameters are the same.

Tests were performed for 1-Mbps and 100-kbps I channel data rates. Figures 4 and 5 summarize the test results for respective I channel data rates. Rms phase jitters were measured for various PT/N_0 (total power within the I channel data

rate bandwidth-to-noise density ratio), parameter R (the I channel-to-Q channel data rate ratio), and parameter P_I/P_Q (the I-to-Q channel power ratio), where $P = P_I + P_Q$ and $T = I$ channel symbol width. The ranges of parameters are:

$$(1) PT/N_0 = -4, -2, 0, 2, +4 \text{ (dB)}$$

$$(2) R = 20, 5, 1$$

$$(3) P_I/P_Q = 6, 10 \text{ (dB)}$$

Throughout the tests, a PN signal was used for I channel data and a squarewave was used for Q channel. It is expected to have similar results if a PN signal is used for Q channel instead of a squarewave.

The tests results agree very well with the theoretical calculations shown in Figure 6. Also shown in Figure 6 is the theoretical phase jitter performance of the loop with BPSK signal. The phase jitter performance for the UQPSK signal does not degrade too much from that for the BPSK signal. For the 6-dB P_I/P_Q ratio, the degradation is less than 2 deg.

IV. Theoretical Predictions

The basic derivations for rms phase jitter of the Costas Loop with the UQPSK signal are documented in Refs. 6 and 7. However, for the sake of self-containment, the method of calculation is summarized here.

Basically, the rms phase jitter is given by (Ref. 7):

$$\sigma_\phi^2 = \frac{1}{\frac{PT}{N_0} \frac{1}{B_L T} S_L} \quad (1)$$

where

σ_ϕ = rms phase jitter

P = total carrier power

T = I channel data bit width

N_0 = Noise spectral density

B_L = single-sided loop bandwidth

S_L = squaring loss

The calculation of squaring loss is given in Ref. 7. The loop bandwidth is given by:

$$B_L = \frac{\omega_n}{2} \left(\zeta + \frac{1}{4\zeta} \right) \quad (2)$$

where B_L = single-sided loop bandwidth for an imperfect second-order loop with a transfer function of

$$F(s) = \frac{1 + \tau_2 s}{1 + \tau_1 s}$$

$$\omega_n = \sqrt{\frac{K}{\tau_1}} = \text{natural angular frequency}$$

$$\zeta = \frac{1 + K \tau_2}{2\omega_n \tau_2} = \text{loop damping factor}$$

K = total loop gain

If K_0 is the loop gain at the design point, the loop gain at an arbitrary SNR is given by:

$$K = K_0 \cdot \frac{\alpha}{\alpha_0} \cdot \frac{g\sqrt{P}}{(g\sqrt{P})_0} \quad (3)$$

where

α_0 is the signal suppression factor at design point

α is the signal suppression factor at a desired SNR

$(g\sqrt{P})_0$ is the total IF gain control voltage at design point

$(g\sqrt{P})$ is the total IF gain control voltage at a desired SNR

Using Eqs. (1), (2), and (3), rms phase jitters for various PT/N_0 , R , and P_I/P_Q were calculated and plotted in Figure 6. The squaring loss was calculated from a low input SNR approximation shown in Ref. 7.

V. Conclusions

An S-band UQPSK modulator was built. Using the modulator, the carrier tracking performance of the MTDD breadboard Costas Loop was tested in the TDL for UQPSK signal. The experimental results were compared with the theoretical predictions.

Experimental and analytical results agree with each other very closely. Finally, it can be concluded that the presence of Q channel data — either a telemetry or a ranging signal — does not degrade the tracking performance to much compared to the BPSK case.

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References

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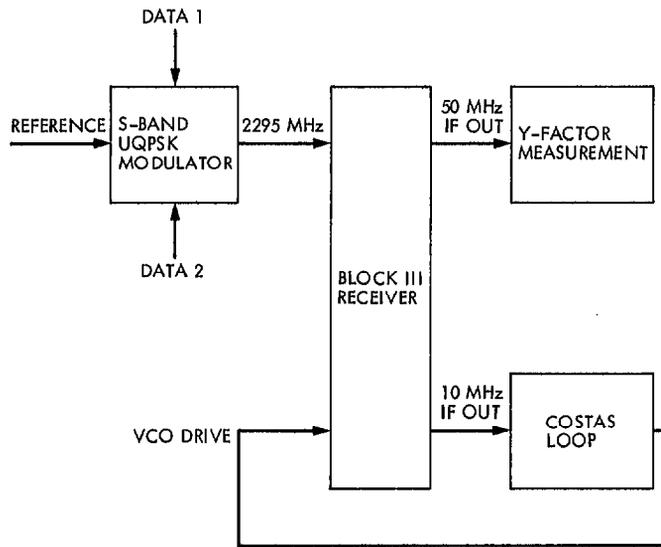


Fig. 1. Test setup in TDL

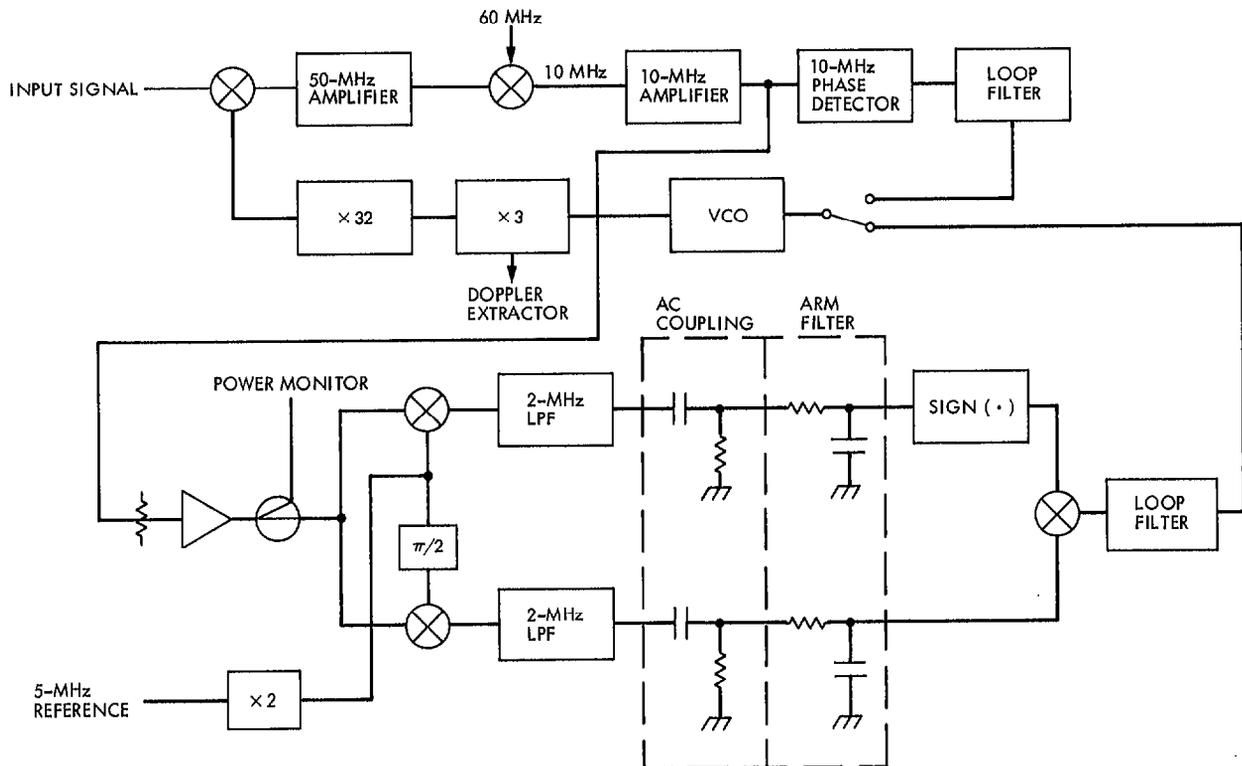


Fig. 2. Configuration of Costas Loop interface with TDL Block III receiver

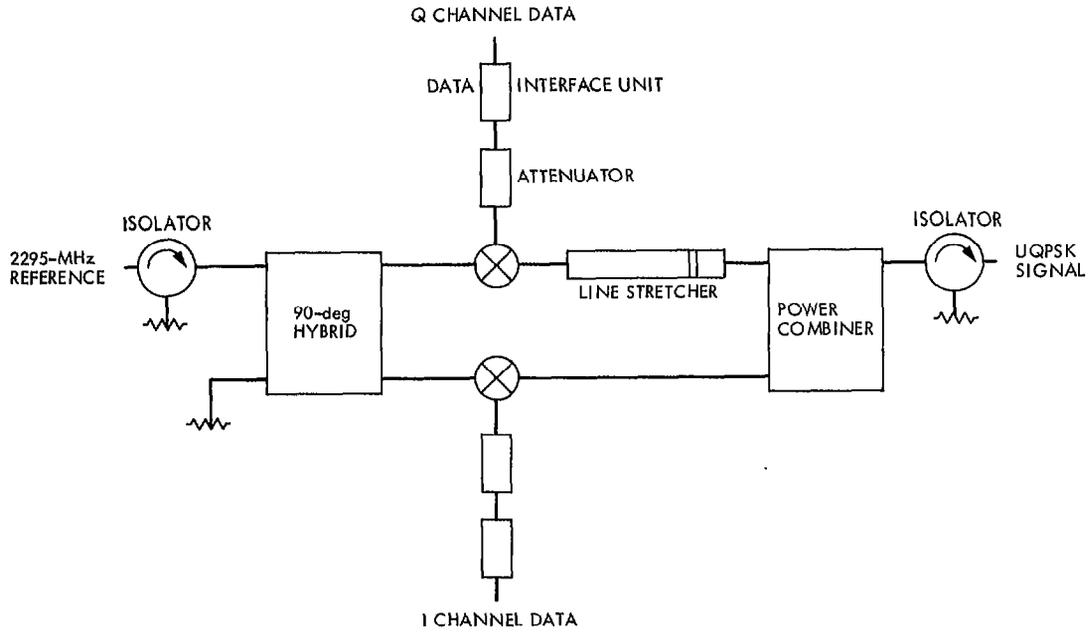


Fig. 3. UQPSK modulator diagram

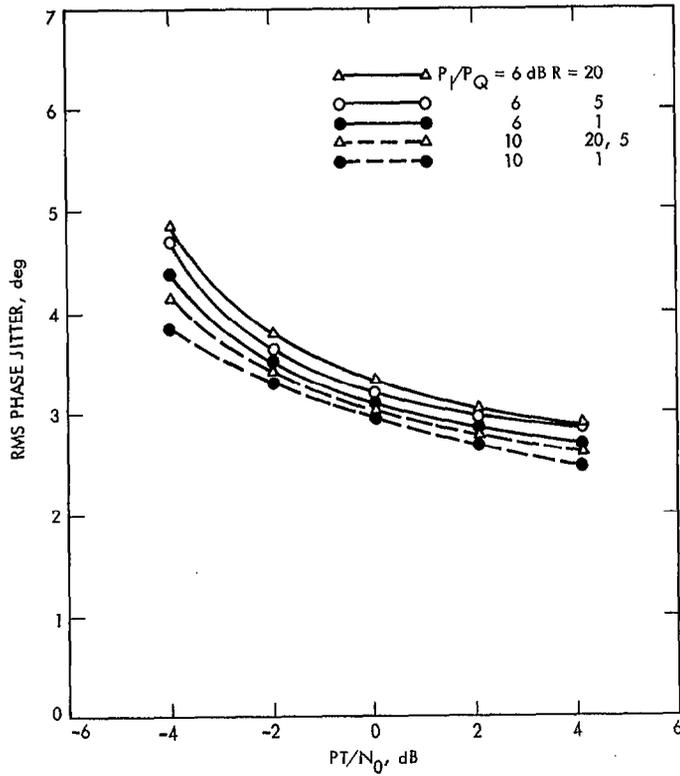


Fig. 4. Measured rms phase jitter for I channel data rate of 1 Mbps

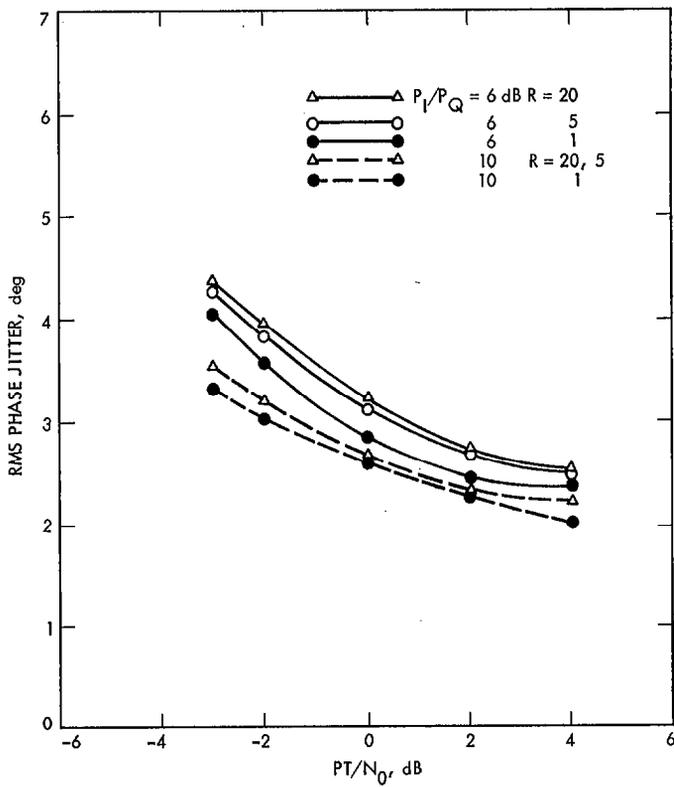


Fig. 5. Measured rms phase jitter for 1 channel data rate of 100 kbps

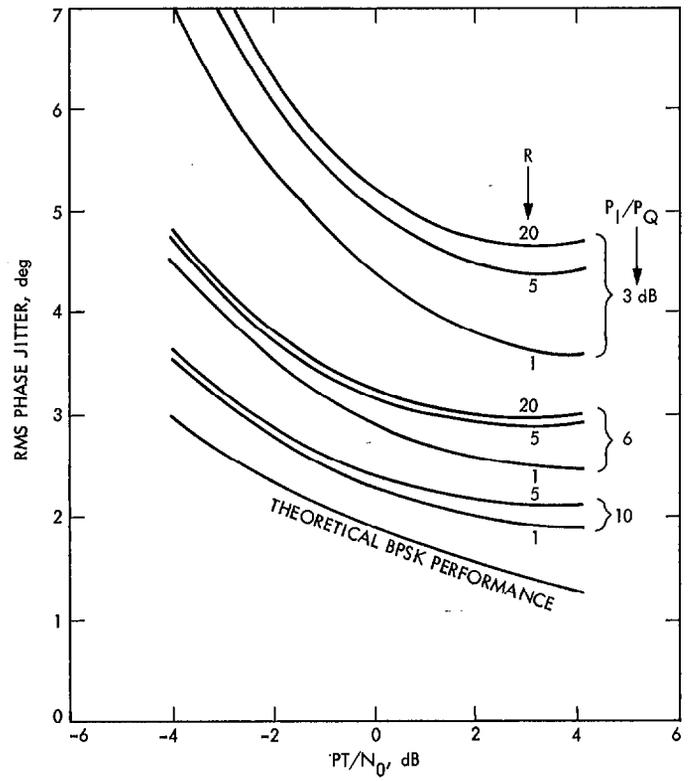


Fig. 6. Theoretical rms phase jitter calculated with low input SNR approximation for MTDD breadboard Costas Loop using UQPSK signals