

JPL 2^{20} Channel 300 MHz Bandwidth Digital Spectrum Analyzer

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A million (2^{20}) channel, 300 MHz bandwidth, digital spectrum analyzer is being constructed at the Jet Propulsion Laboratory. The design, fabrication, and maintenance philosophy of the modular, pipelined, Fast Fourier Transform (FFT) hardware are described. The spectrum analyzer will be used to examine the region from 1.4 GHz to 26 GHz for Radio Frequency Interference (RFI) which may be harmful to present and future tracking missions of the Deep Space Network. The design will have application to the Search for Extraterrestrial Intelligence (SETI) signals and radio science phenomena.

I. Introduction

A million channel digital spectrum analyzer with 300 MHz of bandwidth is under construction at the Jet Propulsion Laboratory. The 300 MHz bandwidth was chosen to take advantage of a 300 MHz bandwidth K-band traveling wave maser which is used with parametric up-converters to cover the frequency range from 1.4 GHz to 26 GHz. The purpose of the spectrum analyzer is to detect and identify radio frequency interference which may be harmful to present and future spacecraft tracking missions of the Deep Space Network.

The block diagram of the spectrum analyzer is shown in Fig. 1. The RF system consists of an antenna, parametric

up-converter, maser, and receiver with 300 MHz bandwidth IF output. An analog filter bank is used to separate the 300 MHz into 32 complex channels of 10 MHz bandwidth each. A pipelined, decimation in frequency FFT is used to process two of these 10 MHz channels simultaneously. The power spectrum is obtained by squaring the real and imaginary parts of the complex spectrum. The power spectrum is accumulated for a number of spectra to reduce the data bandwidth to a manageable value for input to a general purpose computer.

An extensive computer simulation was performed to determine the optimum hardware implementation to support the 60 dB dynamic range required. As a result of this

simulation, the hardware is implemented using 8 bit A/D converters, 12 bit memories in the first four stages, 16 bit memories in the remaining 11 stages, and 16 bit, fixed point, hard scaled calculations in all stages.

II. Analog Filter Bank

The bank of analog filters, shown in Fig. 2, is used to break the 300 MHz total bandwidth into 32 channels of 10 MHz bandwidth each. The input IF signal is distributed to the 32 complex mixers together with the output from a comb generator. This comb generator supplies the 32 local oscillator frequencies separated by 10 MHz. The complex mixer is made of two mixers and a 90° phase shifter between the local oscillator input and one of the mixers. The in-phase (real) and quadrature (imaginary) outputs of the mixer each pass through a 5 MHz low pass filter to an 8 bit A/D converter. These 10 MHz A/D converters are now readily available at relatively low cost because of their use in digital conversion of TV signals.

The low pass filters are 3 dB down at the band edge, resulting in aliasing between adjacent 10 MHz channels. This aliasing is compensated for by a postprocessing algorithm in the general purpose computer.

III. FFT Block Diagram

The FFT, shown in Fig. 3, consists of 15 pipelined stages (Ref. 1), each composed of a memory unit and a "butterfly" arithmetic unit. Only three types of modules are used in the entire FFT. The memory modules used for the first four stages have a maximum capacity of 16K complex words of 12 bits. The other 11 memory modules have a maximum capacity of 1024 complex words of 16 bits. The same 16 bit arithmetic module type is used in all stages.

The memory modules are programmed with a dual-in-line header to provide the appropriate delay and trig coefficients for each stage in the pipeline.

The input to the FFT uses the "Biplex" method (Ref. 2) to simultaneously process two independent 10 MHz channels in the pipelined architecture FFT. This method results in the full-time utilization of all memory and arithmetic elements. The complete spectrum analyzer contains 16 of these dual 15-stage pipelined FFT's.

IV. Memory Units

A block diagram which is common to both types of memory units is shown in Fig. 4. A memory unit is composed of two delay memories and multiplexers which allow straight through or crossed input-output connection as required in the pipelined algorithm. The memory unit also contains the trig coefficient generator. A delay equalization stage is incorporated to compensate for different timing delays in the two paths through the arithmetic unit.

The differences between the two types of memory units concern the size and type of delay memory and type of trig generator.

The first four memory units, called 16K max on the FFT block diagram (Fig. 3) use CCD memories with a capacity of 16K complex words of 12 bits. They are implemented by multiplexing four Fairchild CCD461A integrated circuits to obtain 10 MHz bandwidth. The remaining 11 units, called 1K max, use random access memories (Intel 2125AL) with a capacity of 1024 words of 16 bits.

The trig generator in the first four stages uses differences between successive coefficients, stored in ROM, to calculate the coefficients. This technique is usable because the decimation in frequency algorithm requires trig coefficients in the order of increasing angle. Storing differences rather than coefficients results in smaller ROM size and reduced total integrated circuit count. The trig generator in the remaining 11 stages actually stores the coefficients in ROM.

The trig coefficients used are always negative numbers so that -1 is included in the 2's complement number field. Appropriate sign changes are incorporated in the arithmetic unit to allow this convention.

V. Arithmetic Unit

The FFT radix 2 butterfly arithmetic unit is shown in Fig. 5. The complex adder/subtractor butterfly is placed in front of the complex multiplier in the decimation in frequency algorithm. The adder/subtractor operates on 16 bits of input data to deliver 17 bits of output. The output is scaled and rounded to retain the 16 most significant bits. The adder is implemented with the 74S283 and the subtractor with the 74S381.

The complex multiplier is composed of four real multipliers followed by an adder (74S283) and subtractor (74S381) to combine the partial products. The real multipliers are imple-

mented with the TRW MPY-16A. Two of these multipliers are connected in parallel and multiplexed to obtain a 10 MHz multiply rate. This is simple because of the input and output registers contained within the MPY-16A. The complete complex multiplier contains eight of the MPY-16A's. A fractional multiply is performed, and the 16 most significant bits are retained. The internal circuitry of the MPY-16A is used to round the result.

VI. Fabrication

A dual 32K point FFT prototype is now under construction at JPL. The prototype modules are constructed on wire wrap boards approximately 15 by 35 cm.

VII. Maintenance Philosophy

Testers are being designed to completely exercise the logic of the memory and arithmetic units of the FFT. These testers are used in manufacturing and depot level maintenance.

In the field, digital test signals, instead of the A/D converter outputs, can be injected into the FFT. The output of any module can then be compared to the expected output which is obtained from the general purpose computer. The failed unit is isolated by this technique and repaired by replacement. Failed modules are returned to a depot for repair. Since there are only three module types in the FFT, only a small inventory of spares is required. All diagnostic tests are conducted at full clock rate.

References

1. Rabiner, L. R., and Gold, B., *Theory and Application of Digital Signal Processing*, Prentice Hall, Inc., New Jersey, 1975, pp. 602-609.
2. Emerson, R. F., "Biplex Pipelined FFT", in *The Deep Space Network Progress Report 42-34*, Jet Propulsion Laboratory, Pasadena, California, 1976, pp. 54-59.

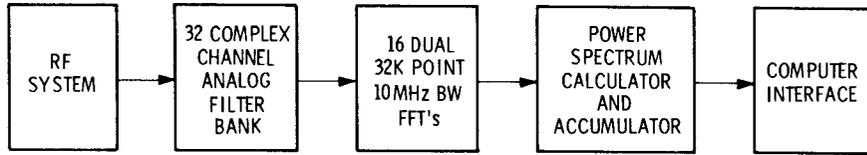


Fig. 1. Spectrum analyzer block diagram

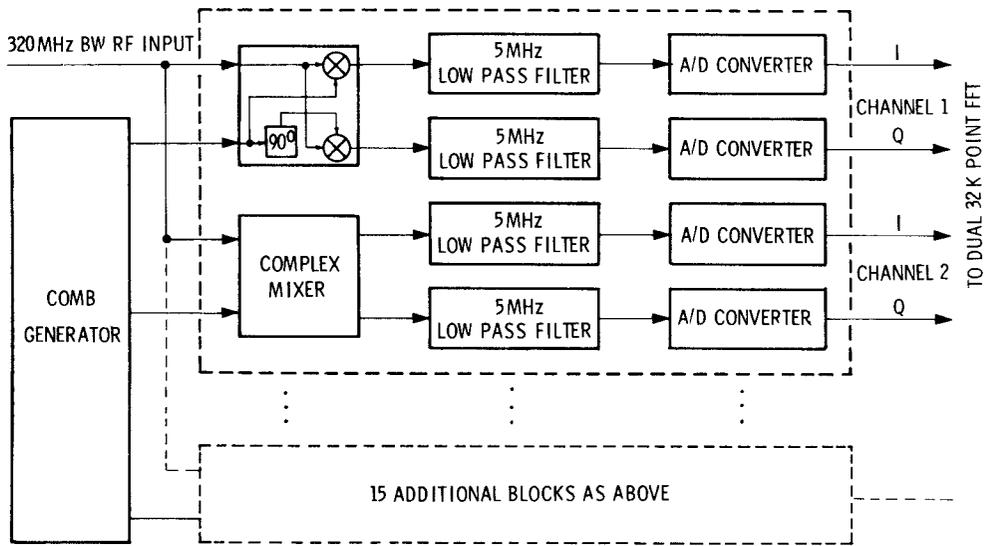


Fig. 2. Analog filter bank

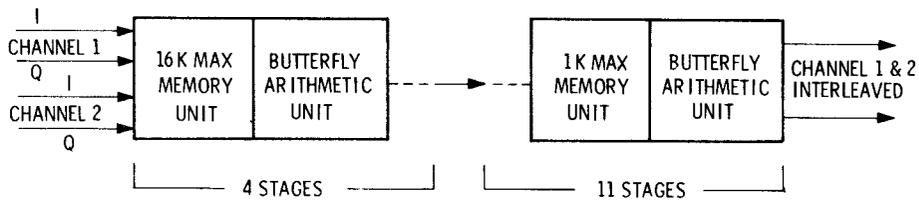


Fig. 3. FFT block diagram

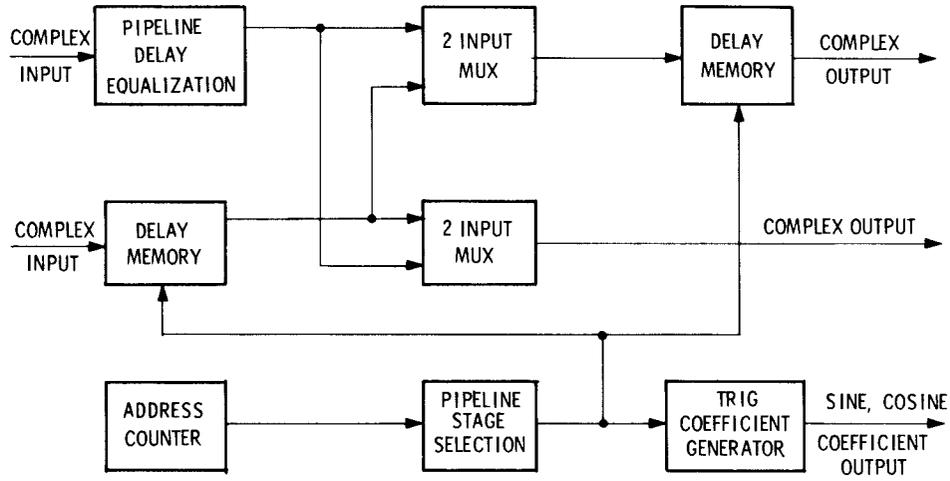


Fig. 4. Butterfly memory unit

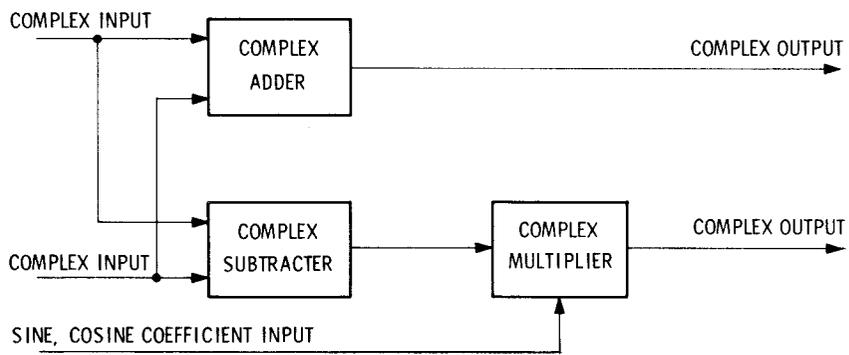


Fig. 5. Butterfly arithmetic unit