An IF-to-Digital Converter for the Advanced Receiver II (ARX II)

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An IF-to-Digital Converter (IDC) breadboard for the Advanced Receiver II has been designed, built, and tested in the laboratory, along with a Frequency Reference Generator and a Test Signal Generator. Field testing was performed by demonstrating Doppler extraction from Voyager 2 and Pioneer 10 signals at DSS 14. This article explains the functional requirements of the IDC, describes the design, and discusses the design trade-offs made. The results of the laboratory performance tests are presented, along with the test setups used.

I. Introduction

A new IF-to-Digital Converter (IDC) breadboard has been developed for the Advanced Receiver II (ARX II). The ARX II is a hybrid analog/digital receiver that is intended for technology demonstration in the Deep Space Network (DSN) [1]. As the successor to the Advanced Receiver I (ARX I) [2], the ARX II has inherited many design characteristics of its predecessor and some new capabilities have been added with the goal of providing a baseline design for the future Block V Receiver. The IDC was designed to provide a digitized IF signal to the ARX II Signal Processor and to meet the long-term requirements of the ARX II as a tracking and high-rate telemetry receiver.

The IDC breadboard was built and evaluated in the laboratory. It has also been tested, as part of the ARX II system, in a Doppler extraction demonstration at the Signal Processing Center (SPC 10) at Goldstone using the DSS 14 antenna and a Very Long Baseline Interferometer (VLBI)/Radio Science Downconverter [3]. This article discusses the IF-to-Digital Converter design requirements and the analyses done for subsystem architecture and component selection. Descriptions of the Frequency Reference Generator and the Test Signal Generator are given, along with test setups and results.

II. Subsystem Design Requirements

A. General Functional Requirements

The thrust of the advanced receiver development has been to implement receiver functions with digital circuits. Processing speed limitations, however, still dictate the use of analog components for the radio frequency (rf) and intermediate frequency (IF) receiver sections. The primary

function of the IDC is to downconvert a received spacecraft signal to an IF frequency that can be digitized with existing technology. Specifically, the IDC is required to downconvert the first IF outputs of the VLBI/Radio Science Downconverters, over a range of 200 to 400 MHz, to an IF of 10 MHz. The converter also provides channel selection in the DSN S- and X-bands (2.2–2.3 GHz and 8.4–8.5 GHz, respectively), the channel bandwidth for data rates up to 6.6 megasymbols per sec (MSPS), and the automatic gain control (AGC) for optimum resolution from the sampler. In Fig. 1, a block diagram of the IDC breadboard for the ARX II shows its configuration at the Goldstone Deep Space Communications Complex (DSCC).

A functional block diagram of the IDC is shown in Fig. 2. The converter supports two different modes of operation of the ARX II: analog loop mode and digital loop mode. For both modes of operation, the 10-MHz IF signal is digitized to 8 bits at a fixed rate of 40 MHz and is connected to the digital signal processor (DSP). For the analog mode, the carrier tracking loop is closed with a tunable 80-MHz local oscillator (LO) derived from a 4-MHz numerically controlled oscillator (NCO) in the signal processor. In the digital mode, a fixed-80-MHz LO is used and the loop is closed inside the signal processor. The converter also accommodates test inputs at the first and second IFs and provides test outputs at the third IF. The 10-MHz noise-free test point can be used for verification of phase lock when the receiver is in the analog loop mode or loop phase error jitter measurement with an external phase detector.

B. Assembly Specifications

A set of specifications for the IDC was developed using both the ARX II requirements and the preliminary Block V Receiver requirements. The specifications for the three assemblies, IF-to-Digital Converter, Frequency Reference Generator, and Test Signal Generator, are summarized in Table 1. Some cost-versus-performance and cost-versus-size trade-offs were made in developing these specifications. These are discussed in Section III. The eventual goal of the ARX II is to demonstrate all the functions of the future Block V Receiver (i.e., telemetry, Doppler extraction, ranging, and radio science). Consequently, an attempt was made to meet these requirements with the resources available.

III. IF-to-Digital Converter Design

A. Cost/Size/Performance Trade-offs

In order to limit development time and cost of the IF-to-Digital Converter, Frequency Reference Generator, and Test Signal Generator, the breadboards were packaged using mainly connectorized components interconnected with flexible coaxial cable. The three assemblies were then mounted in standard rack drawers with internal power supplies, as shown in Fig. 3. This approach minimized the custom fabrication of chassis and printed circuit boards. The resulting assemblies were relatively large but nevertheless met the space constraints of the ARX II system rack.

Cost and scheduling were also issues in IF frequency selection. A 70-MHz IF was chosen because of the availability of off-the-shelf filters. A surface acoustic wave (SAW) device was chosen for the IF-image-reject and antialias filter even though the "closest" stock item had a slightly larger than optimum bandwidth. These decisions were made to avoid the long development time and nonrecurring engineering charge of $15K for a custom design. A cost savings was also realized by downconverting directly from 300 to 70 MHz. This scheme minimizes the component count but is susceptible to mixer intermodulation products in the event of radio frequency interference (RFI) at the antenna inputs. This effect is discussed in Section III.B. The 70-MHz IF frequency also simplifies the design of the Frequency Reference Generator since the required 80-MHz LO is now an integer multiple of the 40-MHz sampling clock.

For the channel select synthesizer, a basic trade-off was made between cost and phase-noise performance. Two units, both costing $6K, were evaluated: a Marconi 2018 and a Hewlett-Packard 8656. The Hewlett-Packard model was chosen on the basis of its superior phase-noise performance. This synthesizer did not meet the radio science phase-noise requirements but was a fraction of the cost of a low-noise unit that would meet those requirements.

A space savings trade-off was also made in the selection of power supplies. Switching supplies were chosen for their small size. The resulting spurious sidebands are higher, however, than the linear supplies; this is an area where the breadboard does not meet the projected Block V spurious-free dynamic range requirement.

B. Frequency Plan

1. Image and Intermodulation Product Rejection. The ARX II is required to track carriers over a carrier-to-noise ratio (CNR) range of 0 to 95 dB-Hz, as outlined in the specifications summary. This is the approximate range between a maser low-noise amplifier (LNA) compression point (−90 dBm) and a 0 dB-Hz carrier (−185 dBm). A spurious-free dynamic range design

goal of 100 dB allows for an additional margin of 5 dB below the weakest expected signal. This magnitude of dynamic range requires careful control of all spurious frequency components, both internally generated and external RFI at the antenna inputs. In reality, a lower spurious-free dynamic range, in the presence of external RFI, was accepted for this breadboard as a cost trade-off. By choosing a simple dual downconversion scheme from 300 MHz to 10 MHz, the cost for components and the synthesizer was minimized.

The spurious frequency component levels from a downconverting mixer can be predicted from the input and output filter characteristics and the mixer operating point. An example for an S-band IF (200–300 MHz) with a desired carrier at 250 MHz and with the LO tuned to 320 MHz will illustrate the analysis approach. With the frequency plan chosen, the second IF frequency (70 MHz) is relatively small compared to the input bandwidth (130 MHz), so that the image frequency is close to the passband, and some of the higher order intermodulation (IM) products actually fall in band. The various IM products for a downconverter can be calculated and plotted, as in Fig. 4(a), along with filter bandwidths, to quickly identify any potential "problem" frequencies [4]. The IM products are determined from

$$f_{out} = N \cdot (f_c + \Delta f) + M \cdot f_{LO} \qquad (1)$$

where

f_{out} = mixer output frequency

f_{RFI} = undesired input frequency

f_c = desired input frequency

Δf = difference between desired and undesired inputs

$= f_{RFI} - f_c$

M, N = positive or negative integers

$M + N$ = IM product order

Parallelograms for both the S- and X-band (2.2–2.3 GHz and 8.4–8.5 GHz, respectively) preselector IF filters are drawn on the plot in Fig. 4(a). Any lines that pass through the filter passbands represent IM products that are not rejected. For example, consider the point f_1. At this point, $f_c = 250$ MHz and $f_{RFI} - f_c = 13.3$ MHz, so $f_{RFI} = 236.7$ MHz. Line Q is for $N = +3$ and $M = -2$, so the mixer product of $3 \times f_{RFI}$ with $2 \times f_{LO}$ gives an output at 70 MHz, thus interfering with the desired IF.

The resulting amplitude levels of the IM products can be predicted from the mixer input operating point and a table (often available from the manufacturer) of the single-tone intermodulation products. Figure 4(b) shows a summary of the problem frequencies and the levels at the downconverter output. From these data, it is apparent that, in the worst case (f_3), the spurious-free dynamic range is only 54 dB. However, this phenomenon only occurs when there is external RFI at the antenna input, and the risk was considered acceptable for this breadboard version receiver in view of the cost savings.

The second downconversion stage uses a fixed-80-MHz LO to translate the IF from 70 MHz down to 10 MHz. This mixer has its own set of IM products when operated near the upper end of its "linear" range. The potential problem frequencies are plotted in Fig. 5(a) and their output levels are summarized in Fig. 5(b). From the data tabulated in Fig. 5(b), it is seen that the worst case spurious-free dynamic range of this stage is 60 dB.

2. Broadband Noise Rejection. Since the ARX II is intended to demonstrate tracking of very weak spacecraft signals, the issue of system noise temperature T_{op} degradation is an important one. The design goal for the IDC was to limit additive noise power to 1 percent (0.04 dB) or less. This requires careful selection of component noise figures, image-reject filters, and (since this is a sampled IF system) anti-aliasing filters. However, in this area, a basic compromise must be made between data bandwidth and image and alias band rejection. The ARX II is required to demonstrate 6.6 MSPS performance, but the processing rate was limited to 40 MHz, by current technology, at the start of the design. Since the Nyquist band (half the sampling rate) was limited to 20 MHz, the third IF frequency was set at 10 MHz, in the center of the band. A 10-MHz IF frequency was also originally required for compatibility with the ranging subsystem, but this requirement was later dropped in lieu of a digital baseband ranging interface.

The image and alias noise rejection is primarily done by the 70-MHz SAW filter, as shown in Fig. 6(a). This technology provides the best combination of steep filter skirts and linear phase when high inherent insertion loss is acceptable. The approach taken was to select a bandwidth as large as possible (to limit symbol signal-to-noise degradation due to band limiting) and still meet the total T_{op} degradation requirement. An off-the-shelf filter was used due to cost and time constraints, and the actual bandwidths are 18 and 20 MHz at the 1 and 3 dB points, respectively. The measured response is plotted in Fig. 6(b). In order to determine the additive noise due to image and alias "folding," the SAW filter was modeled

as a Tchebysheff filter (with a known transfer function) with an equivalent shape factor. The relative noise power in the reject bands, 0–60 MHz and 80–∞ MHz, was then evaluated numerically by [5]

$$\frac{(P_N)_{REJECT}}{(P_N)_{TOTAL}} = \frac{\int_0^{60} |H(jw)|^2 df + \int_{80}^{\infty} |H(jw)|^2 df}{\int_0^{\infty} |H(jw)|^2 df} \quad (2)$$

where

$H(jw)$ = modeled response of SAW filter

The resulting additive noise due to imperfect filtering is 3.5 percent or 0.15 dB. This is greater than the original design goal but was considered an acceptable trade-off for cost and schedule gains.

3. Digital Loop Versus Analog Loop. Two architecture options are built into the ARX II design: an analog loop mode and a digital loop mode. In the analog loop mode, a 4 ±1-MHz NCO is converted to analog and upconverted to 80 MHz to close the carrier tracking loop at the 10-MHz IF. This is analogous to the architecture used in the ARX I. This mode was included to allow interfacing with existing DSN subsystems, which use a 10-MHz-fixed IF. In the digital loop mode, a fixed-80-MHz LO is used and the 10-MHz IF is open loop. This dual capability allows a direct performance comparison between the two modes with all other parameters remaining the same. The analog loop has the advantage of eliminating Doppler excursion on the 10-MHz IF, thereby reducing the effect of band-limiting at high data rates and of carrier group delay variations across the SAW filter passband. The digital loop, however, is simpler (requires only one NCO in the signal processor) and reduces the interconnections between the IDC and the signal processor assembly.

C. Amplitude Control

1. Gain Distribution. Functionally, the IDC is required to accept carrier inputs over the dynamic range of the DSN low-noise amplifiers with system temperatures of 15 to 500 K. An additional gain of 20 dB was added to allow for gain uncertainty in the signal path from the LNA output to the IF distribution (IFD) output. This was done primarily to compensate for an uncertainty in step attenuator settings in the IFD, which could not be controlled from the ARX II controller. The resulting dynamic range of the IDC through its various stages is shown graphically in Fig. 7. Also shown are the parameters for each stage: gain, noise figure, input 1-dB compression point, and noise bandwidth (BW). The composite assembly performance can be summarized as follows (the input step attenuator = 0):

Gain = 48 ±10 dB

Noise figure = 5.8 dB

Input 1-dB compression = −8 dBm

Noise BW = 20 MHz

2. Manual Gain Control. Overall gain control of the converter was partitioned between the first and second IFs. A manual gain control element was chosen for the 300-MHz IF in the form of a 0-to-40-dB step attenuator on the input. This control is used primarily to compensate for the uncertainty in gain in the signal path from the LNA output to the IFD output. As shown in the dynamic range plot in Fig. 7, the manual control is set to maintain a 10-dB margin between the strongest case noise power (8.4–8.5 GHz) or sinusoidal signal and the 1-dB compression point of any stage. Another consideration for the gain distribution is reverse isolation of the first LO at the IDC input. The requirement for the ARX II is to demonstrate performance at a DSN complex on a noninterference basis. In other words, any signals emanating from the ARX II should be negligible to any operational open-loop receivers in the SPC. With this in mind, enough gain was placed before the first mixer in the IDC to provide approximately 100-dB reverse isolation between the mixer LO input and the IDC input. This isolation, along with the added isolation of the IFD, was sufficient to make the LO leakage from the ARX II more than 10 dB below the weakest case carrier.

3. Automatic Gain Control. An AGC circuit was placed at the 70-MHz second IF to compensate for total signal power changes, thereby maintaining a constant power at the analog-to-digital converter (ADC) input. A ±10-dB range was used for the design to accommodate the whole range of specified system noise temperatures, although this much variation would not be expected during a single pass. For optimum sampling, the full-scale range of the ADC is equal to a 4-sigma noise event, so that the root-mean-square (RMS) voltage (1 sigma) at the ADC input is 12 dB below the saturation point, or at 2^5 bit levels for the 8-bit ADC used.

The AGC loop gain and frequency response required were dictated by the need for both an acceptable level of variation at the ADC input and the range of allowable level changes during an update period of the tracking loop processor. A first-order AGC loop was chosen with a gain of 100 (to limit output variations to ±0.1 dB over the ±10-dB input range) and a bandwidth of 10 Hz (much

slower than the lowest loop update rate of 50 Hz) [6]. A block diagram of the AGC loop is given in Fig. 8(a) and an equivalent mathematical model is shown in Fig. 8(b). The closed-loop transfer function derived in the Appendix is then given by

$$H(s) = \frac{\tau s + 1}{\tau s + G_T + 1} \tag{3}$$

where

$\tau = RC$ = loop filter time constant

$G_T = G_1\ G_2\ K_A\ K_D$ = loop gain

(Loop performance measurement data is discussed in Section VI.)

D. Amplitude and Group Delay Flatness

Various functions of the ARX II require a specified degree of amplitude and group delay flatness across the information band. The filters in the IDC are the primary source of these distortions (lack of flatness). A budget for the total system performance, including the VLBI/radio science downconverter, has been estimated and is summarized in Fig. 9. Figure 9 shows the S-band case only. For the X-band case, the VLBI/Radio Science Downconverter would have a negligible contribution to group delay ripple over the 300-to-400-MHz output range. The amplitude ripple is specified over a ±6.6-MHz span to give the worst case for telemetry performance, and the group delay ripple is over ±1 MHz to show the case for the anticipated ranging demonstration. (Measurement data on the composite performance of the IDC is discussed in Section VI.) Amplitude and group delay measurements of the SAW filter used are given in Fig. 10. It is important to note that the measurement aperture for the group delay measurement was set to 2 MHz to simulate the span of two ranging tones (at the highest 1-MHz rate). The measured ripple then corresponds to the actual residual phase difference between the two phase tones at that rate.

E. Phase and Frequency Stability

1. Allan Variance System Model. An estimate of the long-term phase stability of the IF-to-Digital Converter connected to a VLBI/Radio Science Downconverter was made in order to predict the performance of the ARX II in its DSCC demonstration configuration. An Allan variance model of the system is shown in Fig. 11. The stability numbers used were obtained from both measurements and estimates done for the radio science system and the proposed Block V Receiver System.[1] The composite stability budget, tabulated in Table 2, gives a root-sum-square (RSS) total of 2.61×10^{-15} over 1000 sec for the combined receiver and frequency and timing subsystem (FTS). This number is dominated by the hydrogen maser and the coherent reference generator (CRG) in the SPC.

2. Phase-Noise System Model. The block diagram in Fig. 11 also serves as a model for combined phase noise of the system [7]. The single-sideband phase-noise spectral density of the first LOs (8.1 GHz and 2.0 GHz) and some candidate channel select synthesizers are plotted in Fig. 12. The Hewlett-Packard 8656B synthesizer is most likely to be used for demonstrations at a DSN complex because it is a good compromise between cost and performance. The resulting X-band system phase noise with this synthesizer is shown as a separate curve. For an ARX II demonstration where phase noise is critical, such as radio science, a higher performance unit, such as a Hewlett-Packard 8662, could be used. In this case, the system phase noise would be dominated by the FTS 100-MHz noise multiplied up to the X- or S-band.

IV. Frequency Reference Generator

A number of frequency references are required to operate the ARX II and its test generator. These are 80 and 84 MHz as the two third LOs (for the digital and analog loops, respectively), 40 MHz as the sampling clock, 10 MHz as an external reference for the three synthesizers, and a 5-MHz reference for the time code translator (TCT). The ARX II Frequency Reference Generator derives these from either a 10-MHz internal crystal oscillator (TCXO), for operation in the laboratory, or the 1-, 5-, and 10-MHz FTS signals, for operation in the DSN. The block diagram for the generator is given in Fig. 13. The assembly occupies a separate 4-inch-high drawer in the ARX II system rack.

V. Test Signal Generator

A Test Signal Generator was also built as part of the ARX II system and occupies another separate drawer in the rack. The requirements for this assembly were previously summarized in Table 1, and the block diagram for the unit is shown in Fig. 14. The Test Signal Generator can operate in both a quick-test mode, with internal fixed oscillators at 70 MHz, 360 kHz, and 43.2 kHz (for carrier, subcarrier, and symbols, respectively) to simulate a

[1] T. K. Peng, *Deep Space Network System Functional Design: Block-V Receiver*, JPL D-7420 (internal document), Jet Propulsion Laboratory, Pasadena, California, July 1, 1990.

Voyager signal, and in a comprehensive test mode, where external synthesizers are used to generate all required frequencies and Doppler dynamics. The accuracy requirement for the generator is ±0.5 dB for P_c/N_0 and P_d/N_0; this is near the limit of what can be achieved with analog components over a wide dynamic range. A digital test generator, in theory, could be considerably more accurate. The basic design is an evolution of a similar unit used for the ARX I. Several features were added, such as higher subcarrier and data rates (2 MHz and 6.6 MHz, respectively), quadrature phase shift keying (QPSK) and offset quadrature phase shift keying (OQPSK), and a noise bandwidth up to 300 MHz to allow testing at the first IF of the IDC.

VI. Test Methodology and Results

A. Subsystem Amplitude and Phase Response

In order to verify the amplitude and group delay variation of the IDC over the 20-MHz passband, tests of the complete converter were conducted at different points in the 200-to-400-MHz input IF band. The test setup is shown in Fig. 15. The vector network analyzer has an internal synthesized source, and the IDC 10-MHz output is upconverted with a dual mixer scheme for phase detection in the analyzer. The results for an input at 300 ±10 MHz are shown in Fig. 16. The amplitude variation over the band is less than the worst case previously budgeted in Fig. 8. This is probably due to some averaging of ripple in the various filters. The group delay variation is consistent with the ±2.7 nsec budgeted for any 2-MHz span within ±1 MHz of band center.

B. Spurious Responses

The problem with mixer intermodulation products was discussed in Section III. As stated earlier, this is a type of spurious response that originates from externally generated interference, RFI. Predictions of single-tone IM products were previously summarized in Figs. 4 and 5. The measurement results for these same frequency inputs are summarized in Table 3. The large discrepancy between measured and predicted IM levels for the 2 × 2 products is probably due to an imbalance in the mixer circuits caused by nonoptimum packaging. Two-tone, third-order IM products are also a potential problem with any nonlinear device, but these cannot be eliminated by filtering. Rather, they are minimized by operating all receiver components in their linear range, which is inherently the case for this design. Internally generated spurious components, or self-RFI, are also a potential problem. This type of interference originates from the reference LO signals, spurious on the power supply lines (such as at the switching frequency), and from radiated or conducted interference from other components in a system rack. The proximity of digital and analog circuits can be a cause of this type of RFI. Measurements on the IDC with no input signal were made to verify that no spurious components with a P_c/N_0 above 0 dB-Hz were present in a 2-MHz band around the 10-MHz IF. These measurements were made at the input to the ADC and, therefore, did not include any potential spurious components from the ADC itself. The spurious levels over the rest of the 20-MHz IF band (outside of the center 2 MHz) were at a signal-to-noise ratio (SNR) of 20 dB-Hz or less.

C. Automatic Gain Control Step Response

A step response test of the AGC loop was conducted to verify predicted response time. Figure 17 gives a comparison of the pulse rise time for the theoretical and measured cases. The measured performance indicates a loop time constant approximately 25 percent greater than the theoretical 16 msec. This is probably due to either a lower loop gain or a greater loop-filter time constant than predicted.

D. Automatic Gain Control Phase Response

Since the phase stability and linearity of the receiver system is crucial for applications such as ranging, a test was performed to detect any group delay variation versus input level in the AGC amplifier. Many amplifiers exhibit some amplitude-modulation-to-phase-modulation conversion, especially when operated in a nonlinear range. The two sets of curves in Fig. 18 show the gain versus frequency and group delay versus frequency for the maximum and minimum AGC gain points. The nominal operating range for the IDC is ±10 dB. This test verifies that there is negligible amplitude-modulation-to-phase-modulation conversion in the AGC circuit, since the two group delay curves essentially coincide to within a few tenths of a nanosecond.

E. ADC Converter Linearity

Although the ADC converter is the link between the analog/rf receiver components and the digital signal processing functions, it is often overlooked in terms of its potential contribution of spurious components and amplitude and phase distortion. This is probably partly due to the difficulty in measuring high-speed ADC characteristics. One solution to the measurement problem is to use the digital signal processing functions of the receiver itself to characterize the imperfections of the ADC. This approach was taken for measuring harmonics due to the ADC nonlinearities. The fast Fourier transform routine used for carrier acquisition was thus utilized for measuring harmonics due to strong carriers (50 to 80 dB-Hz) at the

ADC input. The test was performed with both signal and noise present. The results of this test are summarized in Fig. 19. Due to the limited time allowed for the test, the averaging time for individual measurements was limited and the noise floor obtained was approximately −8 dB-Hz. Harmonics, therefore, were only detectable from strong input levels with carrier-to-noise ratios of 70 dB-Hz or above. Figure 19 shows the aliased output frequencies measured for inputs at 9.9 and 10.1 MHz.

VII. Conclusions

An IF-to-Digital Converter breadboard was designed to meet the requirements of the ARX II digital receiver. These requirements included near-term performance as well as goals for future Block V performance. The design of the IDC involved some cost–performance trade-offs in areas where the original performance goals could not be met with available resources. These performance areas were spurious-free dynamic range, system noise temperature degradation, and local oscillator phase noise. Functional tests of the IDC were performed, both independently and in conjunction with the signal processor, and the results compared favorably with the near-term performance requirements. To date, the IDC has been used in the ARX II system in a Doppler extraction demonstration at SPC 10 using the Pioneer 10 and Voyager 2 spacecraft. Future demonstrations are planned for telemetry, ranging, and radio science performance.

Possible improvements to meet the Block V Receiver performance requirements exist. The frequency plan could be changed by upconverting to an intermediate fixed IF to increase the spurious-free dynamic range and exceed the 100-dB goal. In addition, the 70-MHz IF could be sampled directly, using a higher speed ADC, thereby eliminating the last downconverter and its associated IM products. The characteristics of the SAW anti-aliasing filter can be optimized, with a custom design if necessary, so that the noise degradation due to aliasing meets the system requirements. Finally, a lower noise synthesizer could be used, but probably at greater cost, to meet the projected radio science system phase-noise requirements. In short, if the above-mentioned improvements were to be made to the IDC, it would meet all the performance requirements of the Block V receiver.

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Table 1. Assembly specifications

IF-to-Digital Converter	
Amplitude control	
AGC range	±10 dB
Gain	50 ±10 dB with step attenuator set to 0 dB
Gain ripple	±0.5 dB across 13.2 MHz BW
Noise figure	6.5 dB with step attenuator set to 0 dB (contribution to system NF ≤ 0.04 dB (1 percent))
Frequency	
First IF	200–400 MHz open-loop
Second IF	70 MHz open-loop, BW (1 dB) = 18.1 MHz
Third IF	10 MHz phase-locked or open-loop, BW (1 dB) = 18.1 MHz
Telemetry BW	BW (3 dB) = 19.8 MHz
Spurious at ADC output:	With no external RFI: $P_i/N_0 \leq 0$ dB-Hz over $f = 10 \pm 1$ MHz ≤ 20 dB-Hz over $f = 0$–9 MHz, 11–20 Hz With strongest case external RFI: $P_i/N_0 \leq 41$ dB-Hz over $f = 0$–20 MHz where P_i = interfering signal power
Phase stability	
Long term (del f/f)	0.07×10^{-15} over 100 sec
Phase noise	LO phase noise — using Hewlett-Packard 8656B as channel select synthesizer

Offset, Hz	SSB density, dBc/Hz
1	−67
10	−80
100	−80
1k	−85
10k	−117
100k	−138

Group delay	
Flatness	±3.0 nsec over 4 MHz BW at band center
Stability	±1.0 nsec over temperature and mechanical perturbations
Inputs/Outputs	
Inputs	First IF (200–400 MHz) $P_c = -16$ to -136 dBm $N_0 = -99$ to -136 dBm First IF test (same as principal input) Second IF test in (70 MHz) $P_c + P_D + N_0B = -28 \pm 10$ dBm all inputs, 50 ohms, VSWR ≤ 2.0 where P_c = carrier power P_D = data power N_0 = noise density B = noise bandwidth
Outputs	10-MHz digitized IF, 8-bit + clock, ECL
Monitor points	10-MHz IF test: carrier × subcarrier × data + noise, −2 dBm, 50 ohms 10-MHz IF test: carrier only, −10 dBm, 50 ohms AGC voltage monitor (panel meter)
Environmental	
Ambient temperature:	25 ±5°C

Table 1 (contd)

Frequency Reference Generator	
Reference inputs	1 MHz, 0 dBm 5 MHz, 0 dBm 10 MHz, 0 dBm all inputs: 50 ohms, VSWR $\leq$ 2.0
Frequency outputs	5 MHz, +12 dBm 10 MHz, 0 dBm, 4 outputs 40 MHz, +12 dBm 80 MHz, +9 dBm 84 MHz, +9 dBm all outputs: 50 ohms, VSWR $\leq$ 2.0, spurious $\leq$ −70 dBc
Test Signal Generator	
Modulation types	BPSK, QPSK, OQPSK Direct Manchester or NRZ Subcarrier: residual or suppressed carrier, NRZ only
Symbol rate	Subcarrier mode: 8 SPS–700 kSPS direct carrier: 100 SPS–6.6 MSPS
Carrier range	Second IF output: 70 ±1 MHz First IF output: 200–400 MHz
Subcarrier range	1 kHz to 2 MHz
Modulation index	0–90 deg
Number of subcarriers	1
Doppler simulation	
Maximum offset	2.33×10^{-4} = 2 MHz at X-band
Maximum rate	6.67×10^{-8} = 560 Hz/sec at X-band
RF output level	$P_D + P_c + N_0B = -28 \pm 10$ dBm where B = noise BW = 300 MHz P_c/N_0: max = 100 dB-Hz min = 0 dB-Hz P_D/N_0: max = 100 dB-Hz min = 0 dB-Hz
Accuracy	P_c/N_0: ±0.5 dB P_D/N_0: ±0.5 dB
Inputs	
Carrier reference	First IF: 200–400 MHz 0 to −70 dBm 50 ohms Second IF: 70 ±1 MHz 0 dBm 50 ohms
Subcarrier clock	1 kHz–2 MHz TTL square wave
Symbol clock	8 Hz–6.6 MHz TTL square wave
Outputs	Main output to IF-to-Digital Converter Monitor output (same as main) SER—symbol-error-rate reference (TTL)

Table 2. Allan sigma error budget (X-band), ARX II with VLBI downconverter

IF-to-Digital Converter (IDC)	
Component	$\times 10^{-15}$ (over 1000 sec)
First mixer[a]	0.020
Synthesizer[b]	0.070
Second mixer[a]	0.005
×8 multiplier[c]	0.005
×4 multiplier[c]	0.005
IDC RSS total	0.070

RCV and FTS combined subsystems		
Component		$\times 10^{-15}$ (over 1000 sec)
RCV		
RF cable to RF-IF		1.00
RF-IF mixer		0.70
×81 multiplier		0.50
IF cable to dist.		0.50
IF dist. (IFD)		0.50
IDC		0.07
NCO quantization		0.20
RCV RSS total		1.51
FTS		
H-maser	8400	1.50
	370	0.07
	80	0.01
		1.58
CRG		1.0
ARD		0.8
100 MHz fiber to ARD		0.4
Station cables		0.5
FTS RSS total		2.13
RCV + FTS (RSS total)		2.61

[a] $0.5 \times f_{IN}/8400$
[b] $1.0 \times f_{OUT}/8400$
[c] $0.5 \times f_{OUT}/8400$

Table 3. Single-tone mixer intermodulation products

	IM Order		$f_c - \Delta f$, MHz	Δf, MHz	R_{dB} predicted mixer suppression with filters, −dBc	Measured suppression with filters, −dBc
	M (RF)	N (LO)				
First IF to second IF downconverter (S-band), mixer input level = −10 dBm						
f_1	+3	−2	236.7	−13.3	71	65
f_2	−2	+2	285	35	80	50
f_3	−3	+3	296.7	46.7	54	50
f_4	+3	−3	343.3	93.3	>90	>90
f_5	+2	−2	355	105	>90	>90
f_{IMAGE}	+1	−1	390	140	80	80
Second IF to third IF, mixer input = −15 dbm						
f_1	−2	+2	75	5	90	50
f_2	−3	+3	76.7	6.7	69	56
f_3	+3	−3	83.3	13.3	>90	>90
f_4	+2	−2	85	15	>90	>90
f_{IMAGE}	+1	−1	90	20	60	60

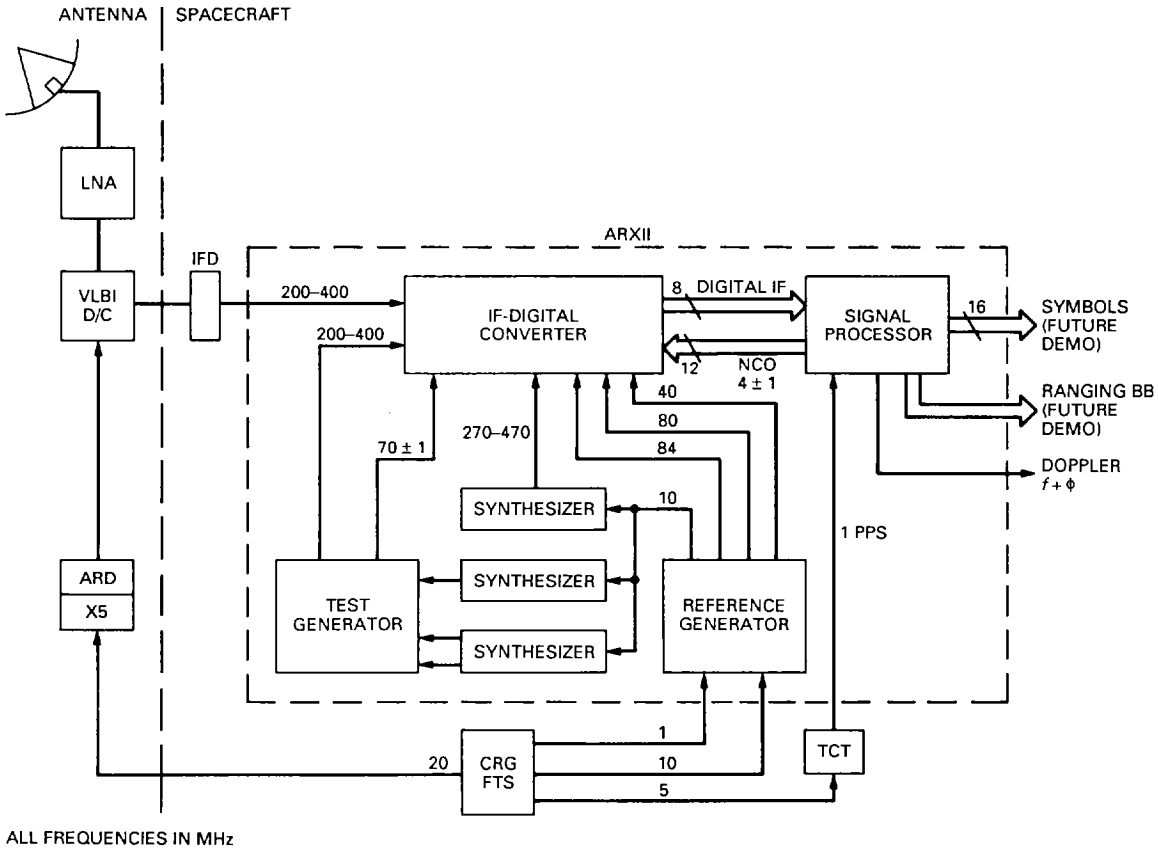
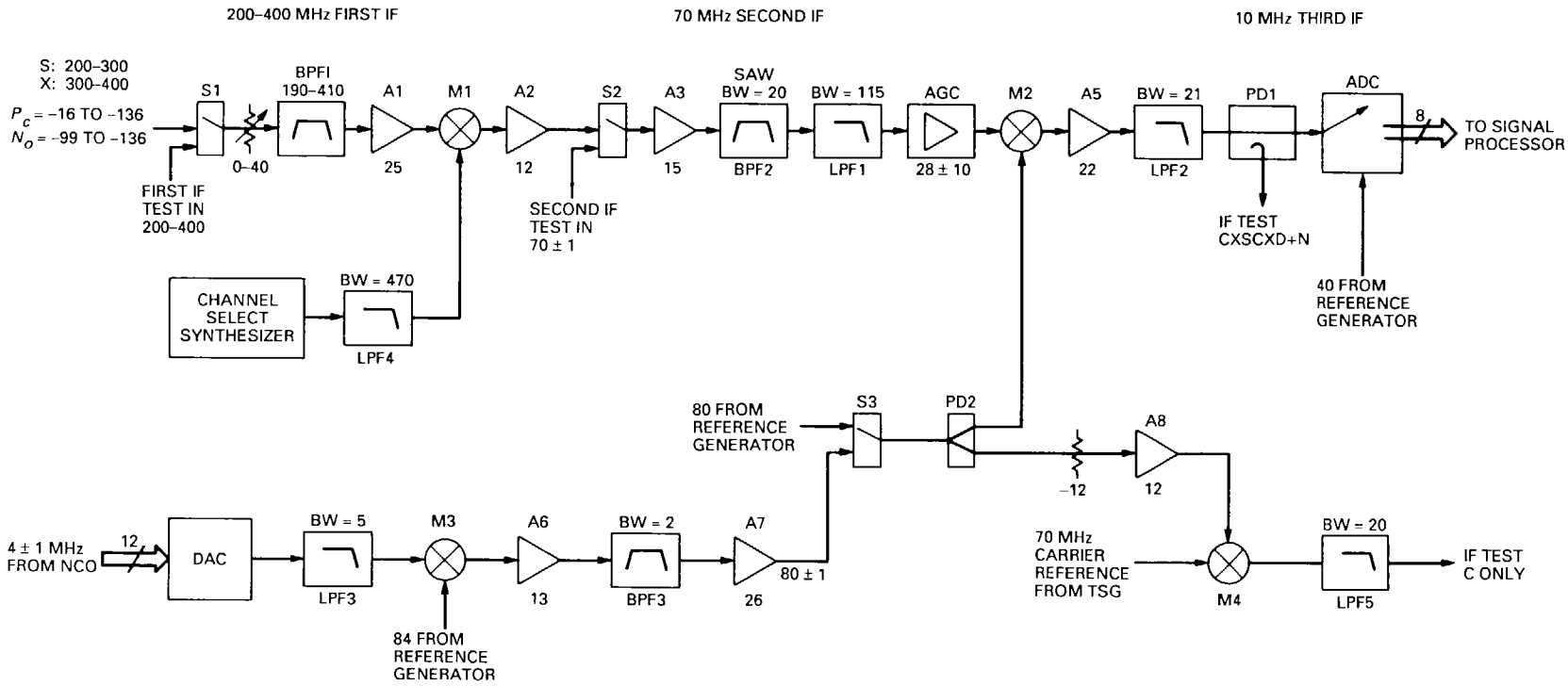


Fig. 1. ARX II: DSCC demonstration configuration.



ALL FREQUENCIES IN MHz.
NUMBERS BELOW COMPONENTS ARE INSERTION GAIN (db).

Fig. 2. IF-to-Digital Converter functional block diagram.

Fig. 3. ARX II rack assembly.

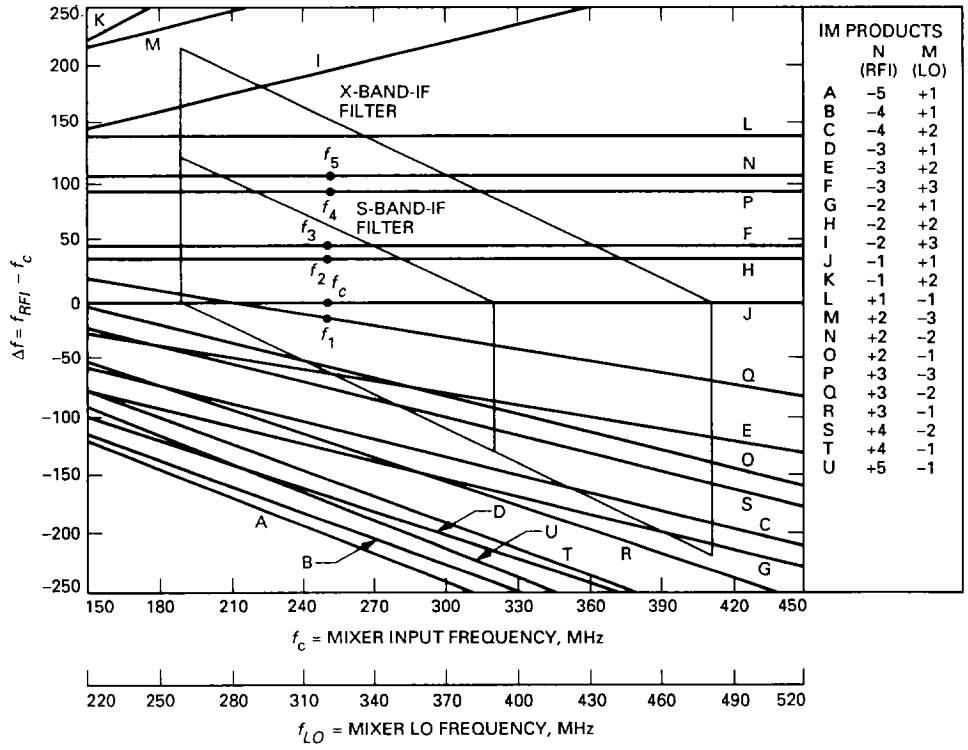
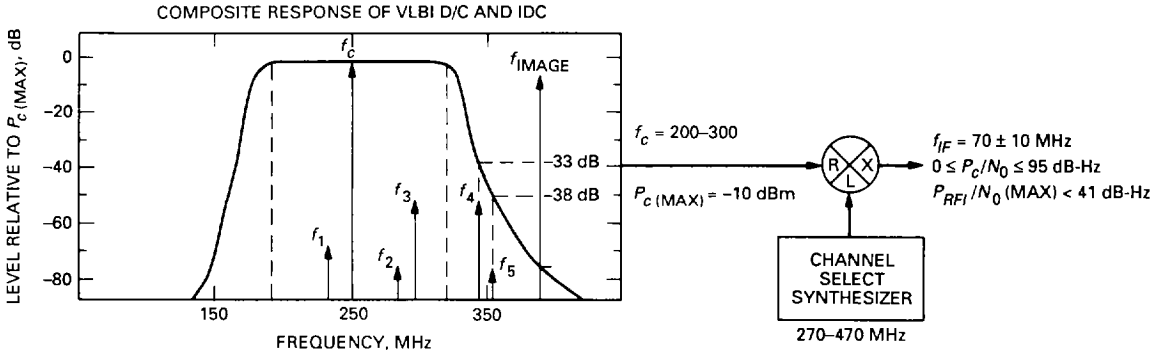


Fig. 4(a). Mixer IM products versus mixer input frequency, first IF to second IF downconverter.



	IM ORDER		f_{RFI}						
	M (RF)	N (LO)	$f_c + \Delta f$, MHz (FOR f_{IF} = 70)	Δf, MHz ($f_{RF} - f_c$)	R_{dB}* MIXER SUPPRESSION FOR -10 dBm IN	MAXIMUM RFI WITHOUT FILTER P_{RFI}/N_0, dB-Hz	REQUIRED FILTER REJECTION, H_f, dB	ACTUAL FILTER REJECTION, dB	MAXIMUM RFI WITH FILTER P_{RFI}/N_0, dB-Hz
f_c	-1	+1	250	0	0	-	-	-	-
f_1	+3	-2	236.7	-13.3	71	24	9.7	0	24
f_2	-2	+2	285	35	80	15	10	0	15
f_3	-3	+3	296.7	46.7	54	41	15	0	41
f_{IMAGE}	+1	-1	390	140	0	95	100	78	17
f_4	+3	-3	343.3	93.3	54	41	15	33	-59
f_5	+2	-2	355	105	80	15	10	38	-61

*MANUFACTURERS DATA, WJ MGE.

$$H_f = \frac{-100 + R_{dB}}{M}$$

Fig. 4(b). Mixer image and IM product rejection, first IF to second IF downconverter.

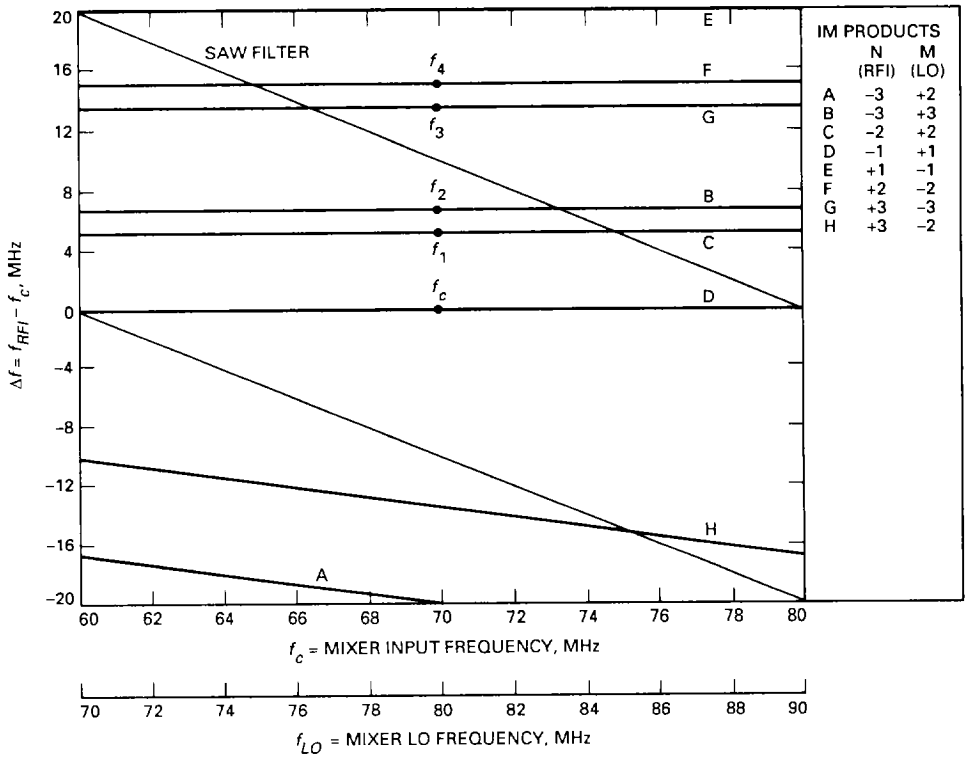
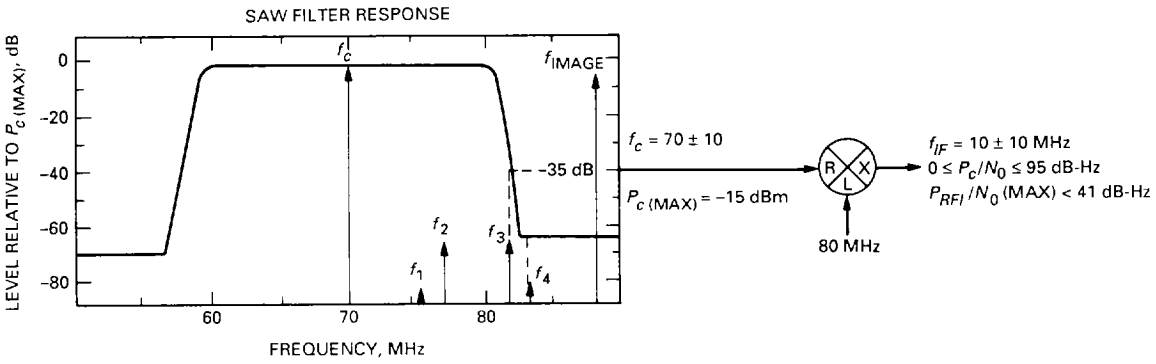


Fig. 5(a). Mixer IM products versus mixer input frequency, second IF to third IF downconverter.



	IM ORDER		f_{RFI} $f_c + \Delta f$, MHz (FOR $f_{OUT} = 70$)	Δf, MHz ($f_{RF} - f_c$)	R_{dB}* MIXER SUPPRESSION FOR −15 dBm IN	MAXIMUM RFI WITHOUT FILTER P_{RFI}/N_0, dB-Hz	REQUIRED FILTER REJECTION, H_f, dB	ACTUAL FILTER REJECTION, dB	MAXIMUM RFI WITH FILTER P_{RFI}/N_0, dB-Hz
	M (RF)	N (LO)							
f_c	−1	+1	70	0	0	–	–	–	–
f_1	−2	+2	75	5	90	5	5	0	5
f_2	−3	+3	76.7	6.7	69	26	10	0	26
f_{IMAGE}	+1	−1	90	20	0	95	100	60	35
f_3	+3	−3	83.3	13.3	69	26	10	35	−79
f_4	+2	−2	85	15	90	5	5	60	−115

*MANUFACTURERS DATA, WJ MGD.

$$H_f = \frac{-100 + R_{dB}}{M}$$

Fig. 5(b). Mixer image and IM product rejection, second IF to third IF downconverter.

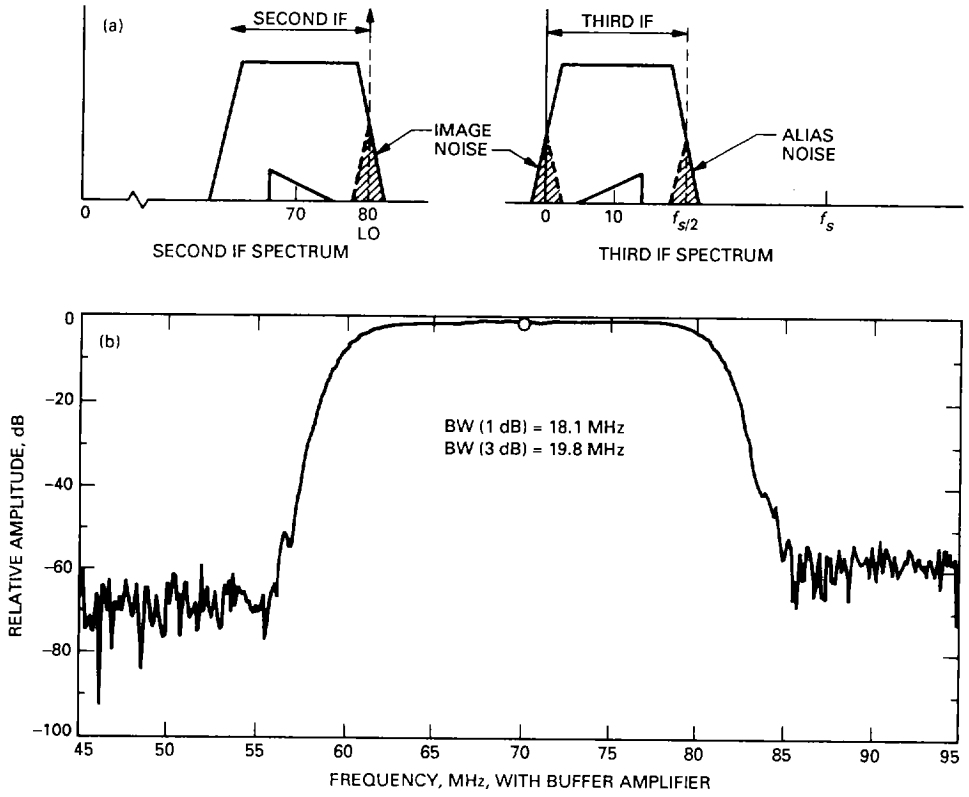
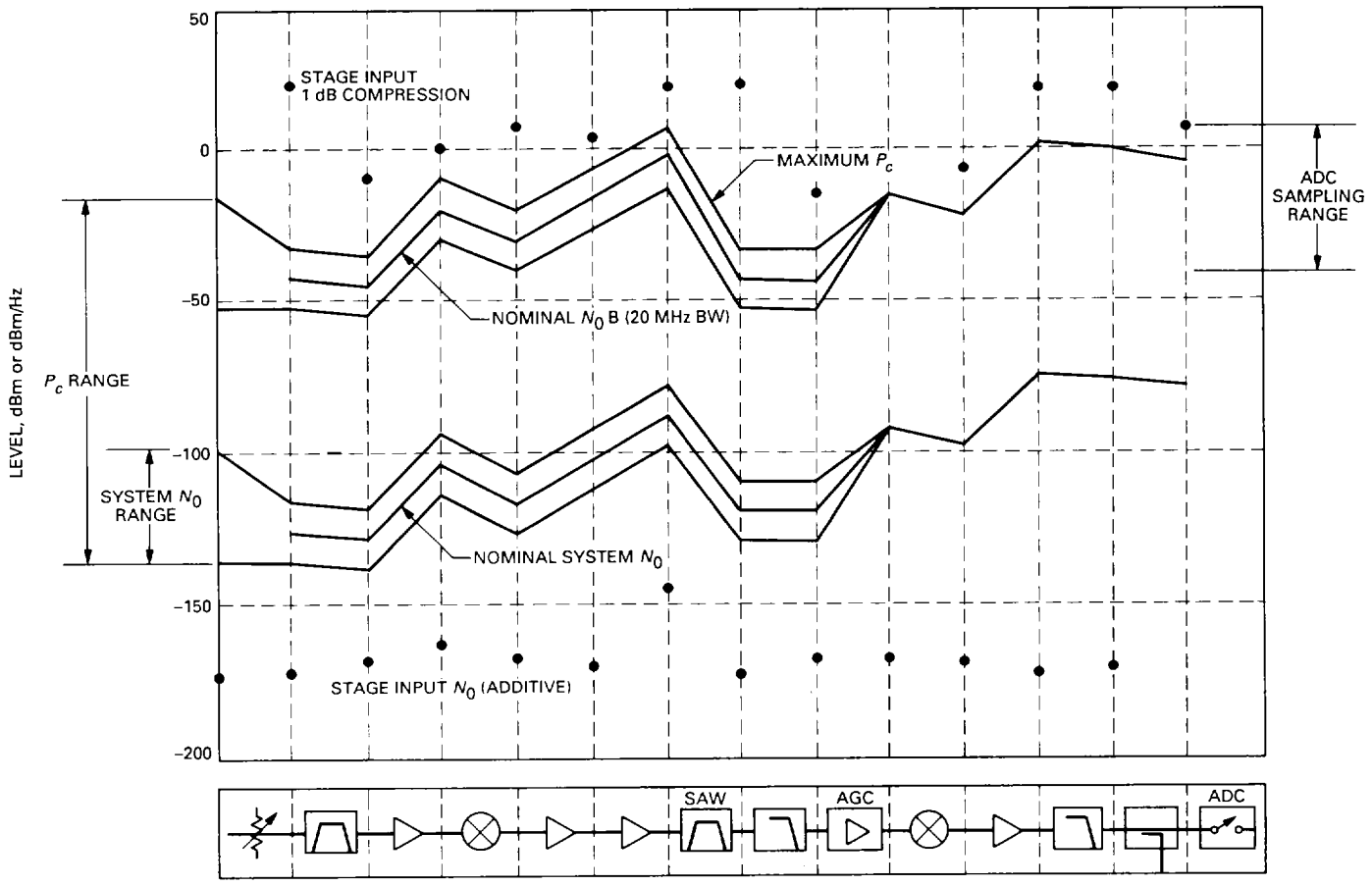


Fig. 6. Broadband noise rejection.

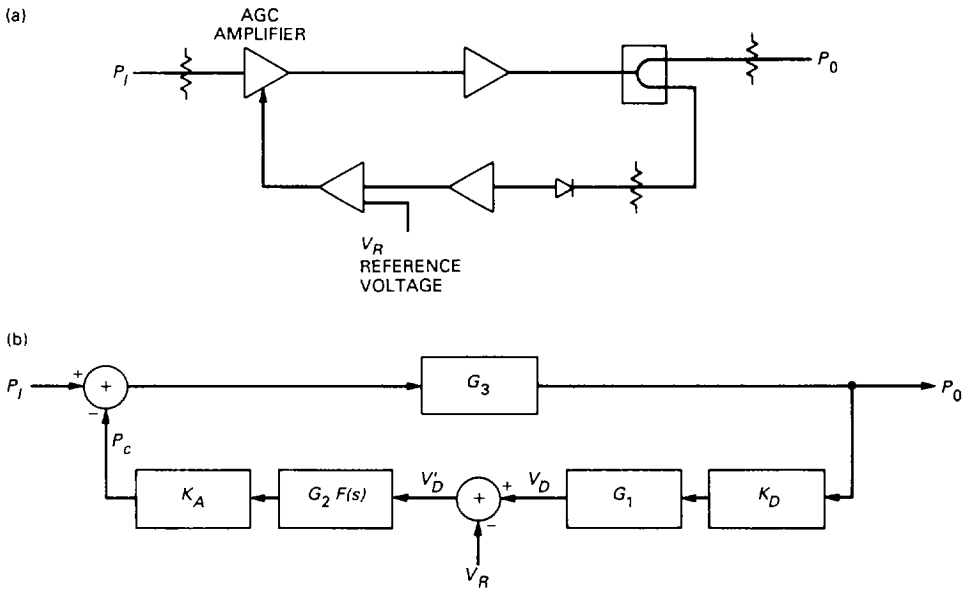


	ATTENUATOR	BPF1	A1	M1	A2	A3	BPF2	LPF1	A4	M2	A5	LPF2	PD1	
GAIN, dB	0 (-40)	-2	25	-10	12	15	-29	-1	28 ±10	-7	22	-1	-4	-
NF, dB	0-40	2	5.7	10	7	3	29	1	7	7	5.7	1	4	-
INPUT COMPRESSION, dBm	-	20	-10	0	-6	-4	20	20	-15	0	-7	20	20	7
NOISE BW, MHz	1000	220	500	500	400	400	18.2	130	120	200	500	23	120	40

SUBSYSTEM SUMMARY

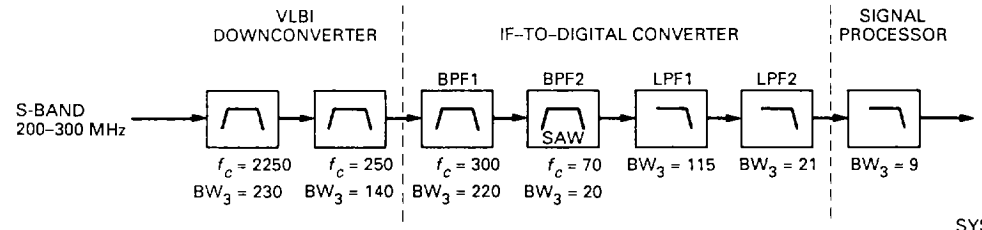
GAIN, dB	48 ±10
NF, dB	5.8
INPUT COMPRESSION, dBm	-23
NOISE BW, MHz WITH ATTENUATOR	20

Fig. 7. IF-to-Digital Converter dynamic range plot.



V'_D	DETECTOR AMPLIFIER OUTPUT WITH OFFSET	G_1	DC AMPLIFIER GAIN, 100 V/V
V_D	DETECTOR AMPLIFIER	G_2	DC AMPLIFIER GAIN, 50 V/V
V_R	REFERENCE VOLTAGE	G_3	REFERENCE FREQUENCY GAIN
P_0	AGC LOOP OUTPUT POWER	K_A	AGC AMPLIFIER GAIN, 15 dB/V
P_I	AGC LOOP INPUT POWER	$F(s)$	LOOP FILTER RESPONSE, 1/RCS + 1, RC = 1.6 sec
K_D	POWER DETECTOR SENSITIVITY, 1.3 mV/dB	s	LAPLACE COMPLEX FREQUENCY VARIABLE

Fig. 8. AGC loop: (a) block diagram, and (b) mathematical model.



								SYSTEM TOTALS
ΔA, AMPLITUDE RIPPLE, dB OVER Δf = ±6.6 MHz[a]	±0.02	±0.02	±0.05	±0.3	±0.1	±0.3	±0.1	±0.89
Δτ, GROUP DELAY RIPPLE, ns OVER Δf = ±1 MHz[b,d]	±0.02[d]	±0.02[d]	±0.05[d]	±1.5[c]	±0.05[d]	±0.9[d]	0	±2.72

[a] 6.6 MHz IS MAXIMUM REQUIRED DATA RATE.
[b] 1 MHz IS MAXIMUM REQUIRED RANGING CODE RATE.
[c] $\Delta\tau = \Delta\phi/(360)\,\Delta f$, WHERE $\Delta\phi$ = PHASE RIPPLE, Δf = 2 MHz.
[d] $\Delta\tau = (d\tau/df)f_{IN} - \Delta f$, WHERE Δf = 2 MHz.

Fig. 9. ARX II with VLBI downconverter: system amplitude and group delay variation budget S-band example with input at 2200 MHz.

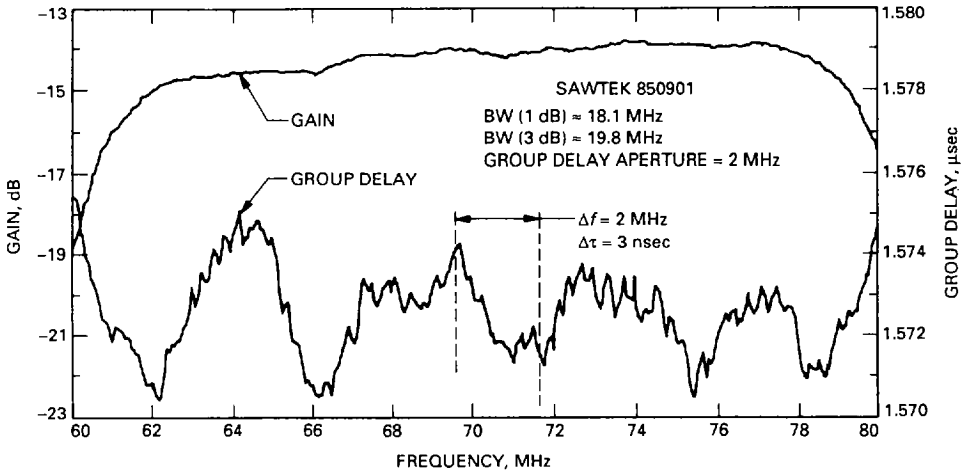
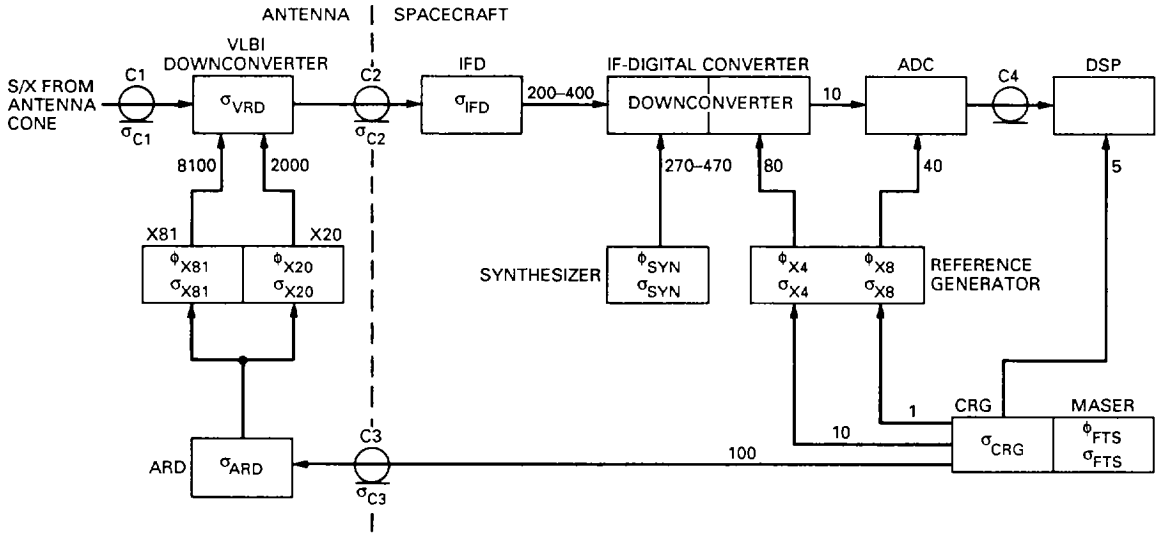


Fig. 10. SAW filter amplitude and group delay ripple.



ALL FREQUENCY IN MHz

CABLES:

- C1 HARD LINE FROM LNA
- C2 300 MHz HARD LINE
- C3 FTS 100 MHz FIBER OPTIC (PLANNED)
- C4 DIGITAL IF

SYSTEM PHASE NOISE CALCULATION

$\phi_0^{-2}(f)$ = DSB PHASE JITTER VARIANCE AT f

$\phi_{SYS}^{-2}(f) = \phi_2^{-2} + \ldots + \phi_1^{-2}$

$\mathscr{L}(f) = 10 \log \phi_{SYS}^{-2}(f)/2$ = SSB PHASE NOISE DENSITY, dBc/Hz

SYSTEM ALLAN VARIANCE CALCULATION

$\sigma_{SYS} = \sqrt{\sigma_1^2 + \ldots + \sigma_n^2}$

$\sigma_{SYS}(1000 \text{ sec}) = 2.61 \times 10^{-15}$

ASSUMING C3 IS FIBER OPTIC LINK AND $\sigma_{SYN}(1000) = 1 \times 10^{-15}$ AT 370 MHz

Fig. 11. Allan variance and phase-noise system model.

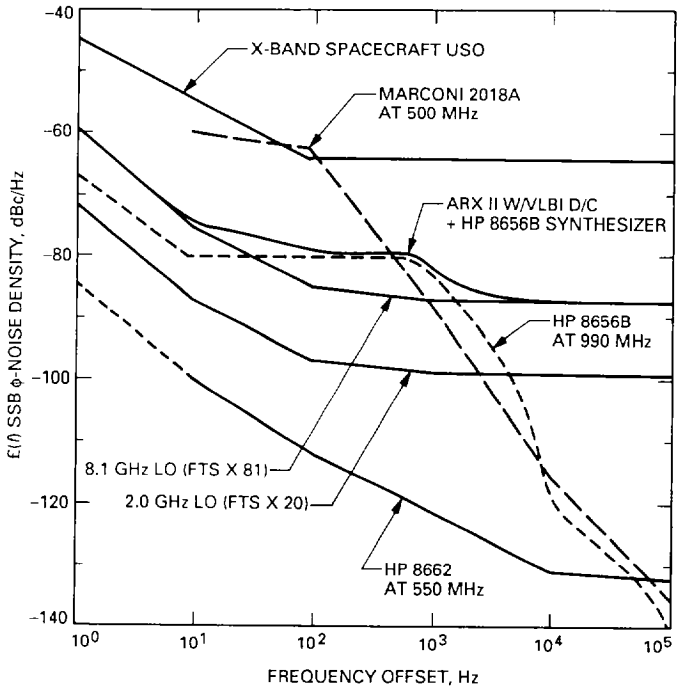


Fig. 12. SSB phase-noise spectral density, ARX II with VLBI downconverter.

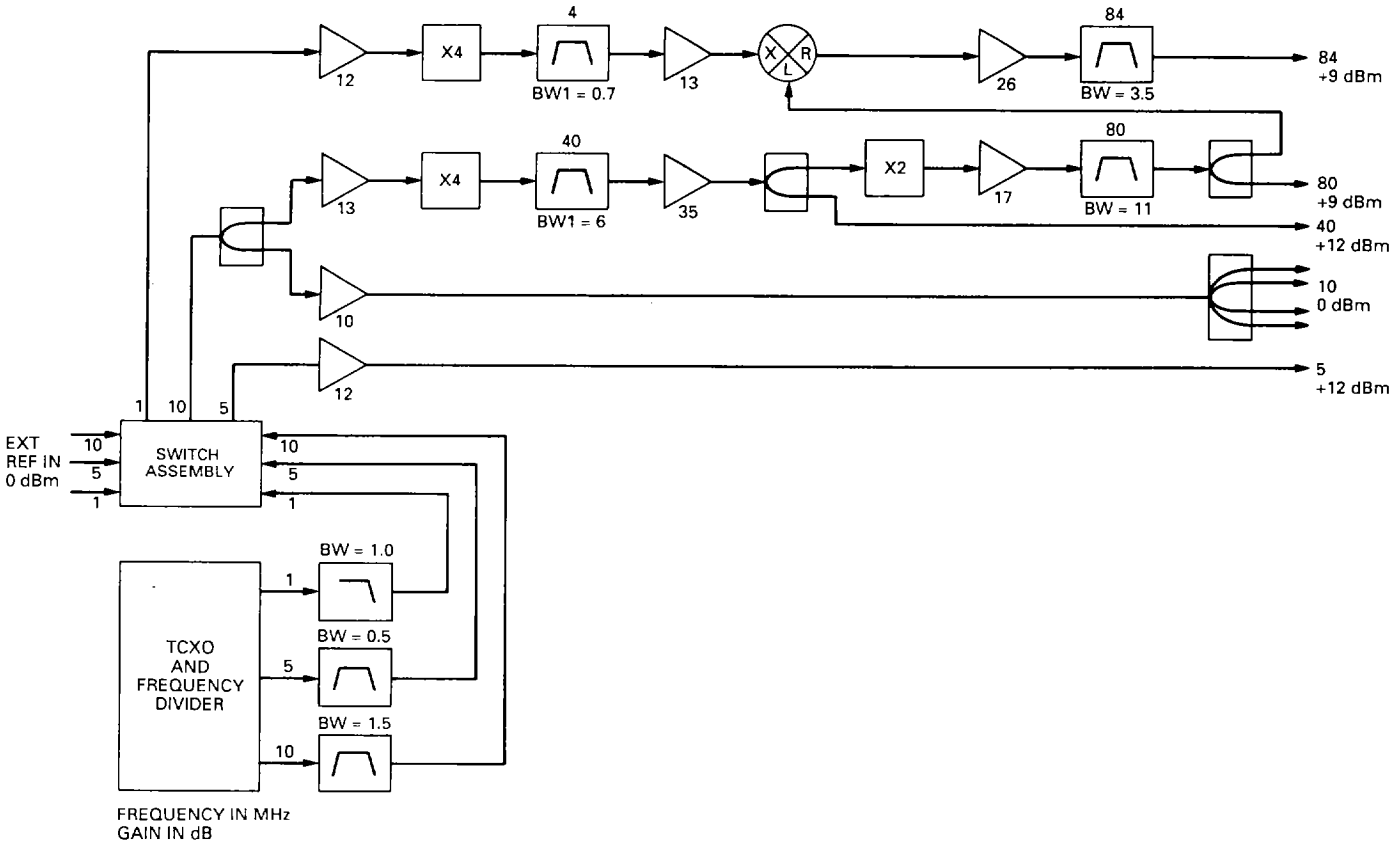


Fig. 13. Frequency Reference Generator block diagram.

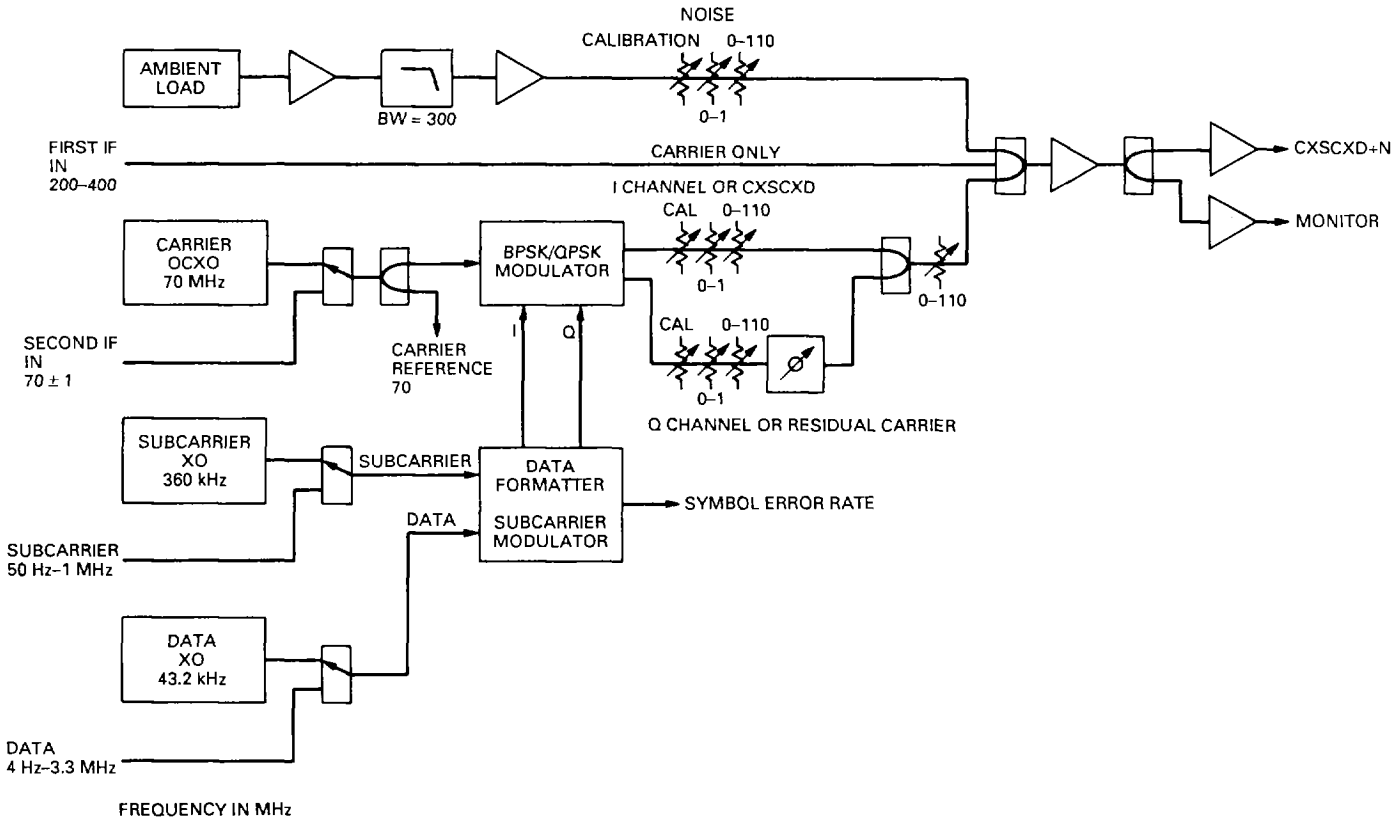


Fig. 14. Test Signal Generator block diagram.

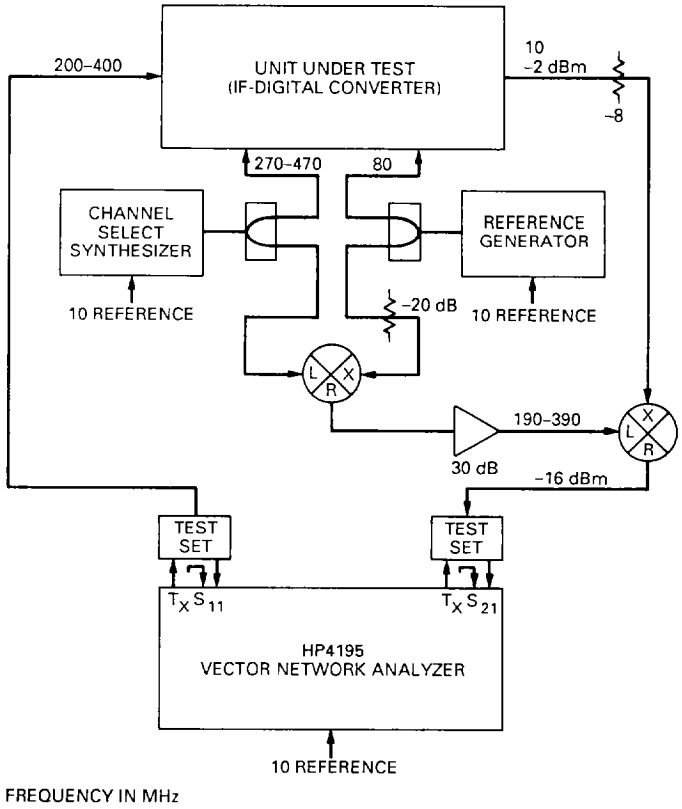


Fig. 15. IF-to-Digital Converter amplitude and phase response test setup.

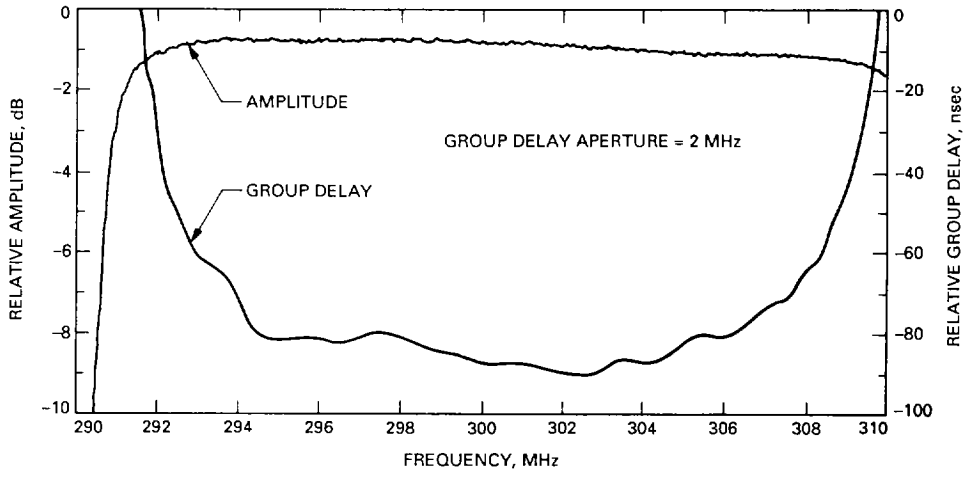


Fig. 16. IF-to-Digital Converter amplitude and group delay response at 300 MHz.

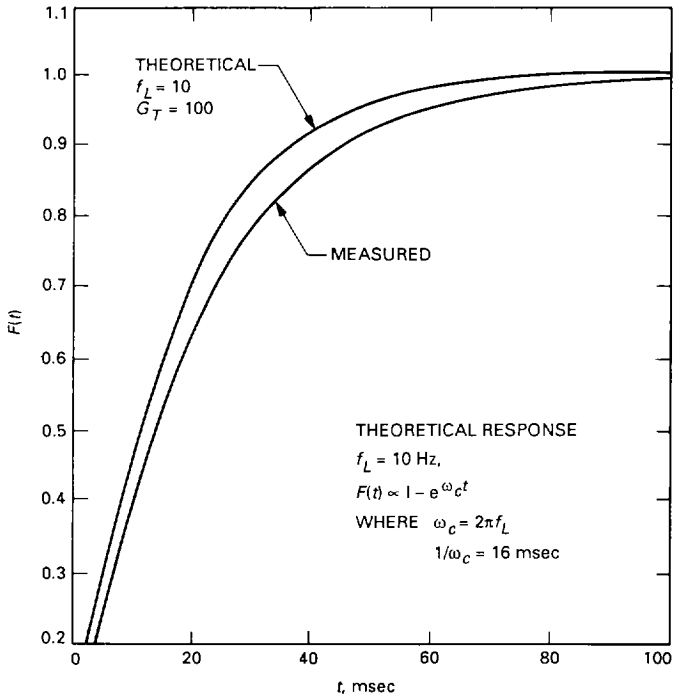


Fig. 17. AGC loop step response.

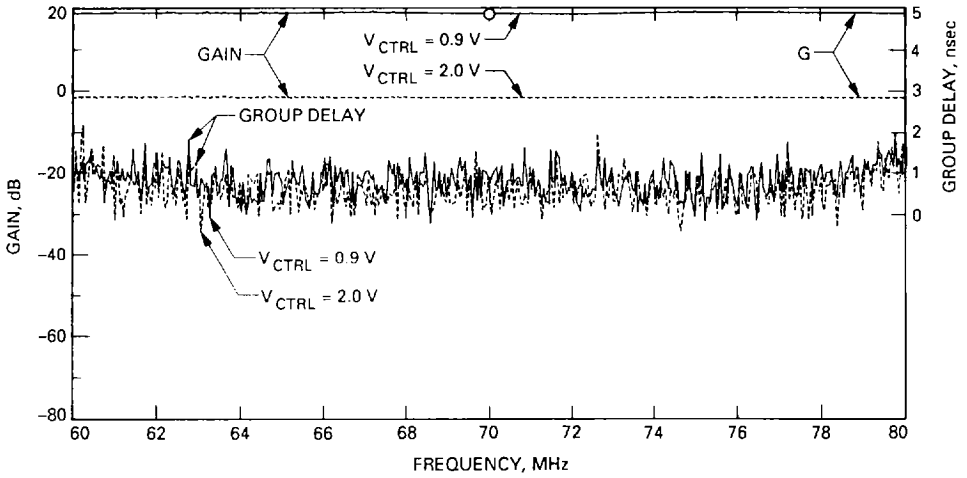
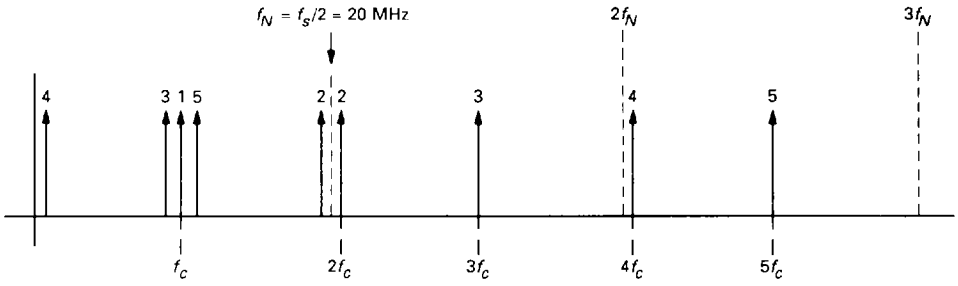


Fig. 18. AGC amplifier gain and group delay versus control voltage.



HARMONIC NUMBER	HARMONIC FREQUENCY	ALIASED FREQUENCY
1	10.1	10.1
2	20.2	19.8
3	30.3	9.7
4	40.4	0.4
5	50.5	10.5
7	70.7	9.3

SAMPLED HARMONIC SPECTRUM FOR f_c = 10.1 MHz
SAMPLE RATE = 40 MHz

FFT PARAMETERS:

RATE = 100 Hz
SIZE = 1024
ITERATIONS = 3
RESULTANT NOISE FLOOR ≈ –8 dB-Hz

MEASURED HARMONIC LEVELS
ADC UNDER TEST: DATEL ADC-303

f_{IN}, MHz	ADC INPUT LEVEL		ADC OUTPUT HARMONIC LEVEL, dBc			
	P_c/N_0, dB-Hz	% F.S.				
9.9			HARMONIC NUMBER	3	5	7
			ALIASED HARMONIC FREQUENCY, MHz	10.3	9.5	10.7
	80	24		–62	–70	≤ –80
	70	15		–72	–76	≤ –80
	60	6		≤ –72	≤ –76	≤ –80
	50	2		≤ –72	≤ –76	≤ –80
10.1			HARMONIC NUMBER	3	5	7
			ALIASED HARMONIC FREQUENCY, MHz	9.7	10.5	9.3
	80	24		–61	–67	≤ –80
	70	15		–72	–75	≤ –80
	60	6		≤ –72	≤ –75	≤ –80
	50	2		≤ –72	≤ –75	≤ –80

Fig. 19. Analog-to-digital converter linearity test.

Appendix

Derivation of AGC Loop Transfer Function

$$V_D = P_0 G_1 K_D$$

$$V_D' = P_0 G_1 K_D - V_R$$

$$P_c = K_A G_2 F(s)[P_0 G_1 K_D - V_R]$$

$$P_0 = (P_I - K_A G_2 F(s)[P_0 G_1 K_D - V_R])G_3$$

$$= (P_I + V_R K_A G_2 F(s) - P_0 G_T F(s))G_3$$

where

$$G_T = G_1 G_2 K_A K_D$$

$$P_0 = P_I/(1 + G_T F(s)) + V_R[G_2 K_A F(s)/(1 + G_T F_s)]$$

$$\text{loop transfer function} = \frac{dP_0}{dP_I} = \frac{1}{1 + G_T F(s)} = H(s)$$

$$H(s) = \frac{1}{1 + G_T F(s)} = \frac{RCs + 1}{RCs + G_T + 1}$$

when

$$F(s) = \frac{1}{RCs + 1} \text{ (first-order LPF)}$$

determination of loop filter time constant for

$$\text{loop BW} = f_L = 10 \text{ Hz}$$

$$w_c = 2\pi f_L$$

$$\text{loop gain} = G_T = 100$$

set

$$|H(s)| = \frac{\sqrt{(RCw)^2 + 1}}{\sqrt{(RCw)^2 + (G_T + 1)^2}} = \frac{1}{\sqrt{2}}$$

then

$$RC = \frac{\sqrt{(G_T + 1)^2 - 2}}{w_c} = 1.6 \text{ sec}$$

Note that all variables refer to Fig. 8.