

Application of Multirate Digital Filter Banks to Wideband All-Digital Phase-Locked Loops Design

R. Sadr, B. Shah, and S. Hinedi
Communications Systems Research Section

A new class of architecture for all-digital phase-locked loops (DPLL's) is presented in this article. These architectures, referred to as parallel DPLL (PDPLL), employ multirate digital filter banks (DFB's) to track signals with a lower processing rate than the Nyquist rate, without reducing the input (Nyquist) bandwidth. The PDPLL basically trades complexity for hardware-processing speed by introducing parallel processing in the receiver. It is demonstrated here that the DPLL performance is identical to that of a PDPLL for both steady-state and transient behavior. A test signal with a time-varying Doppler characteristic is used to compare the performance of both the DPLL and the PDPLL.

I. Introduction and Background

Implementation of wideband phase-locked loops (PLL's) has various applications in the areas of ranging, navigation, communications, and many other fields, where it is desirable to coherently track a continuous waveform (CW) signal with a particular Doppler profile. Such scenarios arise in Earth-orbiting satellites or in deep space links where a satellite or a probe is capable of transmitting signals in various channels (all within the same band) spanning a few hundred megahertz. Currently, superwide PLL's with a front-end bandwidth in the neighborhood of a gigahertz are implemented using analog devices as the digital technology is not mature enough to operate at these high clock rates. Digital PLL's, implemented with comple-

mentary metal-oxide semiconductor (CMOS) or gallium arsenide (GaAs) technologies, can operate at 100 MHz, hence covering a 50-MHz bandwidth at best.

For example, consider the Block V receiver¹ which samples the signal at 160 MHz and then processes these samples at 80 MHz. In order to cover the 100-MHz allocated bandwidth at X-band, preselect filters (see Fig. 1) are used to downconvert a portion of the spectrum to the appropriate intermediate frequency (IF) for digitization. If the Doppler rate were to span a bandwidth larger than the

¹ *Block V Receiver, Subsystem Design Review, JPL D-7420 (internal document), Jet Propulsion Laboratory, Pasadena, California, June 1992.*

preselect filter, the receiver would have to be reset in the middle of a track and then restarted with the output of a different preselect filter. In the future when the DSN operates at Ka-band (33 GHz), the allocated bandwidth will be about 500 MHz and more preselect filters will be required. The Doppler rates at Ka-band can easily reach 1 kHz/sec (the Mars Observer spacecraft experiences a two-way Doppler of 800 Hz/sec in the Ka-band Link Experiment) requiring Doppler tuning using predicts to center the signal in the passband of the appropriate preselect filter.

Advancements in high-speed digital integrated circuit technology enable high-end data acquisition systems to sample signals in excess of hundreds of megahertz. However, digital signal-processing operations (such as filtering, mixing, etc.) of these samples are still not cost-effective and sometimes not even feasible at these rates. A survey of technology (as of December 1991) was performed for high-speed state-of-the-art signal-processing hardware, as shown in Table 1. The total power consumed by these high-speed circuits is excessive, thereby requiring large heat sinks and specially designed boards for proper heat conduction and dissipation. Furthermore, to develop digital hardware at speeds around 100 MHz, it becomes necessary to use extremely accurate scopes and test equipment that could be another major cost-bearing investment on the part of the developer. Naturally one wonders whether it is possible to devise architectures that can employ a low-power CMOS that, at its best, can be clocked at a speed of 75 MHz or lower. This would significantly reduce the cost of development, the cost of the components, and that of the end product as a whole.

This article focuses on a new class of wideband all-digital PLL (DPLL) architectures that employ parallel signal-processing techniques to reduce the processing rate to below the Nyquist rate, while still maintaining a super-wide front-end bandwidth. As an example, a CW signal in principle can be sampled at 1 GHz (with a corresponding front-end bandwidth of 500 MHz) and processed in parallel using 20 channels, each with a 50-MHz clock, to provide a continuous coherent reference, even if the signal's Doppler profile spans the full 500-MHz bandwidth. The new architectures presented in this article, referred to as parallel DPLL (PDPLL), employ multirate digital filter banks (DFB's) to process the signal. There are many possible approaches [1-3] for designing DPLL's for CW tones. A discussion of the approaches and the merits of each approach is beyond the scope of this article. Here, the application of DFB to the DPLL is studied. In Section II, the DPLL is briefly described, and in Section III, the PDPLL is introduced and discussed. The simulation results and

the realization of a particular PDPLL are outlined in Section IV. The design methodology and the characteristics of the DFB are outlined in the Appendix. The discussion begins with a brief background of DPLL theory.

II. DPLL Operation

A general DPLL block diagram is depicted in Fig. 2. The received signal $r(t)$ is assumed to be a single tone embedded in noise, i.e.,

$$r(t) = \sqrt{2P_c} \sin(\Theta_c(t)) + n(t) \quad (1)$$

where

P_c = the carrier power in watts (W)

$\Theta_c(t) = \omega_c t + \theta_c$ is the total carrier phase in radians

$n(t)$ = the additive white Gaussian noise (AWGN) process with two-sided power spectral density, $N_0/2$ W/Hz

The received signal is first band-limited by an anti-aliasing filter, then bandpass sampled to form the DPLL input. The sampled input, $r(nT_s)$ in Fig. 2, is given as (the time between samples T_s is omitted in the following equations to allow a simpler notation)

$$r(n) = \sqrt{2P_c} \sin(\Theta_c(n)) + n_{bp}(n) \quad (2)$$

where the discrete-time bandpass noise process is given by

$$n_{bp}(n) = \sqrt{2} n_c(n) \cos(\Theta_c(n)) - \sqrt{2} n_s(n) \sin(\Theta_c(n)) \quad (3)$$

and $n_c(n)$ and $n_s(n)$ are statistically independent, band-limited, with a two-sided bandwidth of $2Bn$ Hz and a two-sided power spectral density level of $N_0/2$ W/Hz.

The DPLL error signal is obtained by mixing $r(n)$ with $\cos(\hat{\Theta}_c(n))$ and then lowpass filtering the mixer output to simultaneously retain the resulting dc term and suppress the double frequency term. The term $\hat{\Theta}_c(n)$ is an estimate of the incoming carrier phase $\Theta_c(n)$. Assuming an ideal lowpass filter and $N = 1$, the input to the loop filter in Fig. 3 is given as

$$\begin{aligned} \hat{\phi}_c(n) = & \sqrt{P_c} \sin(\phi_c(n)) \\ & + n_c(n) \cos(\phi_c(n)) - n_s(n) \sin(\phi_c(n)) \end{aligned} \quad (4)$$

where $\phi_c(n) = \Theta_c(n) - \hat{\Theta}_c(n)$ is the actual total phase error to be estimated. The loop filter output, $\hat{f}(n)$, is used to update the incoming carrier phase estimate, as follows (assuming $N = 1$ in Fig. 3):

$$\hat{\Theta}_c(n+1) = \hat{\Theta}_c(n) + 2\pi\hat{f}(n)T_u \quad (5)$$

The loop filter transfer function for a third-order loop is given by

$$F(z) = G_1 + G_2 \frac{z}{z-1} + G_3 \left(\frac{z}{z-1} \right)^2 \quad (6)$$

where $G_1 = \frac{rd}{2\pi T_u}$, $G_2 = \frac{rd^2}{2\pi T_u}$, $G_3 = \frac{krd^3}{2\pi T_u}$, and

$$d = \frac{4B_L T_u (r-k)}{r(r-k+1)} \quad (7)$$

The parameter B_L in Eq. (7) denotes the design or equivalent one-sided analog loop bandwidth in hertz, $T_u = NT_s$ is the loop update interval, r is typically 2 or 4 and is equal to 4ξ where ξ is the analog damping ratio and k is a loop gain parameter for a third-order loop with typical values ranging from $1/4$ to $1/2$. The actual loop bandwidth, B_L^* , might be larger than B_L , depending on the product $B_L T_u$. Generally for $B_L T_u < 0.05$, the actual loop bandwidth is very close to the analog loop bandwidth B_L .

The tracking performance of the DPLL is well known [1] to be related to the loop bandwidth and carrier-to-noise density ratio as follows:

$$\sigma_{\phi_c}^2 = \frac{N_o B_L}{P_c} \quad (8)$$

where $\sigma_{\phi_c}^2$ is the variance of the phase error $\phi_c(n) = \Theta_c(n) - \hat{\Theta}_c(n)$.

The DPLL described in this section requires that the analog-to-digital (A/D) output $r(n)$ be downconverted and filtered at the sampling rate. Hence, with the exception of the loop filter, which can be implemented at the lower update rate, all the DPLL components must operate at the higher sampling rate. This is undesirable because the implementation cost of post-sampling operations, such as downconversion and filtering, limit the A/D conversion rate, and consequently, the Nyquist bandwidth. One way to circumvent this problem is by introducing a multirate

DFB between the A/D and DPLL. As shown in the next section, a DPLL together with a DFB, or PDPLL, can track a signal over the Nyquist band but with a DPLL that operates at a much lower rate than the conventional DPLL described in this section.

III. Multirate DFB Implementation of DPLL

Multirate DFB's have been studied extensively in the past [4,5]. Let $H(z)$ denote the transfer function of an arbitrary digital filter, i.e.,

$$H(z) = \sum_{k=-\infty}^{\infty} z^{-k} h_k \quad (9)$$

where $\{\dots h_2, h_{-1}, h_0, h_1, h_2 \dots\}$ is the impulse response of the filter. It is possible to represent $H(z)$ in terms of its M -component polyphase form

$$H(z) = \sum_{k=0}^{M-1} z^{-k} E_k(z^M) \quad (10)$$

where the coefficients

$$e_k(n) = h(nM+k), \quad \forall 0 \leq k \leq M-1 \quad (11)$$

and $E_k(z)$ is the z -transform of $e_k(n)$ and is called the k th polyphase component of $H(z)$. The expansion in Eq. (10) is simply the decomposition of $\{h(n)\}$ into M -subsequence $e_k(n)$. For example, by grouping the impulse response coefficients $h(n)$ into even- and odd-numbered samples, i.e., $e_0(n) = h(2n)$ and $e_1(n) = h(2n+1)$, the transfer function $H(z)$ may be represented as

$$H(z) = E_0(z^2) + z^{-1} E_1(z^2) \quad (12)$$

where

$$E_0(z) = \sum_{n=-\infty}^{\infty} h(2n)z^{-n} \quad (13a)$$

and

$$E_1(z) = \sum_{n=-\infty}^{\infty} h(2n+1)z^{-n} \quad (13b)$$

An important property of this representation is that if the filter is followed by a decimation operation, then the filtering operation and the decimation can be commuted.

This property, known as the Noble identity, is depicted in Fig. 4. With the application of the Noble identity to the polyphase representation of Eq. (10), the filter $H(z)$ can be redrawn, as shown in Fig. 5. This representation is also referred to as the blocked version of the prototype filter $H(z)$. The key advantage of using the model shown in Fig. 5(b) is that the processing rate in each filter bank is a factor of M slower than the sampling clock. The polyphase representation results in an efficient rearrangement of the computations of the filtering operation. This effectively distributes the computations into a set of parallel filter banks operating at a lower speed. This, in turn, reduces the speed constraints on the digital signal processing hardware, thereby enabling it to process samples at a rate much lower than the sampling rate.

In application to a DPLL, as shown in Fig. 2, a full band filter $G(z)$ is inserted at the output of the A/D before the input to the mixer, as depicted in Fig. 6(a). For all practical purposes, the insertion of this digital filter does not alter the performance of the loop as it is a bandpass filter, with a bandwidth identical to that of the bandpass filter prior to the A/D conversion in Fig. 2. Consider decomposing the filter $G(z)$ into M sub-band parallel filters, $G_0(z), G_1(z), \dots, G_{M-1}(z)$, where $G_i(z)$ is a bandpass filter that passes a portion of the spectrum, as shown in Fig. 6(b). Since the input to the DPLL is a CW tone, it occupies a single filter at any given time and, therefore, only the output of that specific filter needs to be processed by the DPLL. In this case, the adder can be replaced by a multiplexer, which only passes the output of the appropriate filter to the DPLL. These filters are implemented at the sampling rate and the DPLL is operating (mixing and phase estimating) also at the sampling rate. Note that since each sub-band filter $G_i(z)$ has a bandwidth equal to $1/M$ of the bandwidth of $G(z)$, the output rate of the sub-band filters can therefore be decimated by a factor M while still satisfying the bandpass sampling theorem [6]. In this case, the DPLL can thus operate at $1/M$ of the sampling rate without any loss of information, as depicted in Fig. 6(c). Each branch now consists of a bandpass filter followed by a decimator. Each filter can be decomposed in terms of its polyphase components, as given by Eq. (10), i.e.,

$$G_i(z) = \sum_{k=0}^{M-1} z^{-k} E_{k,i}(z^M) \quad (14)$$

and since the filter is followed by a decimation, the Noble identity can be invoked to commute the filtering and the decimation, resulting in the structure shown in Fig. 6(d). Only one sub-band filter has been decomposed in the figure, even though all filters should be decomposed in any

practical implementation to allow for a lower processing rate. The combination of the filter banks, their respective polyphase decomposition, the multiplexer, and the lower rate DPLL is referred to as the PDPLL. As can be seen from Fig. 6, the PDPLL processes the samples at a significantly reduced rate (depending on M) while still being able to track a signal spanning the full input bandwidth (which is at most half the sampling rate).

When the signal frequency at the DFB input changes due to spacecraft acceleration or jerk, the signal could pass from one filter to the next. In this case, the output of the filter with a signal present in its passband is multiplexed and used to drive the DPLL. Formally, denote the total DFB bandwidth as Ω . Let $\Omega = [F_1, F_2]$ and let $I_i = [F_i^l, F_i^u]$ such that $\Omega = \bigcup_{i=0}^{M-1} I_i$ where the passband of the i th filter corresponds to the interval I_i . Furthermore, assume that a uniform filter bank is employed, i.e., $F_i^u - F_i^l = F_2 - F_1/M = \Delta F, \forall i$. Note that $I_0 = [F_1, F_1^u]$ and $I_{M-1} = [F_{M-1}^l, F_2]$. In order to properly select the output of the filter bank, let m denote the m th filter whose output is tuned to the received signal. By monitoring the estimated instantaneous frequency of the numerically controlled oscillator (NCO), the multiplexing control operation becomes simply that of selecting the appropriate filter within the bank where the signal lies. Denoting the instantaneous frequency \hat{f}_{IF} as the output from the NCO, the m th filter is found to be

$$m : \hat{f}_{IF} \in I_m \quad \text{and} \quad m \in [0, M-1] \quad (15)$$

The algorithm for selecting the proper filter is also shown in the flowchart of Fig. 7. The IF estimate, \hat{f}_{IF} , of the input signal is found by adding the output of the loop filter to the nominal frequency of the NCO, i.e., $\hat{f}_{IF} = f_{NCO} + \hat{f}$. The multiplexer position is then set to the m th filter in the DFB according to Eq. (15). The control logic can be added as shown in Fig. 6(d) to provide the control signal for the multiplexer. A more elaborate algorithm can be used to control the multiplexer by taking into account the states of the loop filter, which are related to the Doppler rate and its derivatives.

For the PDPLL application, the DFB's in Fig. 6(d) are required to have a constant group delay and continuous phase as a function of frequency. These requirements become critical when the incoming tone is likely to span more than one filter due to a time-varying Doppler characteristic. In this case, DFB's with a constant group delay and continuous phase would not introduce a phase jump to the DPLL input when the multiplexer selects a different filter

output. DFB's without these properties would introduce a phase jump that would cause the DPLL to temporarily lose lock.

In the following section, an example of five filter banks is considered, and simulations are performed to verify both the steady-state and the transient behavior of the PDPLL.

IV. Example of PDPLL and Simulation Results

The tracking and acquisition performance of the DPLL and the PDPLL is characterized by simulation. The DPLL simulation is based on the block diagram shown in Fig. 6(a), and PDPLL simulation is based on Fig. 6(d) with $M = 5$. The DFB's used in the simulation are described in the Appendix. The passband and center frequencies, normalized by the sampling rate, are summarized in Table A-1. The "cross-over frequency," the frequency at which the DFB output is selected to be from a different filter, is also shown in Table A-1. The multiplexing algorithm in the simulation is the same as that described in Section III.

The theoretical tracking variance of the DPLL [Eq. (8) in Section II] versus the tracking variance of the PDPLL obtained via simulation is shown in Fig. 8. The input to the DFB is a 10-KHz sine wave sampled at 40 kHz, the DFB output is decimated by 5 so that the input to the loop is a 2-kHz sine wave. Consequently, the loop was simulated to be in lock by operating the loop NCO at a frequency of 2 kHz. The loop bandwidth was kept constant at 100 Hz and the simulated loop SNR's of 10, 20, and 30 dB were obtained by generating noisy sine waves with P_c/N_0 values of 30, 40, and 50 dB, respectively. The simulations were performed for $100/B_L$ or 1 sec and are seen to agree very well with theory.

The remaining figures (Figs. 9, 10, and 11), which show the acquisition performance of the PDPLL and DPLL in the absence of noise, indicate that both loops have identical transient responses. In the results that follow, the curves for the PDPLL case are deliberately offset to differentiate them from the DPLL curves. Figure 9(a) depicts the transient phase error response to a 0.1-rad phase step when the input to the DFB is a 10-kHz sine wave. Clearly, both cases have the same transient response to a phase step. The next figure, Fig. 9(b), depicts the transient behavior when the frequency error is 10 Hz and the phase error is 0.1 rad. Here, the A/D output is a 10.010-kHz sine wave. Once again, the two cases are seen to be

identical. The acquisition performance when the input signal frequency is linearly changing at a rate of 200 Hz/sec is shown in Fig. 10(a). In this case, the initial signal frequency was set to 10.5 kHz and the simulation was run for 1.25 sec at a sampling rate of 40 kHz. From Table A-1, with the sampling rate of 40 KHz, it is seen that the signal passes from $G_3(z)$ to $G_4(z)$ during the simulation. Figure 10(b) shows the filter selected by the multiplexer versus the frequency of the incoming signal. As expected, the multiplexer selects $G_3(z)$ when the input signal frequency is lower than 10.625 kHz (the cross-over frequency), and it selects $G_4(z)$ when the signal frequency is higher than 10.625 kHz. Note from Fig. 10 that the loop does not lose lock when the multiplexer changes its output. That is, there are no transients in the phase error response at $t = 0.625$ sec, the time when the multiplexer changes its position.

The frequency and phase error responses when the input signal frequency is changing at a rate of 5145 Hz/sec² [as depicted in Fig. 11(a)] are shown in Figs. 11(b) and 11(c). In this case, the initial signal frequency was set to 10.425 kHz and the simulation was run for 1 sec. The frequency was kept constant for the first 0.5 sec of the simulation, after which it changed according to $(5145 \text{ Hz/sec}^2)(t - 0.5)^2/2$ [see Fig. 11(a)], where t is the actual simulation time. Hence, the signal frequency at the end of the simulation is the initial frequency 10.425 kHz plus $5145(0.5^2/2)$ or 11.068 kHz. Once again the signal crosses over from $G_3(z)$ to $G_4(z)$, and the multiplexer, as shown in Fig. 11(d), selects the proper filter output. The steady-state phase error in Fig. 11(c) for these dynamics and loop bandwidth matches the theoretical steady-state error of 0.235 rad [2].

V. Conclusion

It is concluded that the PDPLL provides a viable solution to fabricating low-cost wideband DPLL's. By employing multirate digital filters, it is possible to use a much lower processing rate than the sampling rate. Various input signals with different Doppler profiles were used to demonstrate the utility of the PDPLL. The simulation results indicate that the tracking and acquisition performance of the PDPLL is essentially equivalent to that of the conventional PLL. In order to establish the dynamic range of the tracking loop with the multirate DFB, the simulation was performed with a frequency ramp of 200 Hz/sec, and in the presence of very high dynamics, namely a jerk of 5145 Hz/sec². The steady-state phase error in each case agreed with the theoretically predicted steady-state phase error.

References

- [1] W. C. Lindsey and C. M. Chie, "A Survey of Digital Phase Locked Loops," *IEEE Proceeding*, vol. 69, no. 4, pp. 410–431, April 1981.
- [2] S. Aguire and W. Hurd, "Design and Performance of Sampled Data Loops for Carrier and Subcarrier Tracking," *TDA Progress Report 42-79*, vol. July–September 1984, pp. 81–85, Jet Propulsion Laboratory, Pasadena, California, November 15, 1984.
- [3] S. Aguire, "A Comparison of Methods for DPLL Loop Filter Design," *TDA Progress Report 42-87*, vol. July–September, 1986, pp. 114–124, Jet Propulsion Laboratory, Pasadena, California, August 15, 1986.
- [4] P. P. Vaidyanathan, "Multirate Digital Filters, Filter Banks, Polyphase Networks, and Applications," *IEEE Proceedings*, vol. 78, no. 1, pp. 56–93, January 1990.
- [5] R. E. Crochiere and L. R. Rabiner, *Multirate Digital Signal Processing*, Englewood Cliffs, New Jersey: Prentice Hall, 1986.
- [6] R. Sadr and M. Shahshahani, "On Sampling Band-Pass Signals," *TDA Progress Report 42-96*, vol. October–December 1988, pp. 14–20, Jet Propulsion Laboratory, Pasadena, California, February 15, 1985.

Table 1. Survey of high-speed signal processing hardware (December 1991).

Technology	Device	Speed	Company	Power, W
Acoustic charged transport	FIR	360 MHz	Electronic Design, Inc.	6
Bipolar GaAs	Arithmetic logic unit	250 MHz	Texas Instruments	1.5
Emitter-coupled logic (ECL)	316-NCO	1.4 GHz	Plessey	5
GaAs	10-bit digital-to-analog converter	1 GHz	ITT Avionics	5
Enhanced depletion mode GaAs	Logic gates	1 GHz	Harris	^a
ECL	8-bit analog-to-digital converter	500 MSPS ^b	Tektronics	5
Surface acoustic wave	Voltage-controlled oscillator (VCO)	100 MHz	Ericsson Fatme	1
High-electron mobility transistor	Logic gates at 77 K	40 GHz	(See footnote c)	-
GaAs	4 K × 4 RAM	200 MHz	Mitsubishi Electric	2
GaAs	ROM	650 MHz	Gigabit Logic	4
Heterojunction bipolar transistors	VCO-divider	12 GHz	TRW	-

^a 50 times less than ECL.

^b Millions of samples per second.

^c Six Japanese manufacturing companies, including Fujitsu and Mitsubishi, among others.

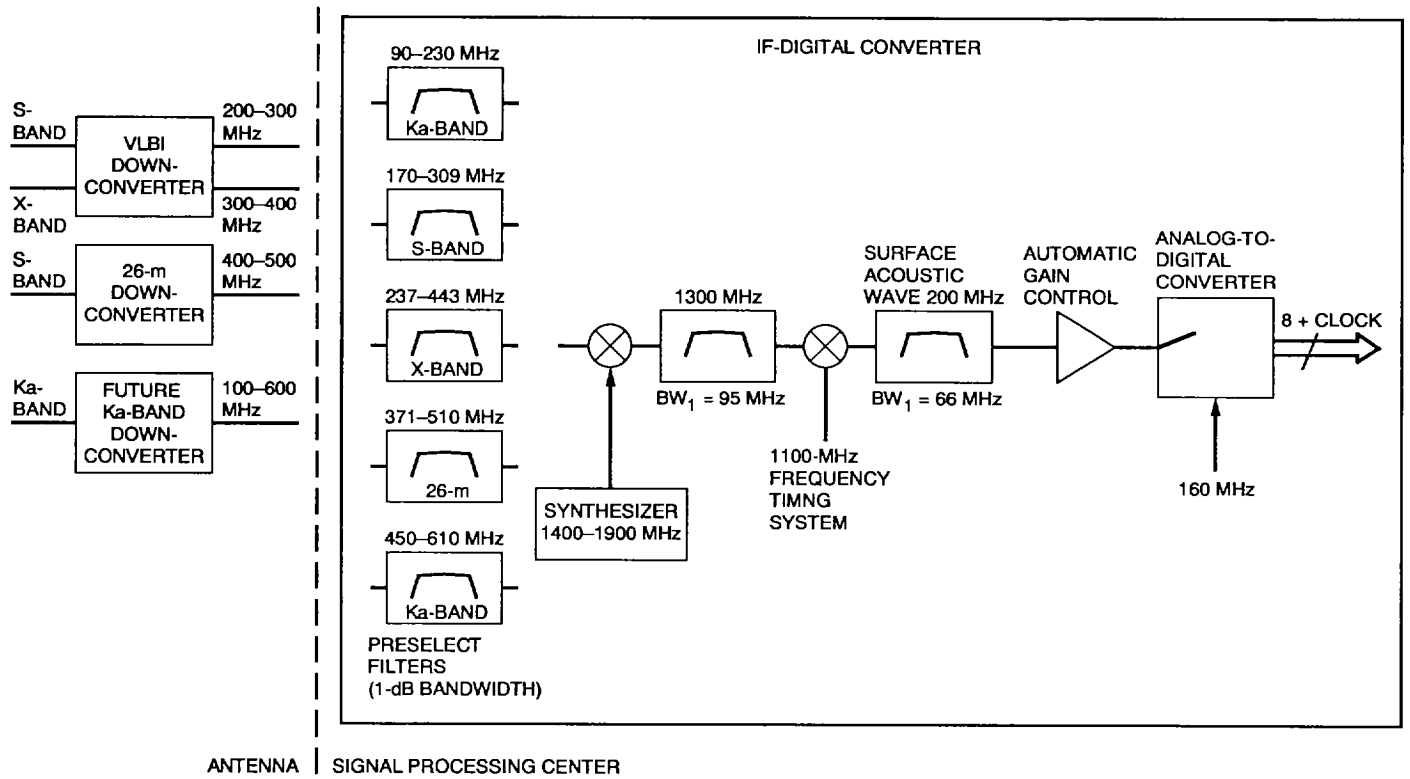


Fig 1. Block V receiver architecture.

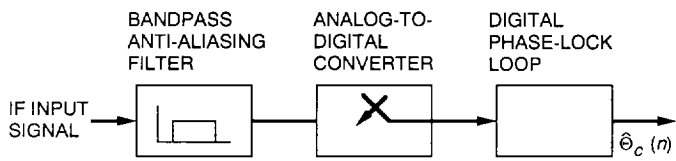


Fig. 2. Digital phase-lock loop preceded by an A/D converter.

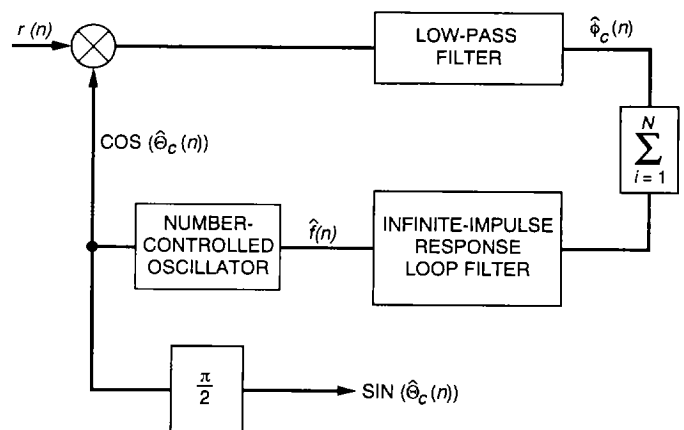


Fig. 3. DPLL block diagram.

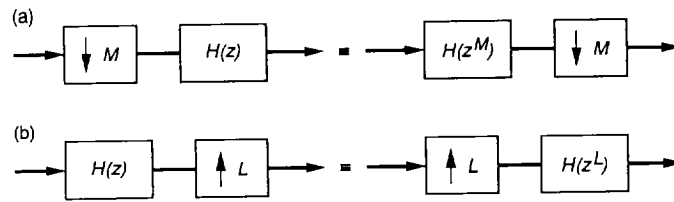


Fig. 4. Noble identity for multirate systems: (a) decimation and (b) interpolation.

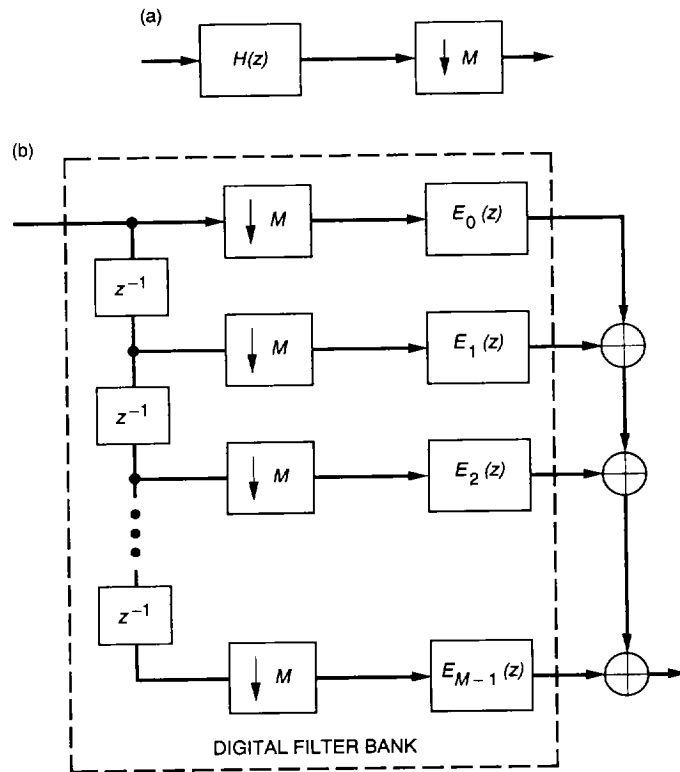


Fig. 5. Polyphase representation: (a) prototype filter and (b) blocked version.

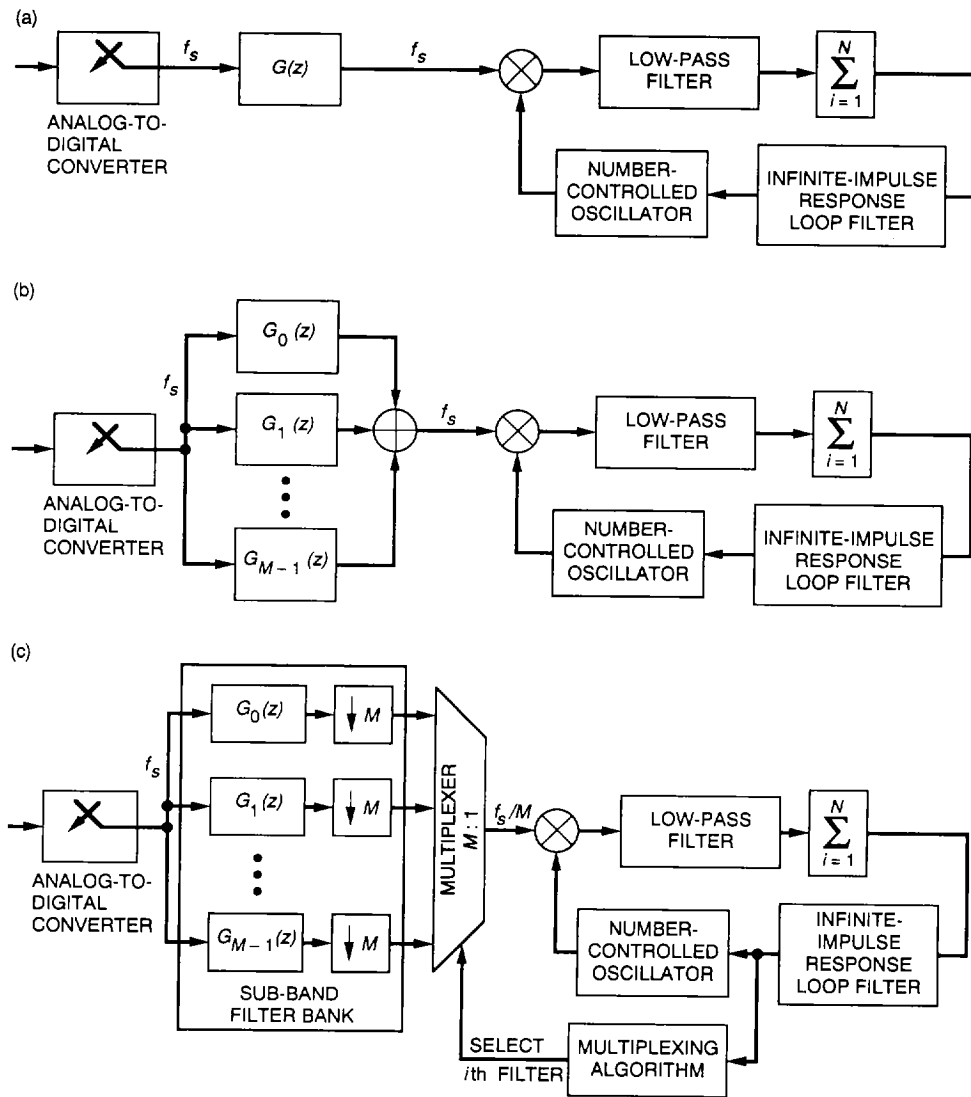


Fig. 6. Development of PDPLL: (a) bandpass filter insertion; (b) sub-band filter decompositions; (c) decimation; and (d) polyphase decomposition.

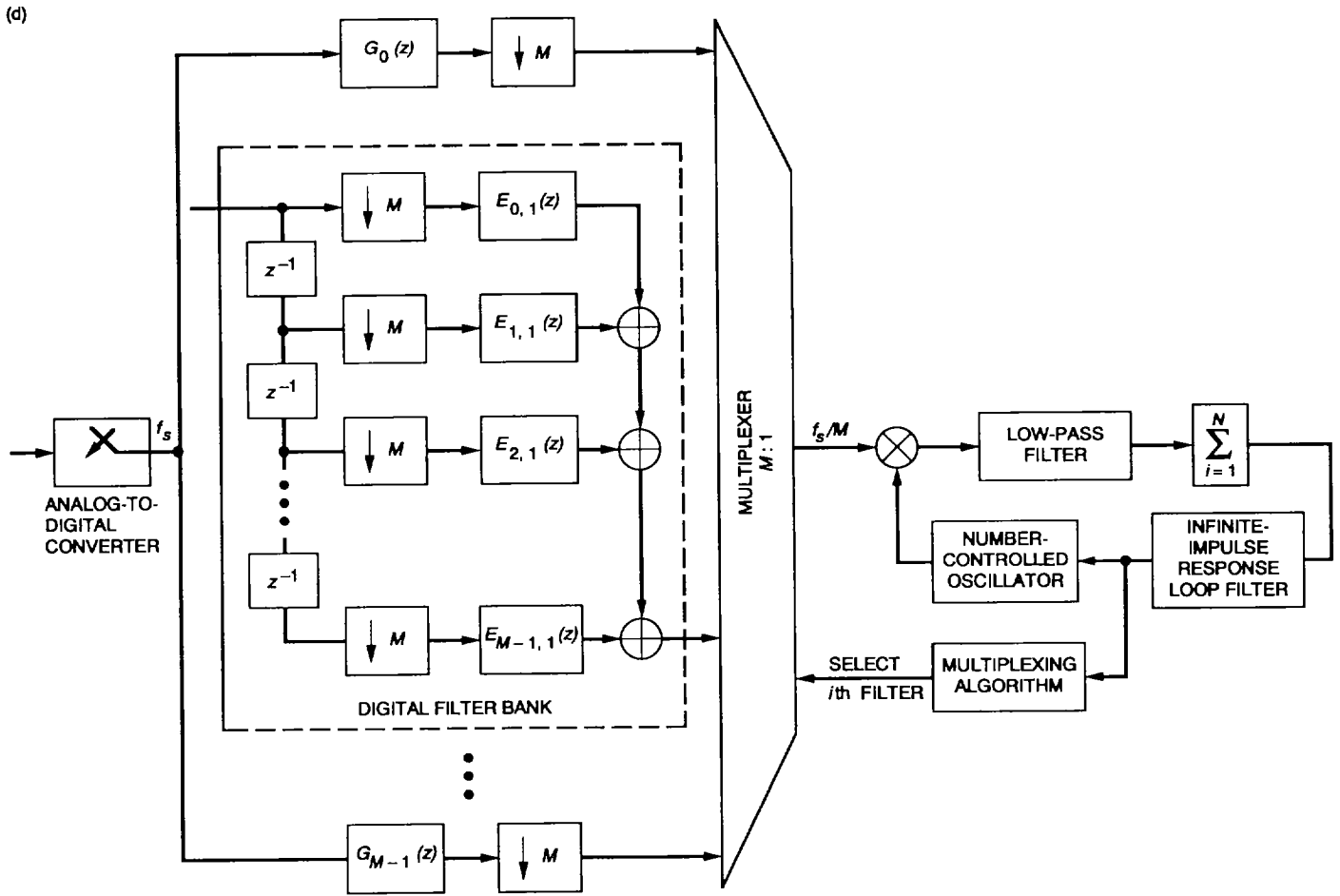
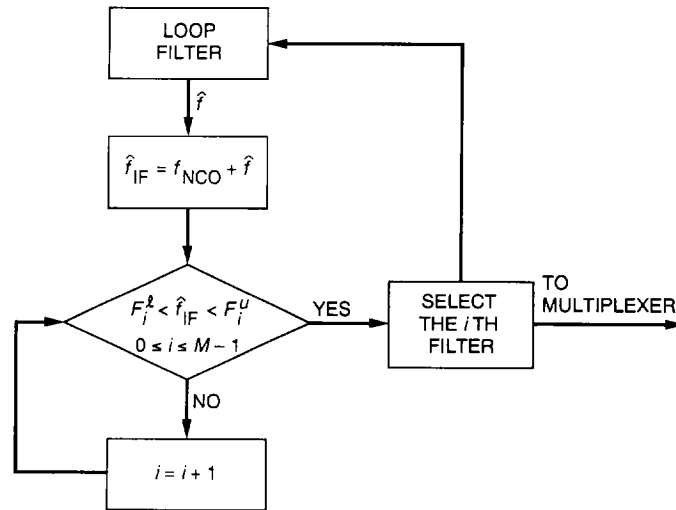


Fig. 6 (contd).



- \hat{f} DOPPLER FREQUENCY ESTIMATE
- f_{NCO} NUMBER-CONTROLLED OSCILLATOR FREE-RUNNING FREQUENCY
- \hat{f}_{IF} DIGITAL FILTER BANK INPUT FREQUENCY ESTIMATE
- F_i^L LOWER CUTOFF FREQUENCY, i TH FILTER
- F_i^U UPPER CUTOFF FREQUENCY, i TH FILTER

Fig. 7. Flowchart for the filter selection (multiplexing) algorithm.

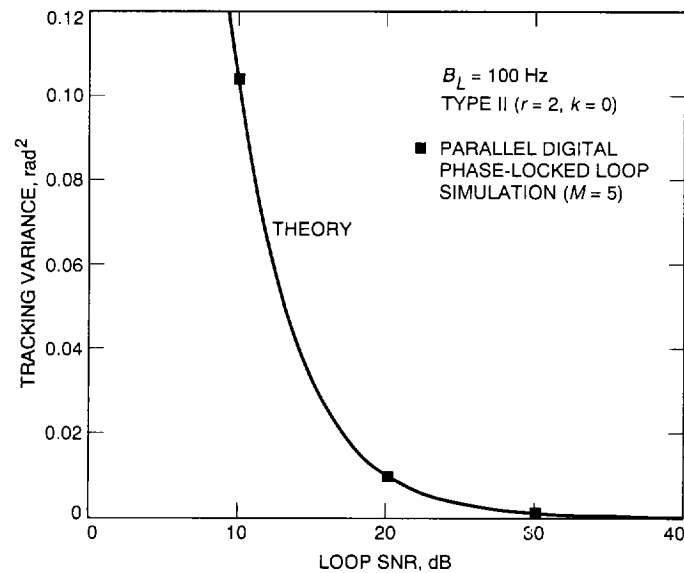


Fig. 8. The simulated tracking variance of the PDPLL ($M = 5$) and the theoretical tracking variance as a function of loop SNR.

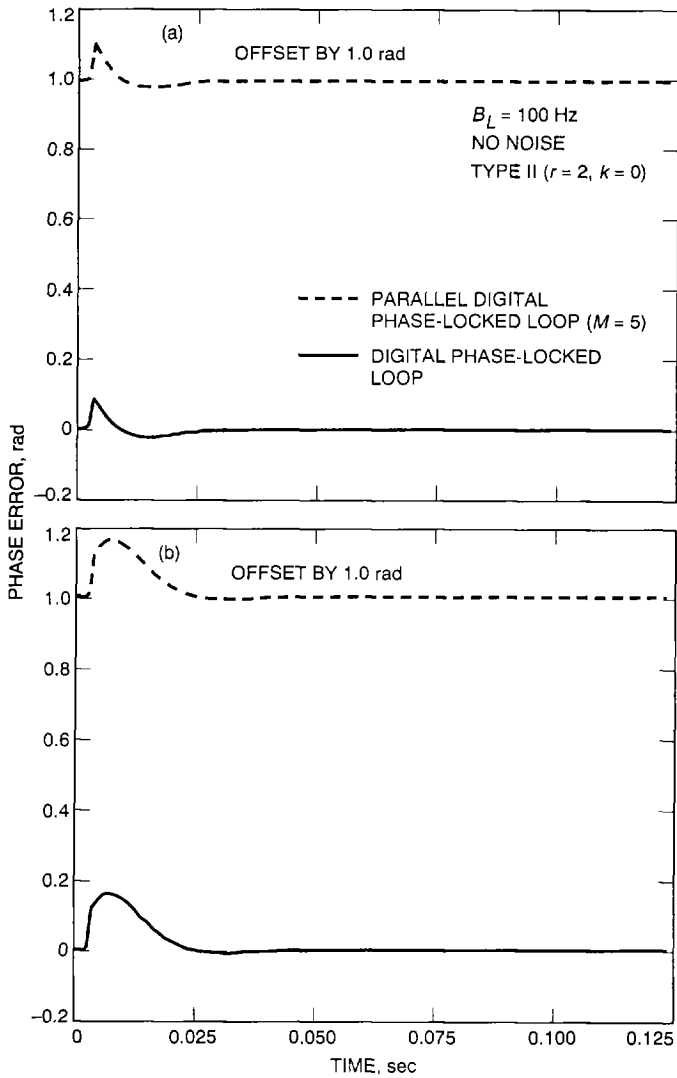


Fig. 9. The DPLL and PDPLL transient response to: (a) 0.1-rad phase step and (b) 10-Hz frequency offset plus a 0.1-rad phase step.

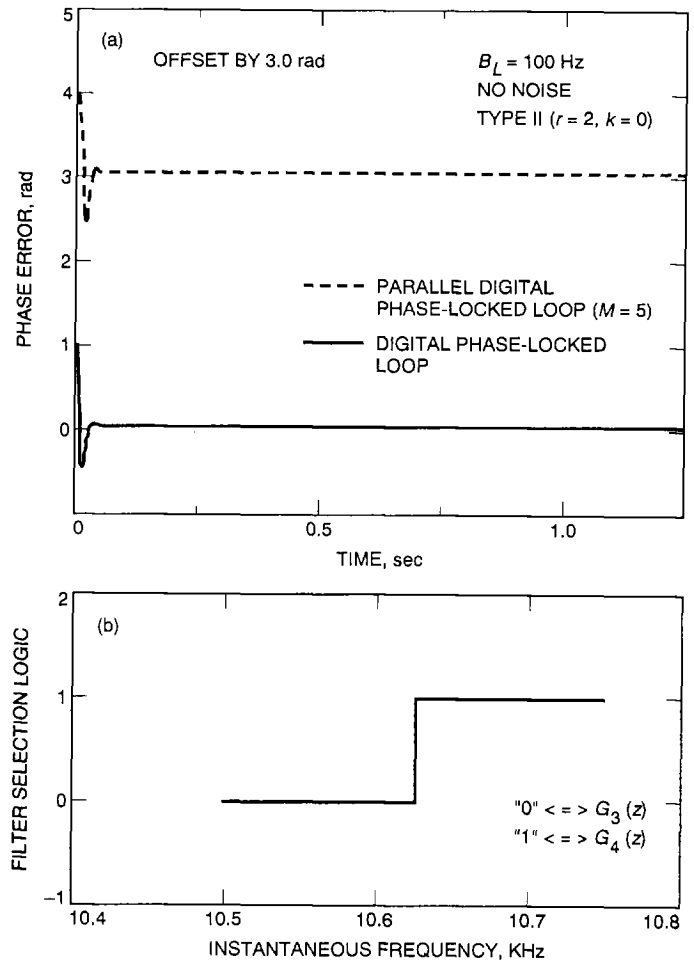


Fig. 10. PDPLL and DPLL simulation results for a 200-Hz/sec Doppler rate: (a) phase-error as a function of time and (b) multiplex control signal as a function of frequency.

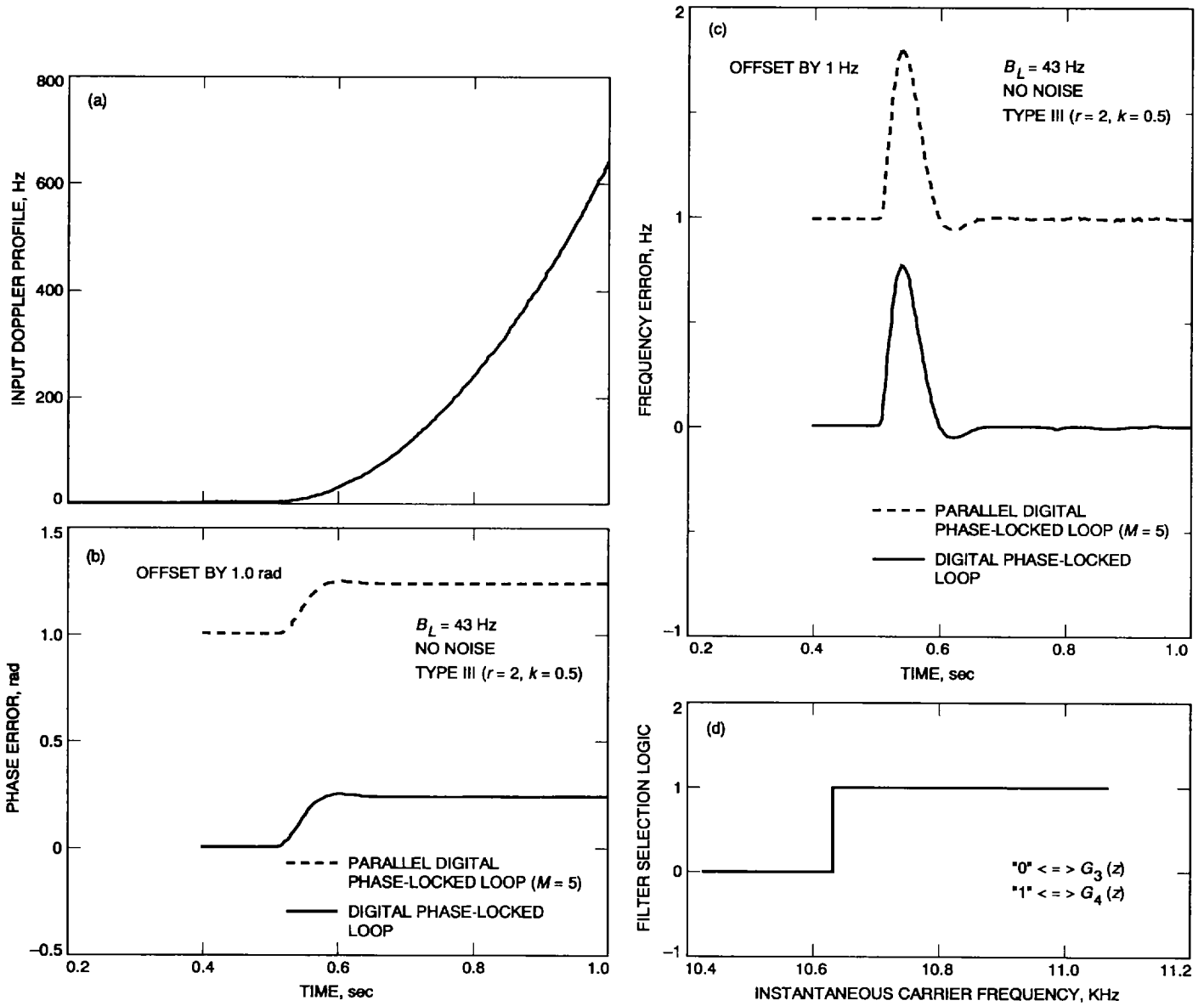


Fig. 11. PDPLL and DPLL simulation results for a jerk of 5145 Hz/sec²: (a) input Doppler profile versus time; (b) phase-error versus time; (c) frequency error versus time; and (d) multiplex control signal as a function of frequency.

Appendix

Typically, the bandpass filters in a uniform DFB are obtained by frequency shifting the response of a low-pass prototype filter. Suppose that the prototype filter is an $N+1$ tap low-pass finite impulse response (FIR) filter with a passband in the frequency interval $[0, \omega_p^u]$ rad, where the upper passband cut-off frequency, ω_p^u , is given as

$$\omega_p^u = \frac{2\pi F_p^u}{f_s} \quad (\text{A-1})$$

The parameters F_p^u and f_s are the analog cut-off frequency of the prototype filter and the sampling frequency, respectively, in hertz. The prototype filter transfer function, $H_p(\omega)$, is represented as

$$H_p(\omega) = |H_p(\omega)|e^{-j\omega N/2} \quad (\text{A-2})$$

where $|H_p(\omega)|$ is the magnitude response and $-\omega N/2$ is the phase response of $H_p(\omega)$. The i th filter of a uniform DFB is obtained by multiplying the prototype filter impulse response, $h_p(n)$, by $2 \cos(\omega_i n T_s)$. Hence, the transfer function of the i th filter is given as

$$G_i(\omega) = H_p(\omega - \omega_i) + H_p(\omega + \omega_i) \quad (\text{A-3})$$

The center frequency of the i th filter was chosen for simulation purposes according to

$$\omega_i = F_1 + \frac{\Delta F}{2} i \quad (\text{A-4})$$

where, using the same notation as in Section III, F_1 is the lower passband cutoff frequency of the DFB and ΔF is the length of the sub-bands.

As noted in the main text, the filters of the DFB should have continuous phase as a function of frequency. That is, the phase angle of $G_i(\omega)$ and $G_{i+1}(\omega)$ must be a multiple of 2π , i.e.,

$$\angle G_i(\omega) - \angle G_{i+1}(\omega) = 2k\pi \quad \forall \omega \in I_i \cap I_{i+1} \quad (\text{A-5})$$

Substituting for the angles in Eq. (A-5) yields

$$\frac{|\omega_{i+1} - \omega_i| N}{2} = 2k\pi, \quad \forall \omega \in I_i \cap I_{i+1} \quad (\text{A-6})$$

Using Eqs. (A-4) and (A-6), the following constraint must be satisfied when designing a phase continuous DFB

$$\frac{\Delta f N}{4} = 2k\pi \quad (\text{A-7})$$

The prototype filter, $H_p(\omega)$, used in the simulations is shown in Fig. A-1(a). The digital cut-off frequency for this filter, ω_p^u , is equal to 0.03125 rad, and the parameter N is 256. The DFB was arbitrarily chosen to have five filters, which are shown in Fig. A-1(b) and summarized in Table 2. These filters have continuous phase because their center frequency separation $(\omega_{i+1} + \omega_i)/2 = (0.03125)2\pi \times N/2 = 128$ satisfies the constraint expressed in Eq. (A-6). The frequency response of the polyphase components of $G_4(z)$ is shown in Fig. A-2. The polyphase decomposition was obtained by applying Eq. (14) with $M = 5$ to the transfer function of $G_4(z)$.

Table A-1. The normalized center frequency, passband, and crossover frequency of the simulated DFB's.

Filter	ω_i , rad	Passband, rad	Crossover frequency, rad
$G_0(z)$	0.1875	[0.15625, 0.21875)	0.203125
$G_1(z)$	0.21875	[0.18755, 0.25)	0.234375
$G_2(z)$	0.25	[0.21875, 0.28125)	0.265625
$G_3(z)$	0.28125	[0.25, 0.3125)	0.296875
$G_4(z)$	0.3125	[0.28125, 0.34375)	—

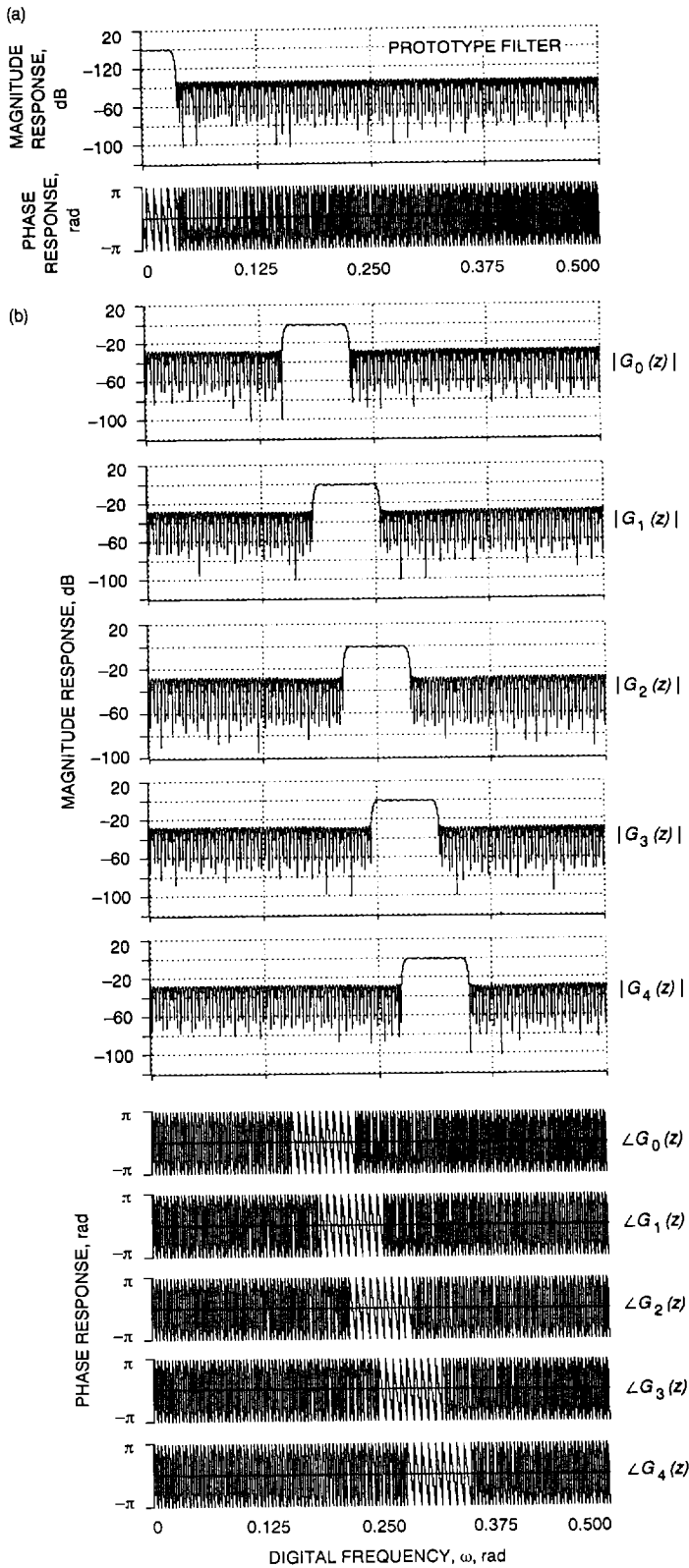


Fig. A-1. Magnitude and phase response as a function of the digital frequency for (a) the prototype filter and (b) the simulated DFB's.

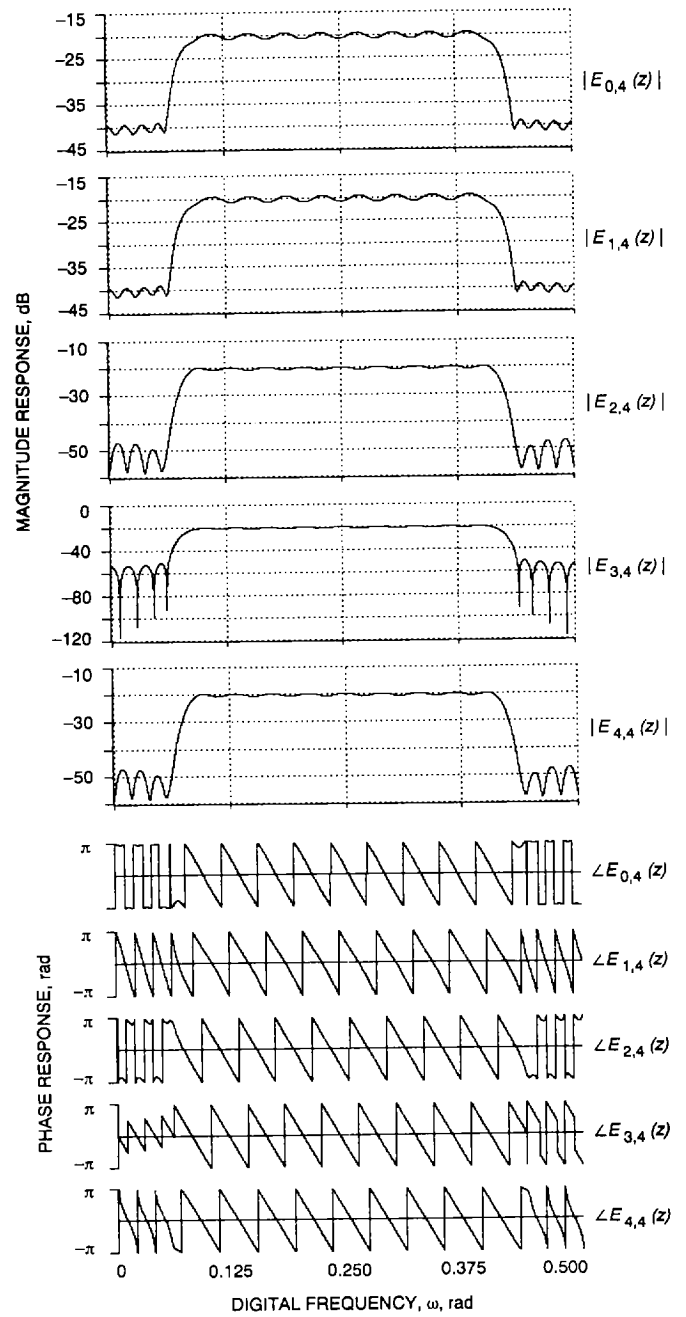


Fig. A-2. Magnitude and phase response of the polyphase components of $G_4(z)$.