Tracking Performance and Cycle Slipping in the All-Digital Symbol Synchronizer Loop of the Block V Receiver

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Computer simulated noise performance of the symbol synchronizer loop (SSL) in the Block V receiver is compared with the theoretical noise performance. Good agreement is seen at the higher loop SNR's (SNR_L*'s), with gradual degradation as the* SNR_L *is decreased. For the different cases simulated, cycle slipping is observed (within the simulation time of* 10^4 *seconds) at* SNR_L*'s below different thresholds, ranging from 6 to 8.5 dB, comparable to that of a classical phase-locked loop. An important point, however, is that to achieve the desired loop SNR above the seemingly low threshold to avoid cycle slipping, a large data-to-loop-noise power ratio,* $P_D/(N_0B_L)$*, is necessary (at least 13 dB larger than the desired* SNR_L *in the optimum case and larger otherwise). This is due to the large squaring loss (*$\geq$*13 dB) inherent in the SSL. For the special case of symbol rates approximately equaling the loop update rate, a more accurate equivalent model accounting for an extra loop update period delay (characteristic of the SSL phase detector design) is derived. This model results in a more accurate estimation of the noise-equivalent bandwidth of the loop.*

I. Introduction

In the Block V receiver, an estimate of the instantaneous symbol phase is generated by the symbol synchronizer loop (SSL). An accurate estimate of the instantaneous symbol phase is necessary for sum-and-dump accumulations over a symbol period of the data, which is done in various parts of the receiver, such as in the biphase-shift-keying (BPSK) and the quadriphase-shift-keying (QPSK) Costas loops, the subcarrier loop, and the symbol signal-to-noise ratio (SNR) estimator.

The Block V symbol synchronizer loop will be an *all-digital* implementation of the data-transition tracking loop (DTTL), which has been studied in depth [1,2,3]. *All-digital* is emphasized to indicate that the entire loop, including the phase detector, is implemented digitally, as opposed to the analog phase detection used in most references of the digital DTTL.

When the number of samples per symbol is large, the behavior of the all-digital loop implementation is expected to be comparable to the equivalent analog loop as long as the loop is updated fast enough; i.e., when the loop bandwidth-update time product, B_LT_u, is much less than one ($B_LT_u \ll 1$). Computer simulations were run to make the comparison of the digital versus analog loop noise per-

formance. Results presented in this article show the level of agreement between the simulation and the equivalent model assumed for analysis.

In Section II of this article, the SSL implementation is described and its noise-equivalent bandwidth is derived. The expected phase error variance of the loop[1] is cited in Section III and compared with the simulated values in Section IV. The normalized phase error is monitored to detect cycle slipping in the simulations. Results are discussed in Section V.

II. Analysis of the Digital SSL

In this section, the digital SSL implementation is described and the linear equivalent models are derived for two cases: (1) for loop update rates approximately equaling the symbol rates ($f_u \approx R_{sym}$) and (2) for loop update rates much less than the symbol rates ($f_u \ll R_{sym}$). From the equivalent models, the actual noise-equivalent bandwidths of the loops are calculated.

A. Description of the SSL

The digital SSL design is shown in Fig. 1. The input to the loop is assumed to be data plus noise sampled at $f_s = 1/T_s$ Hz

$$r(k) = Ad(k) + n(k)$$

$$= (Ad(t) + n(t))\,|_{t=kT_s}$$

$n(k)$'s are white, Gaussian noise samples with variance $N_0/(2T_s)$ where N_0 is the one-sided spectral density of the noise. The $d(k)$'s are samples of a non-return-to-zero (NRZ) random data of data rate $R_{sym} = 1/T_{sym}$ Hz and amplitude A, shown in Fig. 2(a). The loop's estimated end-of-bit (EOB) indicator signal (which goes low when the EOB is detected) with a timing error of τ seconds is sketched in Fig. 2(b) with respect to the true data stream in Fig. 2(a). Basically, the SSL drives τ to zero.

From Fig. 1, it can be seen that the SSL is a form of the classical phase-locked loop (PLL) with the difference in phase detection. The SSL phase detector (PD) estimates the timing error τ as $\hat{\tau}$ in seconds (instead of the phase error as in the classical PLL). The estimated timing error is then converted to the symbol phase error, $\hat{\phi}$, which is filtered and used to adjust the numerically controlled oscillator (NCO). Instead of feeding back phase as in a classical PLL, symbol timing is fed back to the PD. For timing feedback, the NCO phase output is converted to pertinent symbol timing signals which control the phase detector timing. The conversion is achieved in the timing logic.

1. SSL Phase Detector. The PD design is shown in Fig. 3. The mid-phase accumulation, $M(n)$, is the sum of samples across a window width W about the estimated symbol transition [3] [the accumulation interval is shown in Fig. 2(b)]; i.e., accumulation of samples from $(1 - W/2)$ of the first symbol through $(W/2)$ of the second symbol. (W is $2^{-\ell}$ for any integer $\ell = 0, 1, 2, \ldots$.) Defining d_j to be the jth symbol,

$$M(j) = \begin{cases} 2AN_s d_j \hat{\tau}/T_{sym} & \text{if a data transition is detected } (d_{j-1} \neq d_j) \\ AW d_j N_s & \text{if no data transition is detected } (d_{j-1} = d_j) \end{cases}$$

where $\hat{\tau}$ is the estimated timing error and the index j corresponds to time jT_{sym}. Due to the discrete nature of the accumulation, $\hat{\tau}$ is always quantized to an integer multiple of the sampling period; i.e., $\hat{\tau} = LT_s$, where L is an integer. However, the presence of noise makes the quantization effect negligible.

In-phase accumulation, $I(j)$, is the sum of samples over the estimated symbol period [the accumulation interval is shown in Fig. 2(b)]. For $\tau < T_{sym}/2$,

$$\text{sgn}(I(j)) = \text{sgn}(d_j) \tag{1}$$

where sgn(·) = signum function. Hence,

$$V(j) \triangleq M(j)\frac{[\text{sgn}(I(j)) - \text{sgn}(I(j-1))]}{2} \tag{2}$$

$$= \begin{cases} 2AN_s\hat{\tau}/T_{sym} & \text{if there is data transition} \\ 0 & \text{if there is no data transition} \end{cases}$$

In the presence of noise, the S-curve of the SSL has a slope K_g about the origin [1] (more details are given in Section III). In this case,

[1] M. K. Simon, personal communication, Telecommunications Systems Section, Jet Propulsion Laboratory, Pasadena, California.

$$V(j) = \begin{cases} 2AN_s K_g \hat{\tau}/T_{sym} & \text{if there is data transition} \\ 0 & \text{if there is no data transition} \end{cases} \quad (3)$$

The value $V(j)$ is accumulated over T_u seconds. Since $V(j)$ is updated at every detected EOB (which is at irregular intervals) and T_u is fixed, some asynchrony exists in the averaging process. The asynchrony is especially noticeable for symbol rates approximately equaling the loop update rate. Nevertheless, the averaged phase error estimate, $\bar{V}(m)$, is approximately

$$\bar{V}(m) \approx 2AN_s K_g M P_t \frac{\hat{\tau}}{T_{sym}} \quad (4)$$

where the time index m corresponds to time mT_u and

$$M = \frac{T_u}{T_{sym}}$$

$P_t = 1/2$ (probability of symbol transition in the data stream)

$K_g =$ Slope of the S-curve about the origin

The estimated timing error is then

$$\hat{\tau}(m) = \frac{\bar{V}(m)T_{sym}}{2AN_s K_g M P_t} \quad (5)$$

which is converted to a symbol phase error estimate as

$$\hat{\phi}(m) = 2\pi \frac{\hat{\tau}(m)}{T_{sym}} \quad (6)$$

2. Loop filter. The phase error $\hat{\phi}(m)$ is filtered in the loop filter (the same as for the standard DPLL loop filter [4,5] and is included for reference in Appendix A).

$$F(z) = \left[\alpha_1 + \alpha_2 \frac{z}{z-1} + \alpha_3 \frac{z^2}{(z-1)^2}\right] \quad (7)$$

and the loop filter output is $\Delta\omega(m)$.

3. NCO and the timing logic. The phase accumulation in the NCO is adjusted by $\Delta\omega(m)$ as

$$\hat{\theta}(k) = [G_{NCO}(\Delta\omega(k) + \omega_{init})T_s + \hat{\theta}(k-1)]_{\text{mod}G_{NCO}} \quad (8)$$

The value G_{NCO} is the NCO gain, and ω_{init} is the initial NCO frequency. Note that the NCO accumulates at the sample rate f_s Hz, a faster rate than the loop update rate, and the time index k corresponds to time kT_s.

From $\hat{\theta}(k)$, the timing logic block generates the EOB, the $(W/2)$-of-bit, and the $(1 - W/2)$-of-bit pulses, which are fed back to the PD (instead of phase, as in the classical PLL). The EOB is indicated at the time $\hat{\theta}(k)$ (before the modulo G_{NCO} operation) first equals or exceeds G_{NCO}. Similarly, $(W/2)$- and $(1 - W/2)$-of-bit are indicated when $\hat{\theta}(k)$ (before the modulo G_{NCO} operation) first equals or exceeds $(G_{NCO} \times W/2)$ and $(G_{NCO} \times (1 - W/2))$, respectively. Note that $\hat{\theta}(k)$ is also an estimate of the instantaneous symbol phase. The loop is closed as the EOB, the $(W/2)$- and $(1 - W/2)$-of-bit indicators are fed back to the in-phase and mid-phase accumulators in the phase detector.

B. Equivalent Linear Model of the SSL

A linear equivalent model of the loop is derived in this section. From the equivalent model, the noise-equivalent bandwidth of the loop, B_L^*, is estimated for calculation of the theoretical phase error variance. The derivation is made for two cases: (1) $f_u \approx R_{sym}$; and (2) $f_u \ll R_{sym}$.

1. Equivalent model for $f_u \approx R_{sym}$. For $f_u \approx R_{sym}$, an equivalent model can be derived at the symbol rate as shown in Fig. 4. The first delay models the fact that the estimated phase error at a given symbol transition is available at the PD output *after* a one-symbol period delay beyond the transition. This delay is characteristic of the SSL phase detector design (and, for example, not present in the residual carrier tracking PLL phase detector). This delay is significant when $f_u \approx R_{sym}$, and it is important that it be modeled for calculating B_L^*.

The second delay in Fig. 4 models the transport lag in the loop, and the third delay models the time delay prior to when the NCO output phase is corrected by the entire amount prescribed by the loop filter output.

The closed-loop transfer function of the model is

$$H(z) \triangleq \frac{\hat{\Theta}(z)}{\Theta(z)}$$

$$= \frac{z^{-3}F_{\theta_1}(z)}{(1 - z^{-1}) + z^{-3}F_{\theta_1}(z)} \quad (9)$$

where $F_{\theta_1}(z) = F(z)T_{sym}$. The loop filter transfer function $F(z)$ is as defined in Eq. (7).

2. Equivalent model for $f_u \ll R_{sym}$. For $f_u \ll R_{sym}$, an approximately equivalent model at the loop update rate f_u is shown in Fig. 5. The first delay approximates the delay between the PD output and the loop filter update corresponding to the accumulation time over the update period. Since in this case, several phase error estimates are accumulated over an update period, the one-symbol delay due to the phase detector is neglected. The second delay models the transport lag in the loop, and the third delay models the time delay prior to when the NCO output phase is corrected by the entire amount prescribed by the loop filter output. It should be noted that for $f_u \ll R_{sym}$, the total of three delays estimated in the equivalent model is conservative and results in an overestimated B_L^* in the linear region. The true number of delays in the loop is between 2.5 and 3. The approximate closed-loop transfer function of the loop for $f_u \ll R_{sym}$ is

$$H(z) \triangleq \frac{\hat{\Theta}(z)}{\Theta(z)}$$

$$= \frac{z^{-3}F_{\theta_2}(z)}{(1-z^{-1}) + z^{-3}F_{\theta_2}(z)} \qquad (10)$$

where $F_{\theta_2}(z) = F(z)T_u = F(z)/f_u$. The loop filter transfer function $F(z)$ is as defined in Eq. (7).

C. The Noise-Equivalent Loop Bandwidth, B_L^*, of the Digital SSL

Using the linear equivalent model, the actual noise-equivalent loop bandwidth of the loop is calculated from the closed-loop transfer function as [5]

$$B_L^* = \frac{1}{2T_u H^2(1)} I_n \qquad (11)$$

where

$$I_n \triangleq \frac{1}{2\pi j} \oint H(z)H(z^{-1})\frac{dz}{z}$$

The value I_n can be evaluated using methods described in [6,7].

For the parameters used in the simulations, B_L^* can be quite different from the loop bandwidth parameter, B_L, chosen for the loop.

III. Theoretical Noise Performance

The variance of the normalized phase error (λ) of the SSL was derived in [1,2] based on the assumption that the SSL is equivalent to an analog phase-locked loop (Fig. 6) when the symbol phase error is approximately constant over many symbols *and* when the loop response is much slower than a symbol period ($2B_L T_{sym} \ll 1$). The normalized phase error is defined as

$$\lambda \triangleq \frac{\tau - \hat{\tau}}{T_{sym}} \qquad (12)$$

in unitless fractional cycles, and where $\tau - \hat{\tau}$ is the time offset between the true and the estimated symbol times in seconds. For uncorrupted NRZ data input with additive white Gaussian noise (AWGN) of one-sided power spectral density N_0, and a high data to noise power ratio in the loop, $P_D/(N_0 B_L)$, the normalized phase error variance, σ_λ^2, in cycles squared, is[2]

$$\sigma_\lambda^2 \triangleq \mathrm{Var}[\lambda]$$

$$= \frac{h(0)WB_L}{2R_{sym}SNR_{sym}K_g^2[1-2B_L T_{sym}]} \qquad (13)$$

For comparison with the simulated all-digital SSL, the estimated noise-equivalent bandwidth, B_L^* [Eq. (11)], is used instead of the loop bandwidth parameter, B_L

$$\sigma_\lambda^2 = \frac{h(0)WB_L^*}{2R_{sym}SNR_{sym}K_g^2[1-2B_L^* T_{sym}]} \qquad (14)$$

where

$$R_{sym} = 1/T_{sym} \text{ (symbol rate)}$$

$$SNR_{sym} = A^2 T_{sym}/N_0 \text{ (symbol SNR)}$$

$$h(0) \triangleq S(0,0)/W(N_0 T_{sym}/4)$$

$$= 1 + \frac{W}{2}SNR_{sym} - \frac{W}{2}\left[\frac{1}{\sqrt{\pi}}e^{-SNR_{sym}} + \sqrt{SNR_{sym}}Erf\left[\sqrt{SNR_{sym}}\right]\right]^2$$

[2] Ibid.

W = Window width of the mid-phase accumulation in the PD

$S(0,0)$ = Spectral density of the equivalent additive noise $n_\lambda(t)$ at $\omega = 0,\ \lambda = 0$

$K_g \triangleq \frac{\partial g(\lambda)}{\partial \lambda}\,|_{\lambda=0}$ ($g(\lambda)$ is the normalized S-curve)

$= Erf[\sqrt{SNR_{sym}}]$

$-\frac{W}{2}\sqrt{SNR_{sym}/\pi}\ e^{-SNR_{sym}}$

B_L = loop bandwidth parameter

B_L^* = loop noise-equivalent bandwidth from Eq. (11)

The phase error variance in radians squared can be expressed as

$$\sigma_{\phi_e}^2 = (2\pi)^2\sigma_\lambda^2 \tag{15}$$

$$= (2\pi)^2 \frac{h(0)WB_L^*}{2R_{sym}SNR_{sym}K_g^2[1-2B_L^*T_{sym}]} \tag{16}$$

where $\phi_e \triangleq 2\pi(\tau-\hat{\tau})/T_{sym}$. The loop SNR, SNR_L, is defined as

$$SNR_L \triangleq \frac{1}{\sigma_{\phi_e^2}} \tag{17}$$

$$= S_L \frac{P_D}{N_0 B_L^*} \tag{18}$$

where

$$P_D = A^2 \ \text{(data power)}$$

$$S_L = \frac{2}{(2\pi)^2}\frac{K_g^2[1-2B_L^*T_{sym}]}{h(0)W} \ \text{(squaring loss)} \tag{19}$$

Note that the squaring loss S_L is less than $2/(2\pi)^2$ and approaches this value when $B_L^*T_{sym} \ll 1$, $W = 1$, and the symbol SNR is large [when $h(0)$ and K_g equal 1]. Hence, to achieve a given loop SNR of SNR_L', the data-to-loop noise power ratio must be

$$\frac{P_D}{N_0B_L^*} = SNR_L'S_L^{-1}$$

$$\geq SNR_L'\frac{(2\pi)^2}{2} \tag{20}$$

i.e., $P_D/(N_0B_L^*)$ must be at least 13 dB higher than the desired loop SNR. For low SNR_{sym}, e.g., -10 dB, S_L approaches $(2/\pi^3)(SNR_{sym}/W)$; then for $W = 1$, $P_D/(N_0B_L^*)$ must be at least [13 dB $-$ SNR_{sym}(dB)] higher than the required loop SNR.

IV. Simulation Results

For noise evaluation, the variance of the normalized phase error, $\hat{\sigma}_\lambda^2$, is measured via computer simulations and compared with the theoretical value of Eq. (14). Agreement between the two is expressed through the percentage error, $\Delta e\%$, defined as

$$\Delta e\% \triangleq \frac{\hat{\sigma}_\lambda^2 - \sigma_\lambda^2}{\sigma_\lambda^2} \times 100\% \tag{21}$$

Also, $\hat{\lambda}$, defined as the normalized difference between the true symbol phase and the NCO estimated symbol phase, $(\tau-\hat{\tau})/T_{sym}$, is monitored in the simulations to detect the occurrence of cycle slipping during the simulation.

All simulations were made for 10^4 seconds unless otherwise stated. Since the loop bandwidths ranged from 0.2 to 20 Hz, there were at least 2000 inverse loop bandwidths in each simulation, which is enough to identify the cycle-slipping threshold SNR_L. Simulations were made for the two cases, $f_u \approx R_{sym}$ and $f_u \ll R_{sym}$, for decreasing values of loop SNR's.

A. First Case: $f_u \approx R_{sym}$

For $f_u \approx R_{sym}$, simulations were made for the first- and the second-order loops with the asynchronous implementation where the loop is updated at a fixed period of T_u seconds. Simulations were made with both integer and noninteger number of samples per symbol. The parameters used in the simulations are

f_s = 10^5 Hz (sampling frequency)

R_{sym} = f_s/N_s (symbol rate)

N_s = number of samples per symbol

f_u = 1000 Hz

SNR_{sym} = $(A^2T_{sym})/N_0$ (symbol SNR)

B_L = loop bandwidth parameter in Hz

W = 1 (window width of the mid-phase accumulation)

For the first set of simulations, $SNR_{sym} = 5$ dB, and N_s was set to 100.0 and 100.001, which results in $R_{sym} \approx 1000$ Hz. Results are shown in Table 1.

The unreasonably large $\Delta e\%$'s are due to cycle slipping. This is confirmed by observation of $\hat{\lambda}(t)$. In Figs. 7(a) and (b), plots of $\hat{\lambda}(t)$ for $t = 0.9 \times 10^4$ seconds to 10^4 seconds of the simulations are shown for $N_s = 100.001$, and $B_L = 13$ Hz and $B_L = 17$ Hz, respectively. No cycle slipping is seen for $B_L = 13$ Hz, whereas cycle slipping is apparent for $B_L = 17$ Hz. It is seen that cycle slipping occurs at $SNR_L \approx 8.5$ dB and below. For SNR_L's above 8.5 dB, gradual degradation of $\Delta e\%$ is observed with the gradual decrease in SNR_L.

For the same parameters as above, additional simulation results for the second-order loop are shown in Table 2.

For the second-order loop, cycle slipping is observed at a higher loop SNR than that of the first-order loop, which is characteristic of a PLL. Plots of $\hat{\lambda}(t)$ for $N_s = 100.001$, and $B_L = 3$ Hz and $B_L = 15$ Hz, respectively, are shown in Figs. 8(a) and (b) where no cycle slipping is present for $B_L = 3$ Hz and cycle slipping is present for $B_L = 15$ Hz. Extensive simulations with gradually decreasing SNR_L's must be made to determine the actual cycle-slipping threshold for this case.

An additional set of simulation results for the first-order loop and the same parameters as above, but for a lower $SNR_{sym} = -1$ dB, is shown in Table 3.

B. Second Case: $f_u \ll R_{sym}$

For $f_u \ll R_{sym}$, cycle slipping was observed to start occurring at lower loop SNR's in the following simulations of the first-order loop. The parameters used in the simulations are

B_L = 3 Hz ($B_L^* = 4.08$ Hz)

f_s = 10^5 Hz

R_{sym} = f_s/N_s

N_s = 100.001 (number of samples per symbol)

f_u = 100 Hz

W = 1 (window width of the mid-phase accumulation)

and decreasing values of SNR_{sym}'s. Results are summarized in Table 4.

Cycle slipping is seen to start at an SNR_L between 6.0 and 6.8 dB. Note, however, that even though this minimum required loop SNR is small, squaring loss is large for these parameters and a $P_D/(N_0B_L^*)$ greater than 22.4 dB is necessary to achieve the minimum loop SNR to avoid cycle slipping. Extensive simulations with gradually decreasing SNR_L's must be made to determine the exact cycle-slipping threshold for this case.

To check the agreement between σ_λ^2 and $\hat{\sigma}_\lambda^2$ in the absence of cycle slipping, "quick" simulations (of simulation time = 30 seconds) were run for decreasing SNR_L for the following parameters. Results are shown in Table 5.

f_s = 10^5 Hz

R_{sym} = f_s/N_s

R_u = 50 Hz

N_s = 100.0 (number of samples per symbol)

SNR_{sym} = 5 dB

The difference $\Delta e\%$ is seen to grow as SNR_L is decreased. The very large negative values just show the invalidity of the equivalent model when B_LT_u is large (note that $B_LT_u = 0.1$ at this point).

V. Discussion of the Simulation Results

From the simulation results, it can be seen that $\Delta e\%$ increases with the decrease in the SNR_L until a loop SNR threshold is reached below which cycle slipping occurs (within the simulation time of 10^4 seconds). Cycle slipping is confirmed from the observation of $\hat{\lambda}(t)$, as shown in Figs. 7 and 8. The cycle-slipping threshold SNR_L varies for different cases. For $f_u \approx R_{sym}$, in a first-order loop, the cycle-slipping loop SNR threshold is approximately 8.5 dB; for the second-order loop, the threshold is higher, above 9.3 dB. For $f_u \ll R_{sym}$, the cycle-slipping threshold in the first-order loop is seen to

be between 6.0 and 6.8 dB; further simulations need to be executed to find a more accurate threshold. Additional simulations are also necessary to study the different cycle-slipping thresholds. In all cases, the cycle-slipping threshold loop SNR's are reasonably small. However, the difference in the SSL is that to achieve the small minimum SNR_L, a large $P_D/(N_0B_L^*)$ which is at least 13 dB higher than the desired SNR_L is necessary; a larger $P_D/(N_0B_L^*)$ is required when the symbol SNR is smaller. For example, to achieve the minimum required 8.5 dB for $f_u \approx R_{sym}$, $SNR_{sym} = 5$ dB in the first-order loop, $P_D/(N_0B_L^*) > 22$ dB is required. Similarly, to achieve the minimum required loop SNR (which is around 6 dB) in the simulations of $f_u \ll R_{sym}$, $SNR_{sym} = -1.5$ dB in the first-order loop, $P_D/(N_0B_L^*) > 22.4$ dB is required. This is due to the large squaring loss that exists in the SSL [Eq. (19)].

Prior to the loop breakdown due to cycle slipping, gradually increasing $\Delta e\%$ between the model and the simulated variances was observed for decreasing SNR_L. (Note that in the simulations, SNR_L was decreased by increasing B_L at a fixed symbol SNR, or by decreasing the symbol SNR at a fixed loop bandwidth.) One possible cause may be the self-noise due to the randomness that exists within the loop; i.e., the random phase detector output of 0 or $\hat{\phi}$ with transition probability P_t. In the simulations, the randomness in the phase detector output is compensated for by dividing the PD output by P_t, assuming then that the expected value of the PD output is $P_t\hat{\phi}$ and the expected value after the compensation is $\hat{\phi}$. In reality, the averaged value varies about $\hat{\phi}$ from one update time to another. This variation can cause additional variations in the NCO phase values which are used to estimate $\hat{\sigma}_\lambda^2$. As B_L is increased, variations are increased resulting in a larger additional variance.

For $f_u \approx R_{sym}$, another contribution to the increasing $\Delta e\%$ may be the nature of the PD design which detects the phase error after one symbol period delay, adding one delay to the equivalent digital loop (Fig. 4). As the number of transport delays in a digital PLL is increased, the equivalence between the digital and its equivalent analog loops collapses for smaller values of B_LT_u.

VI. Conclusion

The all-digital SSL design was computer simulated and the performance was compared with the theoretical model performance. Results show good agreement for higher loop SNR's, and gradual degradation in the agreement as SNR_L was decreased. Eventually, cycle slipping starts to occur (within the simulation time of 10^4 seconds) at SNR_L's below the cycle-slipping threshold. The cycle slipping thresholds appear to be comparable to that of the classical PLL. However, a very large $P_D/(N_0B_L^*)$ is necessary to achieve the seemingly small required minimum loop SNR, due to the large squaring loss that is inherent in the SSL.

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Table 1. Percentage error Δe % in a first-order SSL for $f_u \approx R_{sym}$, SNR_{sym} = 5 dB, increasing B_L.

B_L, Hz	B_L^*, Hz	$B_L T_u$	$P_D/\left(N_0 B_L^*\right)$, dB	SNR_L, dB	$N_s = 100.0$, Δe%, percent	$N_s = 100.001$, Δe%, percent
0.2	0.2004	0.0002	42	28.7	2.18	–
0.7	0.704	0.0007	36.5	23.3	2.49	–
1.5	1.52	0.0015	33.2	19.9	3.08	–
3	3.09	0.003	30.1	16.8	4.5	2.19
5	5.26	0.005	27.8	14.5	6.2	–
7	7.5	0.007	26.2	13.8	8.9	3.32
8	8.67	0.008	25.6	12.3	–	3.68
9	9.85	0.009	25.1	11.8	9.21	–
10	11.06	0.01	24.6	11.2	9.95	4.5
13	14.8	0.013	23.3	9.9	–	5.7
14	16.1	0.014	22.9	9.6	–	6.2
15	17.4	0.015	22.6	9.2	13.7	6.7
16	18.8	0.016	22.3	8.7	14.35	7.15
17	20.2	0.017	22.0	8.5	14.7	962
18	21.59	0.018	21.7	8.2	1.5×10^4	–
20	24.48	0.02	21.1	7.7	2×10^5	1790

Table 2. Percentage error Δe % in a second-order SSL for $f_u \approx R_{sym}$, SNR_{sym} = 5 dB, increasing B_L.

B_L, Hz	B_L^*, Hz	$B_L T_u$	$P_D/\left(N_0 B_L^*\right)$, dB	SNR_L, dB	$N_s = 100.0$, Δe%, percent	$N_s = 100.001$, Δe%, percent
3	3.07	0.003	30.1	16.9	–	3.4
10	10.85	0.01	24.6	11.1	9.9	–
15	16.99	0.015	22.7	9.3	290	3300
16	18.27	0.016	22.4	9.0	–	8600

Table 3. Percentage error Δe % in a first-order SSL for $f_u \approx R_{sym}$, SNR_{sym} = 1 dB, increasing B_L.

B_L, Hz	B_L^*, Hz	$B_L T_u$	$P_D/(N_0 B_L^*)$, dB	SNR_L, dB	$N_s = 100.001$, Δe%, percent
2	2.04	0.002	26	9.9	15.8
3	3.09	0.003	24.1	8.0	Cycle slipping occurs
3.5	3.62	0.0035	23.4	7.3	Cycle slipping occurs
4	4.16	0.004	22.8	6.7	Cycle slipping occurs

Table 4. Percentage error Δe % in a first-order SSL for $f_u \ll R_{sym}$, decreasing SNR_{sym}.

SNR_{sym}, dB	$P_D/(N_0 B_L^*)$, dB	SNR_L, dB	Δe %, percent	Comments
3	26.9	13.1	−5.6	No cycle slipping
0	23.9	8.5	1.97	No cycle slipping
−0.9	23	7	7.8	No cycle slipping
−1	22.9	6.8	8.4	No cycle slipping
−1.5	22.4	6.0	–	Cycle slipping occurs
−2.0	21.9	5.1	–	Cycle slipping occurs
−2.53	21.4	4.1	–	Cycle slipping occurs

Table 5. Percentage error Δe % in first-order SSL for $f_u \ll R_{sym}$ for a short simulation time = 30 seconds, SNR_{sym} = 5 dB, increasing B_L.

B_L, Hz	B_L^*, Hz	$P_D/(N_0 B_L^*)$, dB	SNR_L, dB	σ_λ^2 (cycles)^2	$\hat{\sigma}^2$ (cycle.	Δe%, percent
1.5	2.04	32	18.7	3.4448×10^{-4}	3.4753×10^{-4}	0.88
2.0	3.03	30.2	16.9	5.128×10^{-4}	5.02×10^{-4}	−2.1
2.5	4.24	28.7	15.5	7.198×10^{-4}	6.89×10^{-4}	−4.3
3.0	5.7	27.4	14.1	9.772×10^{-4}	9.22×10^{-4}	−5.6
5.0	17.6	22.5	9.2	3.07×10^{-3}	2.23774×10^{-3}	−27

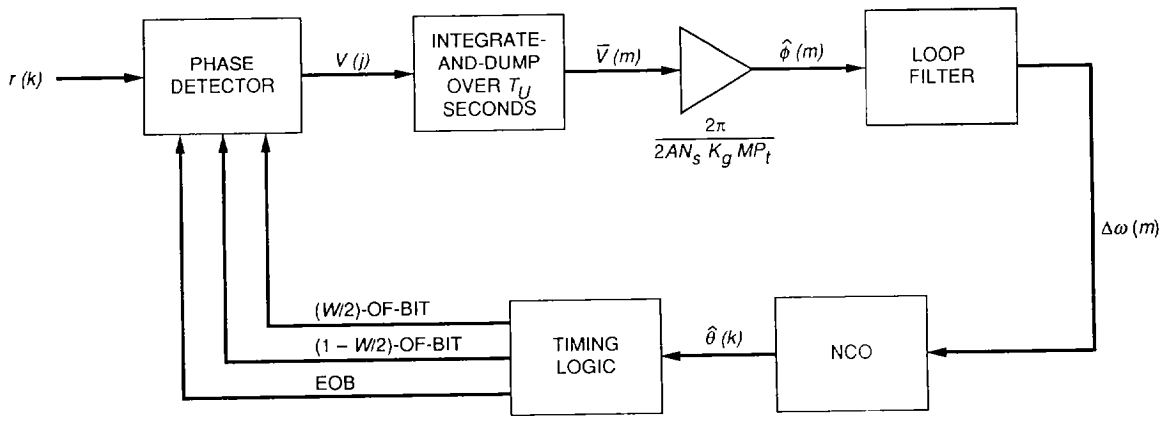

Fig. 1. The Block V digital symbol synchronizer loop.

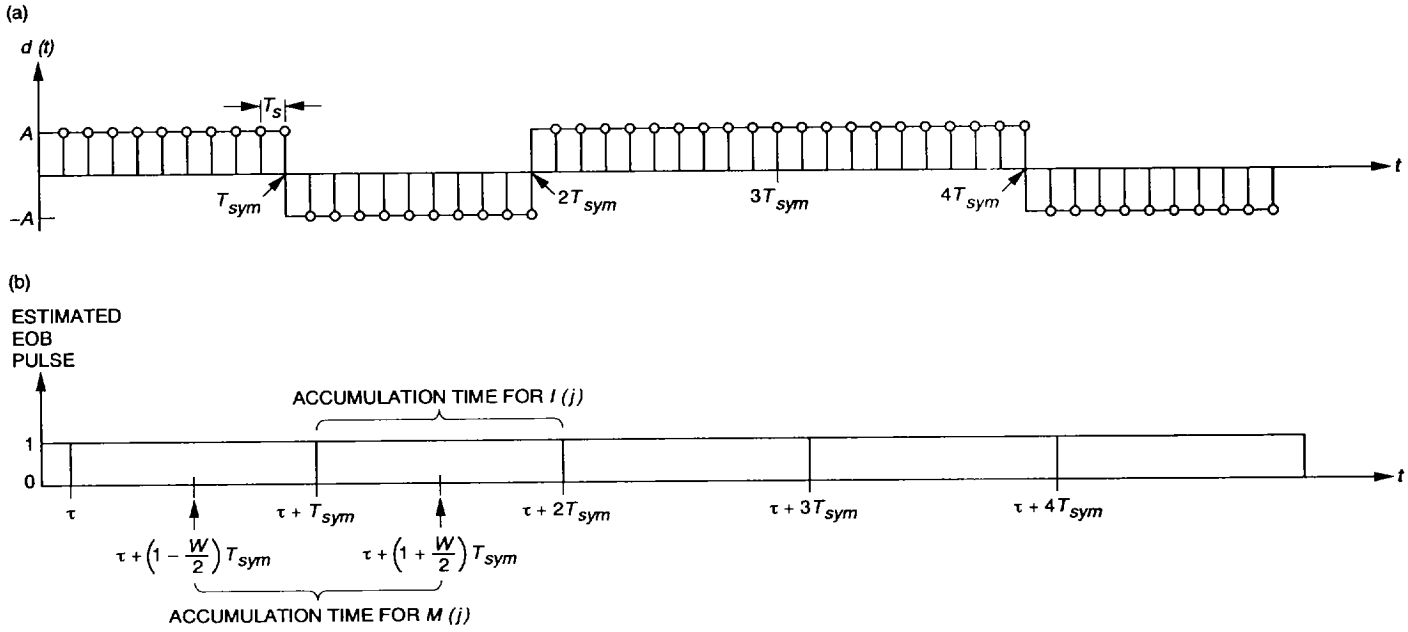

Fig. 2. input data stream and loop estimate of the EOB-time: (a) input data to the SSL and (b) estimated EOB timing with an error of τ seconds. Also shown are integration times for the in-phase and mid-phase integrations.

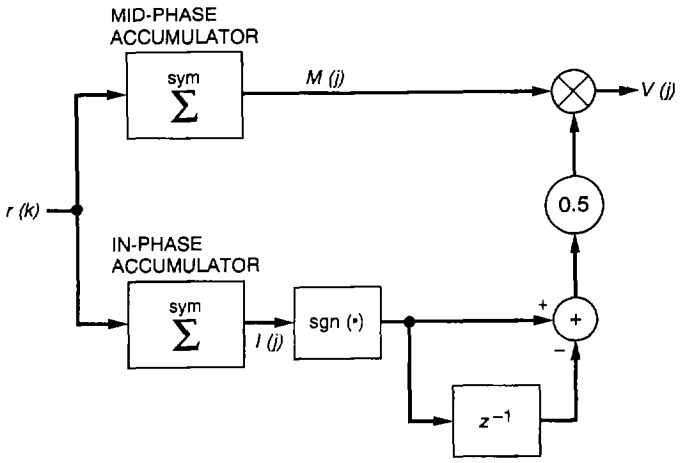

Fig. 3. The SSL phase detector design.

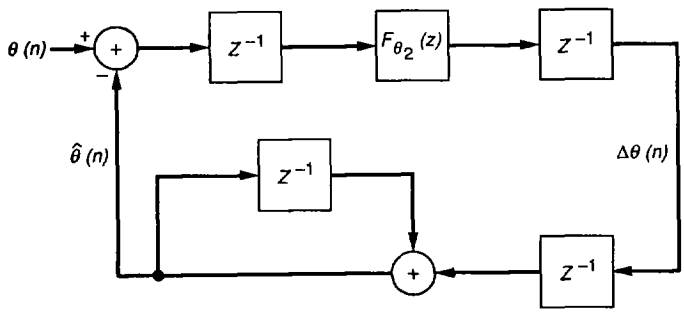

Fig. 5. An approximately equivalent digital PLL of the SSL for $f_u << R_{sym}$.

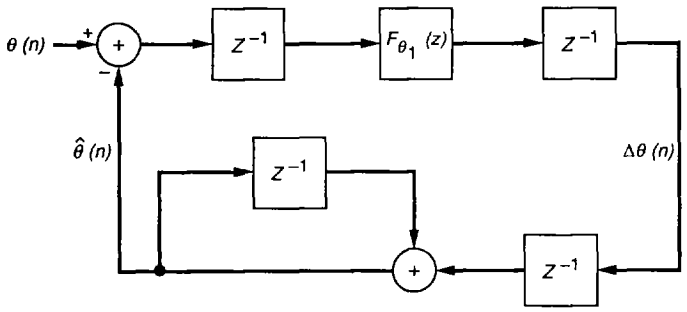

Fig. 4. Equivalent digital PLL of the SSL for $f_u \approx R_{sym}$.

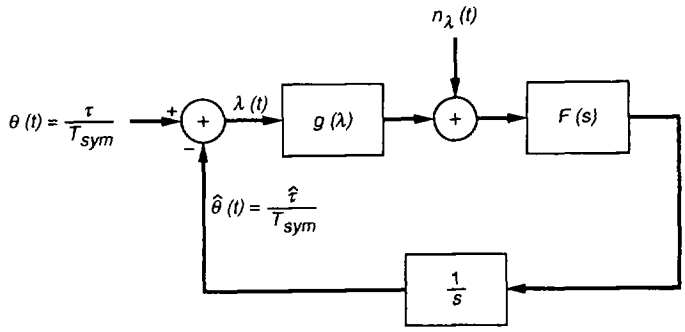

Fig. 6. Equivalent analog PLL of the SSL [1].

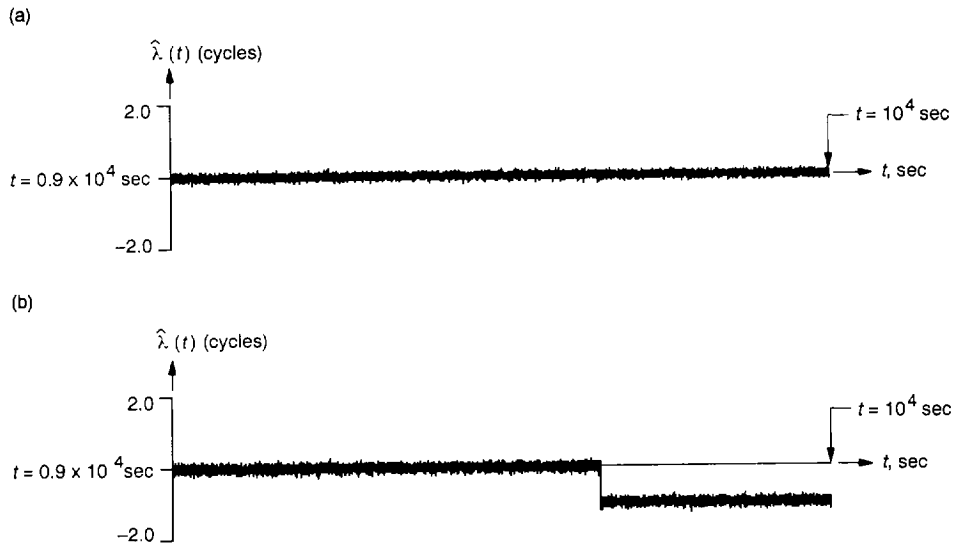

Fig. 7. $\hat{\lambda}(t)$ **for a first-order SSL,** $R_{sym} \approx f_U$**: (a)** SNR_L **= 9.9 dB and** $B_L T_u = 0.013$ **and (b)** SNR_L **= 8.5 dB and** $B_L T_u = 0.017$.

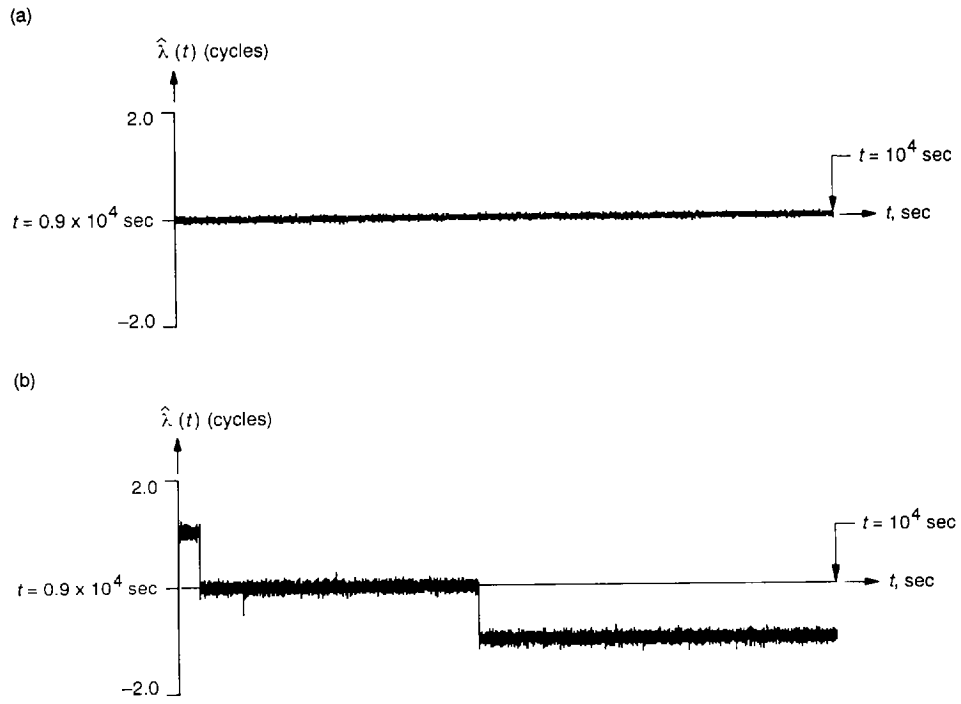

Fig. 8. $\hat{\lambda}(t)$ **for a second-order SSL,** $R_{sym} \approx f_U$**: (a)** SNR_L **= 16.9 dB and** $B_L T_u = 0.003$ **and (b)** SNR_L **= 9.3 dB and** $B_L T_u = 0.015$.