A 32-GHz Phased Array Transmit Feed for Spacecraft Telecommunications

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A 21-element phased array transmit feed has been demonstrated as part of an effort to develop and evaluate state-of-the-art transmitter and receiver components at 32 and 34 GHz for future deep-space missions. Antenna pattern measurements demonstrating electronic beam steering of the two-dimensional array are reported and compared with predictions based on measured performance of MMIC-based phase shifter and amplifier modules and Vivaldi slotline radiating elements.

I. Introduction

The DSN is implementing telecommunication capability at 32 GHz (Ka-band) with expected improvement of as much as 8 dB over the current capability at 8 GHz (X-band). In preparation for this new capability on the ground, a proof-of-concept 32-GHz phased array transmitter to feed a near-field dual-reflector system has been designed and implemented for future space application. The work described herein builds on the earlier design of a smaller active linear array [1] and a passive two-dimensional array [2,3].

The objective was to demonstrate useful RF power (1 to 10 W) and end-to-end efficiency (15 to 30 percent) at 32 GHz through array combining of low-power devices. One benefit of array combining of solid-state devices is improved reliability through graceful degradation of the RF output if individual devices fail. In addition to solid-state amplification, vernier electronic beam-steering capability (±10 deg) was also a goal with potential relief to pointing required of the spacecraft attitude control system.

The array development to be described has provided practical hands-on experience in the incorporation of monolithic microwave integrated circuits (MMIC) into arrays, mechanical and electronic system integration, and electronic beam-steering calibration and test. The completed hardware from this effort is currently used as a testbed for evaluating more efficient active devices, antenna elements, and signal distribution circuits as they are developed. Future microspacecraft missions to asteroids and the outer planets are the missions most likely to benefit from the Ka-band technology being demonstrated through this work.

II. Subsystem Design

The transmit phased array was designed to feed a spacecraft's dual-reflector antenna typically from the Cassegrain feed point. In this configuration, limited scan capability is traded for higher system gain. The feed, capable of ±10-deg scanning, would provide ±1-deg scanning in a system with a magnification factor of 10 [3]. The pointing resolu-

tion of the feed is also reduced by a factor of 10, suitable for satisfying pointing requirements on the order of hundredths of a degree.

The array consists of 21 active antenna elements fed by a beam-forming network. A modular architecture was selected to facilitate testing and substitution of individual components. Five linear subarray layers comprise the full two-dimensional array. The middle three layers contain five elements each and the outer two layers contain only three. Each subarray slides horizontally into an aluminum structure, providing support and alignment, and then plugs into a vertical RF signal distribution strip at the back of the structure (Fig. 1). Each subarray layer is divided into four modules: an input power divider, a phase shifter module, an amplifier module, and an antenna module. A photograph of a five-element subarray layer is shown in Fig. 2. Each path of a module is tested before integration into the subarray layer, and each subarray layer can be tested before integration into the full array.

III. Array Performance

The array was measured on a 7-m indoor antenna range capable of operation over the 26.5- to 40-GHz band. Amplitude and phase of the received signal were measured in a calibration sequence that steps through the 4-bit phase shifters' 16 states for each of the 21 elements. Figure 3 shows a typical calibration measurement giving the measured phase and amplitude in the far field. These data are contained in the lookup table used to set the beam-steered position of the array. In order to improve pattern measurements, paths with higher gain were attenuated, which provided a more uniform array aperture. The amplitudes for 17 elements vary within ± 3 dB, 3 of the elements have amplitudes ~ 5 dB lower, and 2 of the elements were not operating due to device failures during preliminary testing on the antenna range.

A. Antenna Patterns

Three-dimensional antenna patterns for the array are measured by sweeping in 1-deg increments in azimuth and then rotating in 10-deg increments, as indicated in Fig. 4(a). The result is that each azimuth cut measures a 10-deg sector of the azimuth–elevation plane in the contour plots that appear in Fig. 4(b) and (c). The half-power beamwidth is 9 deg, and the peak side-lobe level measured -13 dB pointing boresight. When steered off boresight by 10 deg, the scan loss is -1.5 dB and the peak side-lobe level is -10 dB.

The measured and modeled E- and H-plane patterns for a boresight beam and the principal cuts for beams scanned in the E- and H-planes are shown in Fig. 5. The 3-dB beamwidth is 9 deg for the boresight and scanned beams. The peak side-lobe level is -13 dB for the boresight and -10 dB for the scanned beams. The measured patterns are compared with a model that assumes an element pattern with a $(\cos\theta)^{10}$ variation for the main beam shape and a constant -15.7-dB side-lobe level. In addition, the modeled patterns include the actual phase and amplitude measured for each element. Differences between the measured and modeled patterns are a result of using a simplified element pattern and not including mutual coupling between elements in the model.

B. Gain and Efficiency

The gain of the 21-element array was predicted to be 26.7 dB. This was scaled from the measured gain of 22 dB for the best five-element linear subarray. The actual gain of the 21-element array was measured to be 25.6 dB where 2 of the elements had failed, 6 of the elements were 4 to 7 dB lower in gain than expected, and 10 elements were 1 dB higher than expected because they were not operating in compression.

The power-added efficiency (PAE) for the array, defined as

$$PAE = \frac{RF_{\text{power out}} - RF_{\text{power in}}}{DC_{\text{power in}}}$$

is predicted to be 8.7 percent based on measured RF output power for the best five-element tray. Efficiency will increase to 16 percent with a reduction in extraneous circuit losses. In future arrays, 30-percent array efficiency is feasible with an increase in device efficiency to 35 percent.

C. EIRP

A common figure of merit for a transmitter array is the effective isotropic radiated power (EIRP). The measured EIRP for the array, based on results for the best five-element subarray, is 56 dBm with 1 W of input power. For the 21-element phased array, the power into the coaxial connector feeding the power divider is the transmit power and the gain of the array includes all the losses from that point. Table 1 summarizes the gain and loss of the array components and predicts an EIRP of 57 dBm.

IV. Array Modules

A. Antenna Module

The Vivaldi slotline antenna element design and passive array analysis was performed under contract with the Uni-

versity of Massachusetts [3,4]. The slot antenna is fed with a microstrip-to-slotline transition from the back side of the substrate for easy integration in a planar microstrip configuration with MMIC amplifiers and phase shifters. The two sides of the antenna substrate, containing five active and two parasitic elements, are shown in Fig. 6.

The optimum element spacing takes into consideration the reflector system, packing density, and grating lobes. For an isotropic element beam, as the spacing increases to greater than 1.0λ, the directivity decreases due to losses in the grating lobes; however, by using elements with higher gain, such as Vivaldi slots (12-dB gain), this loss is reduced while allowing more space between elements to accommodate the MMICs. The University of Massachusetts and JPL performed a study and concluded that an element spacing of 1.22λ could be tolerated while maintaining high (>95 percent) radiative efficiency. This element spacing was selected for the 21-element array.

B. Amplifier Module

Two types of amplifer MMICs were integrated into the array. The devices used are pseudomorphic high-electron-mobility transistor (PHEMT) MMICs designed by Texas Instruments' (TI) Central Research Laboratory [5]. The first device is a three-stage amplifier with transistors of gate widths 50 μm, 100 μm, and 250 μm in cascade. Gate and drain bias circuitry are fabricated on the chip. The best device of this design is capable of 30-percent power added efficiency, 190-mW output power, and 23-dB gain at 31 GHz. Typical devices produce 20-percent efficiency, 100-mW output power, and 20-dB gain at 32 GHz. A photograph of the chip appears in Fig. 7(a).

Due to lack of availability of the first MMIC, a second three-stage device [Fig. 7(b)] was obtained from TI and integrated into the two three-channel modules. This device had lower gain (12 dB) and required a different bias voltage than the others, and therefore produced only 25 mW of RF input at 32 GHz under the fixed RF input and dc bias conditions of the array. However, under proper operating conditions, TI reports that this device is capable of >30-percent PAE, 250-mW output power, and 18-dB gain at 31 GHz.

Five amplifier MMICs were integrated on a single carrier module. All devices share common drain and gate supplies so that only two dc lines are required to interface to the module. In this approach, not all the devices are optimized at the same bias point, so RF power and efficiency are traded for array-biasing simplicity. The printed circuitry for a module is combined on one substrate, which simplifies assembly since all the channels are automatically aligned; however, the substrate becomes more complicated and reworking individual channels is less convenient than if each amplifier were first integrated into a submodule.

The original design contained a cascade of two amplifiers: the 100-mW driver amplifier followed by a power amplifier capable of 5-dB gain and 350-mW output power. The 350-mW device consisted of a single stage with 800-μm gate periphery and no on-chip bias or decoupling circuitry. The two devices were integrated on the module and tuned in a coaxial test fixture. Upon integrating the cascade of amplifiers with the antennas and phase shifters, destructive oscillations occurred and the circuit design was reevaluated. Modifications to the bias circuit were made in an attempt to prevent oscillation; however, schedule and resource constraints did not permit the extent of rework that was required. The approach taken was to use only the 100-mW amplifier, which has proved to be stable by itself in the module. A 50-Ω transmission line fabricated on quartz was placed in the second substrate cutout where a suitable high-power device could be inserted in the future. A photograph of the modified amplifier module is shown in Fig. 8.

The amplifier modules were measured on a scalar network analyzer setup. The best amplifier module produced 560 mW with 17-percent power-added efficiency at 32 GHz. Frequency response and efficiency measurements for an amplifier module are shown in Fig. 9. Crosstalk between channels was observed to be as high as −20 dB at 32 GHz. A channelized cover machined from RF-absorbing material was placed over the module, which reduced the crosstalk by >10 dB.

Molybdenum was the selected carrier material because of its relatively high thermal conductivity as compared to other materials with a temperature coefficient of expansion matching the alumina substrate. A trade study was performed to analyze the thermal performance of various die-attach methods with the result that gallium arsenide (GaAs) chips were gold-eutectic soldered to a copper subcarrier and then silver epoxied to the molybdenum carrier. A thermal model of the 21-element array was developed, and the predicted temperature rise from the carrier to the chip was calculated to be 20 deg C, with a channel temperature of 61 deg C. Actual temperatures were measured using thermocouples placed on the array. Predicted and measured temperatures agree to within 5 deg C.

C. Phase Shifter Module

The phase shifter module contains the 4-bit switched-line phase shift MMICs designed by Honeywell under con-

tract with NASA Lewis Research Center. Associated with each phase shift MMIC is an addressable digital serial-to-parallel converter application-specific integrated circuit (ASIC) designed at JPL. Use of this ASIC reduces the number of signal lines to each module from 35 to 6. A photograph of a single path appears in Fig. 10.

The power dividers and phase shifters were integrated together and measured on a vector network analyzer. Typical insertion loss was around 20.5 dB, measured without the vertically oriented power divider, which provides an additional 9-dB loss. These measurements are consistent with previous measurements of the separate components, as recorded in Table 1. Phase errors were less than 10 deg. Plots of insertion loss and phase at 32 GHz as a function of phase state are shown in Figs. 11(a) and (b). The load impedance presented to the amplifiers was also measured, and plots of the output return loss $|S_{22}|$ for different phase states are shown in Fig. 11(c). Lower loss phase shifters are becoming available from industry and will be implemented in future arrays.

V. Summary

A phased array transmitter operating at 32 GHz with 2-W total RF power and 9-percent total efficiency, with a capability of 16-percent efficiency, has been demonstrated using existing devices. This is based on the performance of the best five-element subarray. The method of spatially combining low-power devices to increase transmit power has proved successful. Beam steering in a 10-deg cone by the phase shifters was also demonstrated, with a scan loss of −1.5 dB and a peak side-lobe level of −10 dB.

Fabrication of the hardware provided valuable practical experience in the area of MMIC insertion. System-level issues for arrays were also addressed, including accommodation for bias and control for many individual elements and reduction of crosstalk within the array. By integrating the full array, procedures and control software for operating and evaluating the array were developed. The existing array will be used as a testbed for more efficient antennas, power dividers, and devices.

Several areas for future work have been identified. MMIC technology is the key to realizing economical large arrays, and a fast and universal method for evaluating state-of-the-art devices is being developed. Advanced MMIC power amplifiers are under development with improved RF output and efficiency. Packaging of individual devices and modules at 32 GHz is the next major step from a testbed to a breadboard phased array. Device packaging will address hermeticity, crosstalk, thermal management, and radiation as well as facilitate device handling. Advances in these areas will enable smaller, more efficient array designs needed for future microspacecraft missions.

Acknowledgments

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References

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Table 1. Gain summary.

Parameter	Value	
Input power, dBm		31.5
Power division (÷21), dB	−13.2	
Power divider insertion loss, dB	−4.3	
Phase shifter insertion loss, dB	−12.2	
Amplifier gain, dB	18.0	
Power combination (×21), dB	13.2	
Antenna gain, dB	24	
Total, dB	25.5	
EIRP, dBm		57.0
Total radiated power, W		2.0

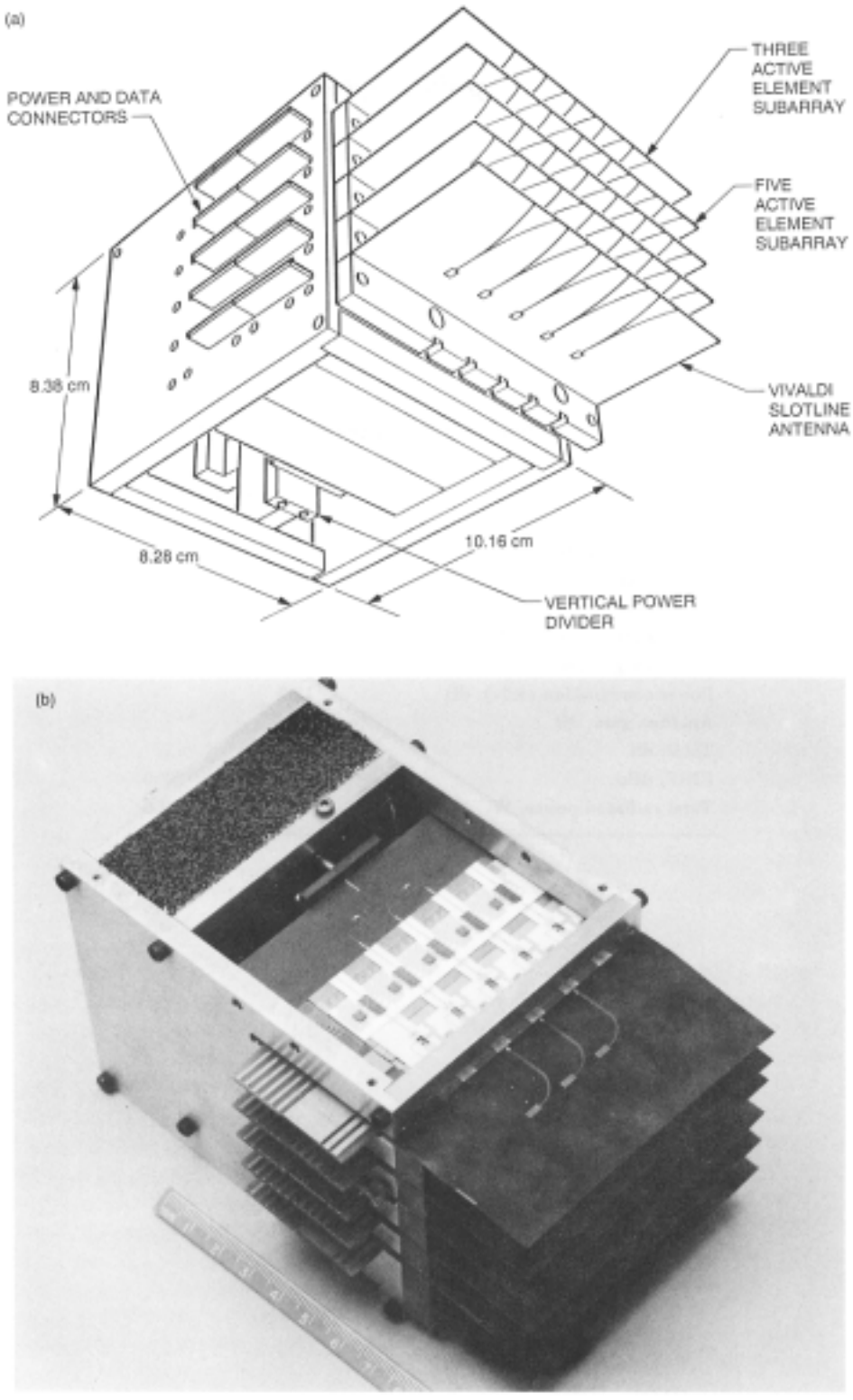


Fig. 1. The 32-GHz phased array transmitter feed: (a) subarray modules integrated into a two-dimensional array and (b) the completed testbed array. The use of highly integrated solid-state devices reduces the overall volume and simplifies array construction. MMICs provide phase shifting and amplification at 32 GHz. Custom designed digital ASICs provide phase shift control and reduce the number of signal lines required for the array.

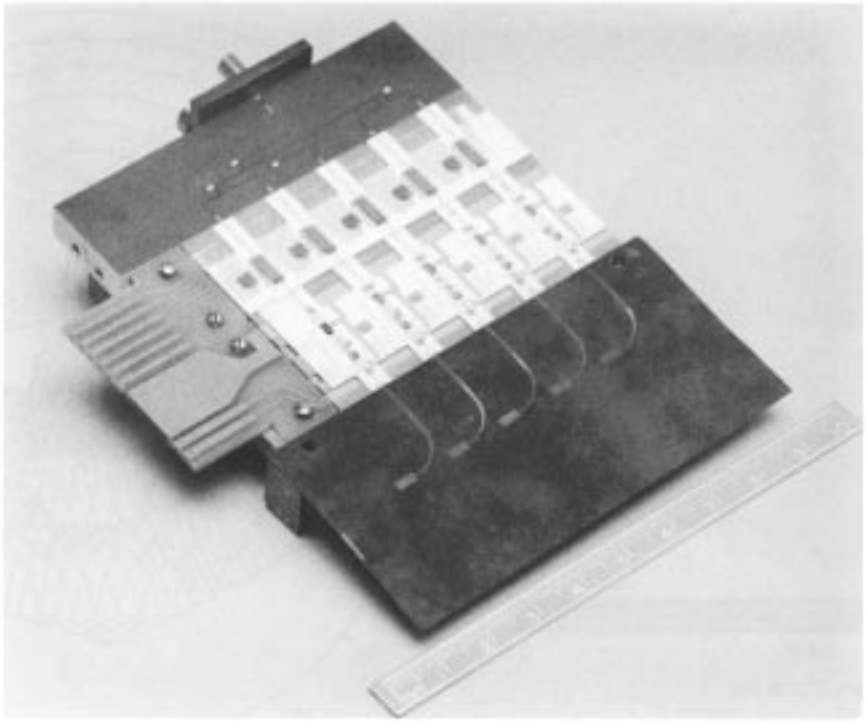


Fig. 2. Power divider, phase shifter, amplifier, and antenna modules integrated into a five-element subarray tray.

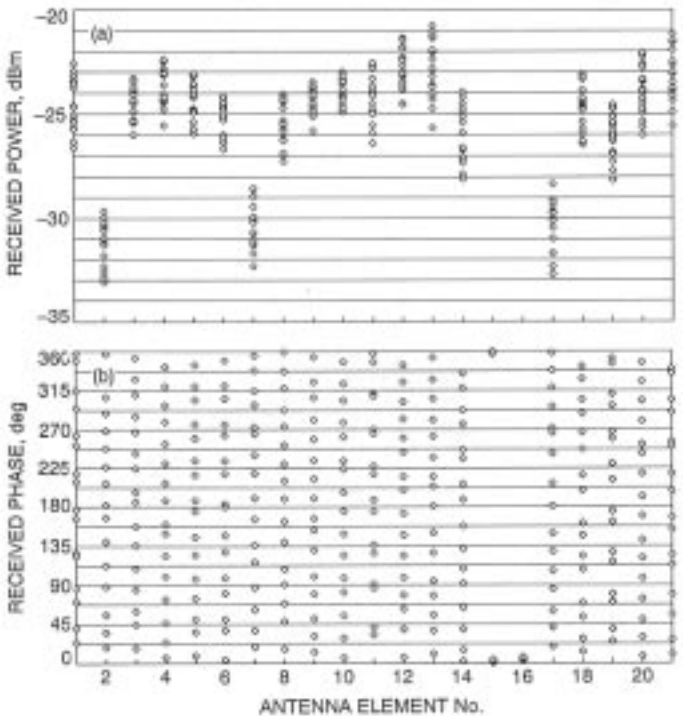


Fig. 3. Received amplitude (a) and phase (b) for each of 21 elements in each of 16 phase shifter states measured in the far field of the array at 32 GHz.

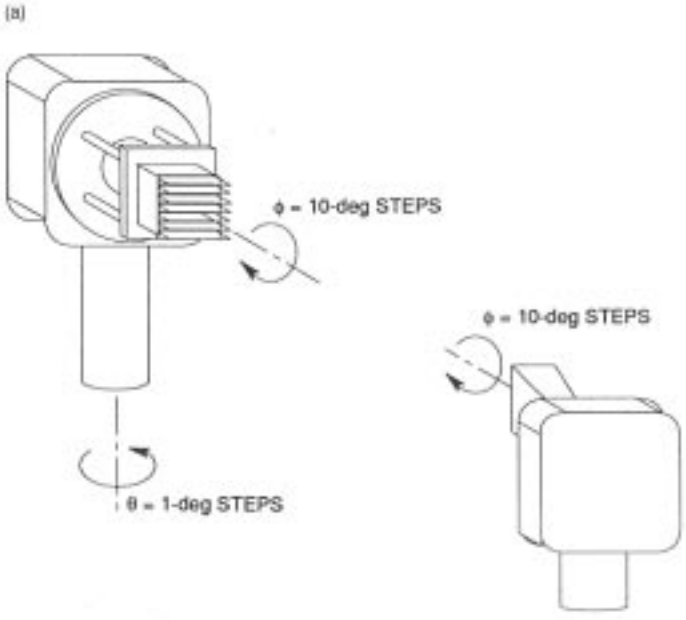
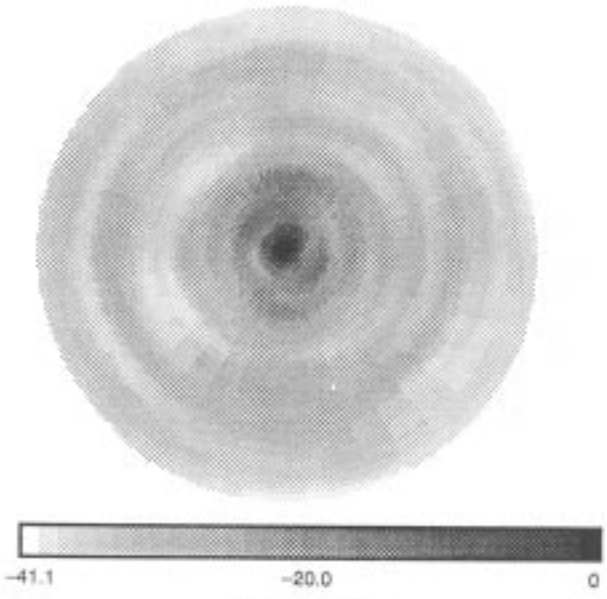
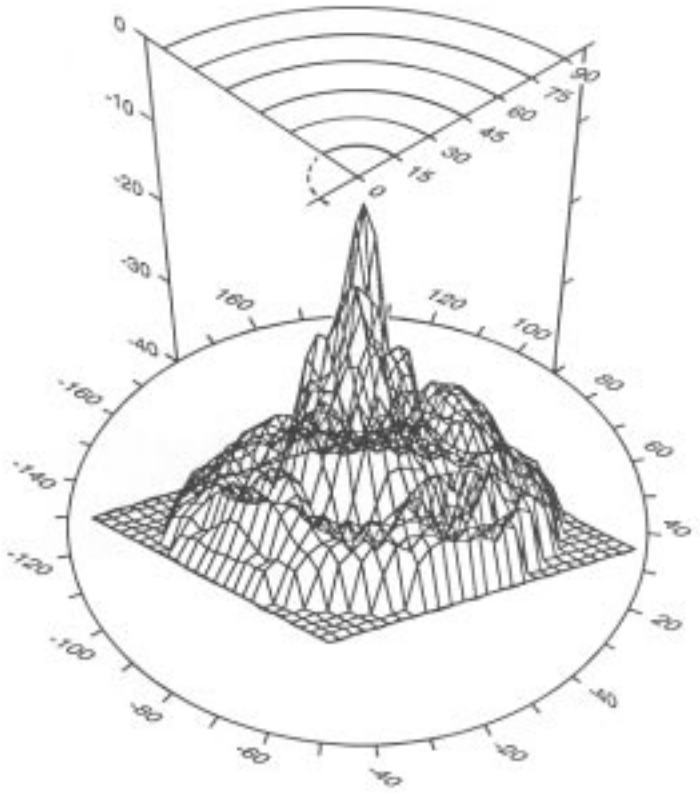


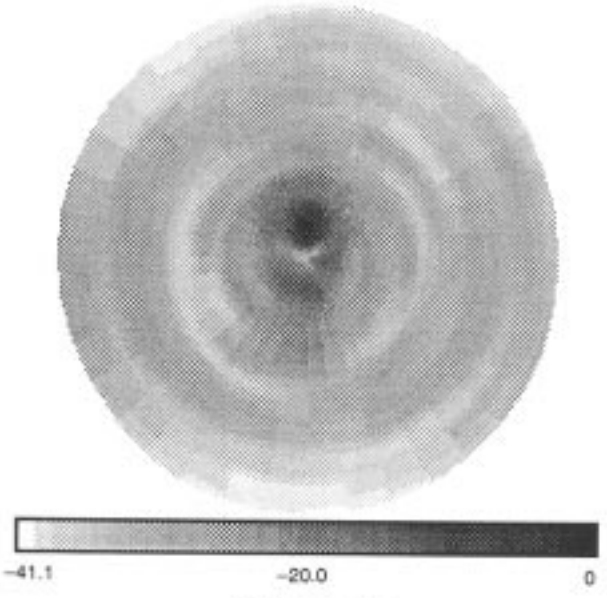
Fig. 4. Three-dimensional antenna pattern generation for the array: (a) pattern ϕ cuts generated by sweeping in azimuth and three-dimensional patterns formed from cuts with ϕ = 0 to 180 deg, with receive horn rotated to maintain copolarization; (b) measured far-field antenna patterns of the array feed pointed boresight; and (c) scanned 10 deg. Half-power beamwidths are 9 deg, and peak side lobe levels are −13 dB and −10 dB for the boresight and scanned beams, respectively.

(b)





(c)



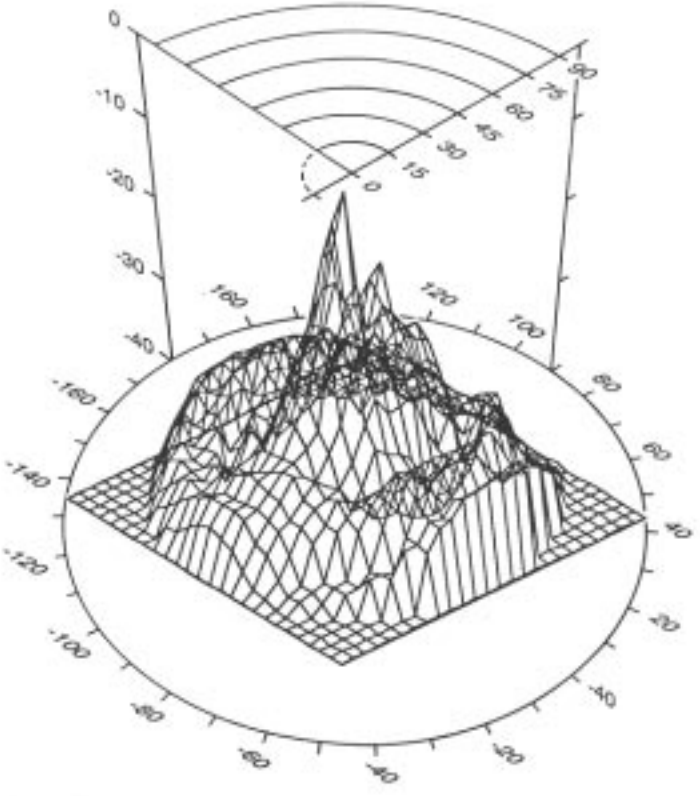


Fig. 4 (contd).

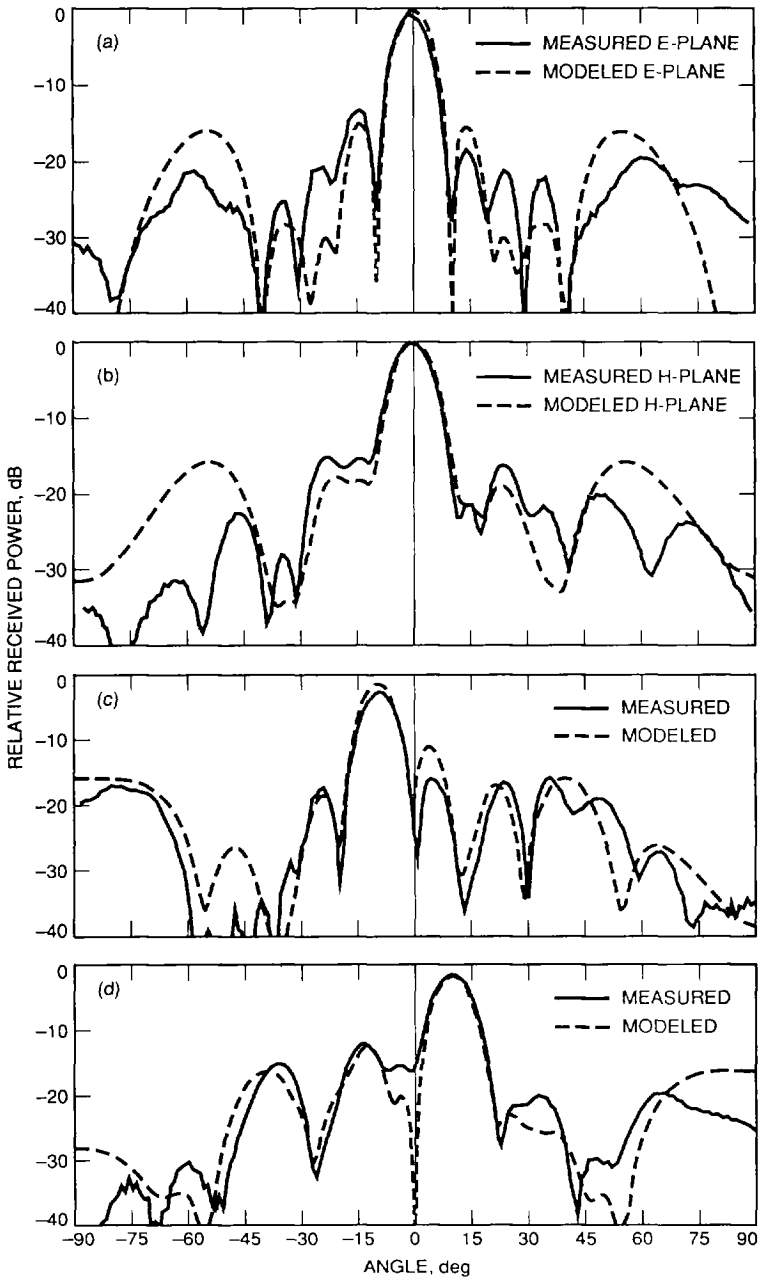


Fig. 5. Comparison of measured and modeled patterns of the phased array: (a) E-plane at boresight; (b) H-plane at boresight; (c) scanned 10 deg in the E-plane; and (d) scanned 10 deg in the H-plane. (The model assumes an element main beam shape of (cos θ)^{10} with a constant side lobe level of −15.7 dB.)

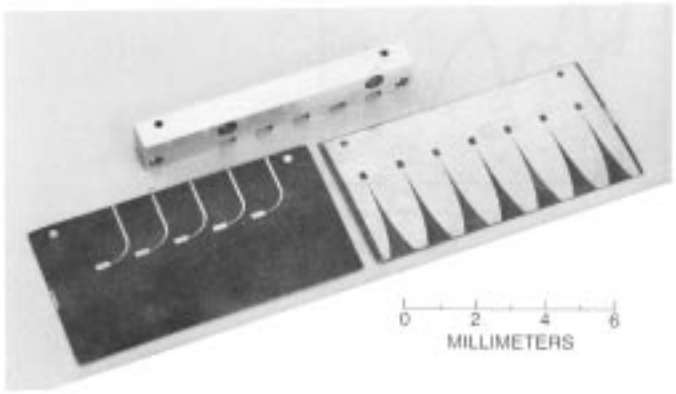


Fig. 6. The Vivaldi antenna substrate. Five active and two parasitic printed antennas are etched on one side (right) and microstrip-slotline transitions are etched on the opposite side (left).

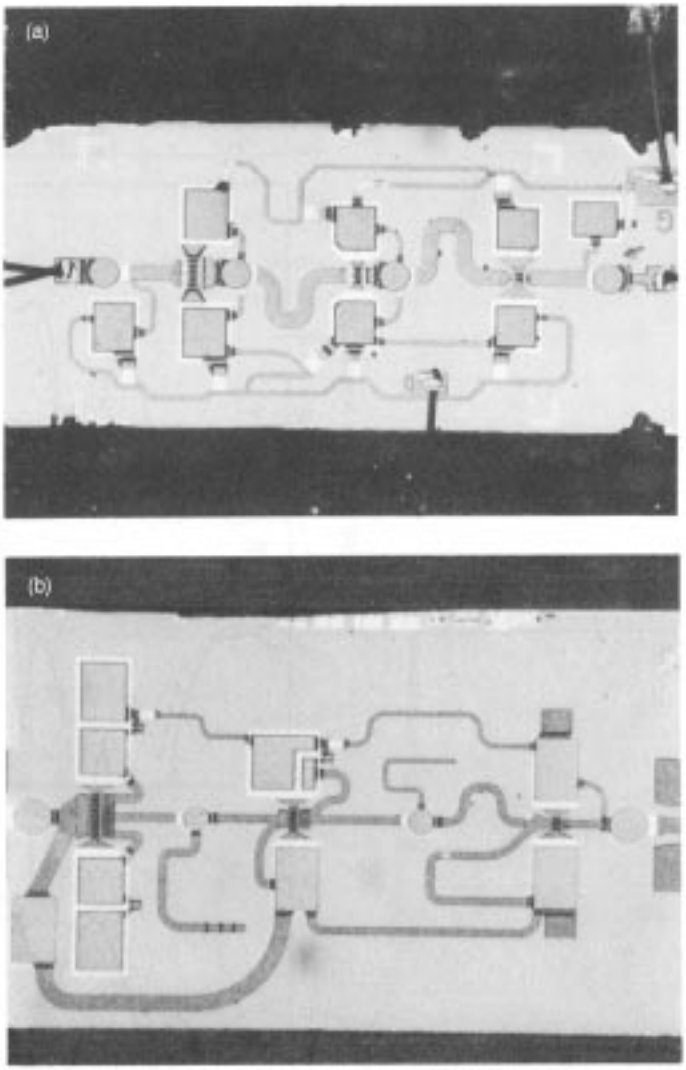


Fig. 7. Amplifier MMICs: (a) the 50-, 100-, and 250-μm amplifier and (b) the 100-, 200-, and 400-μm amplifier.

Fig. 8. Amplifier module containing the 100-mW 32-GHz amplifier and 50-Ω through line.

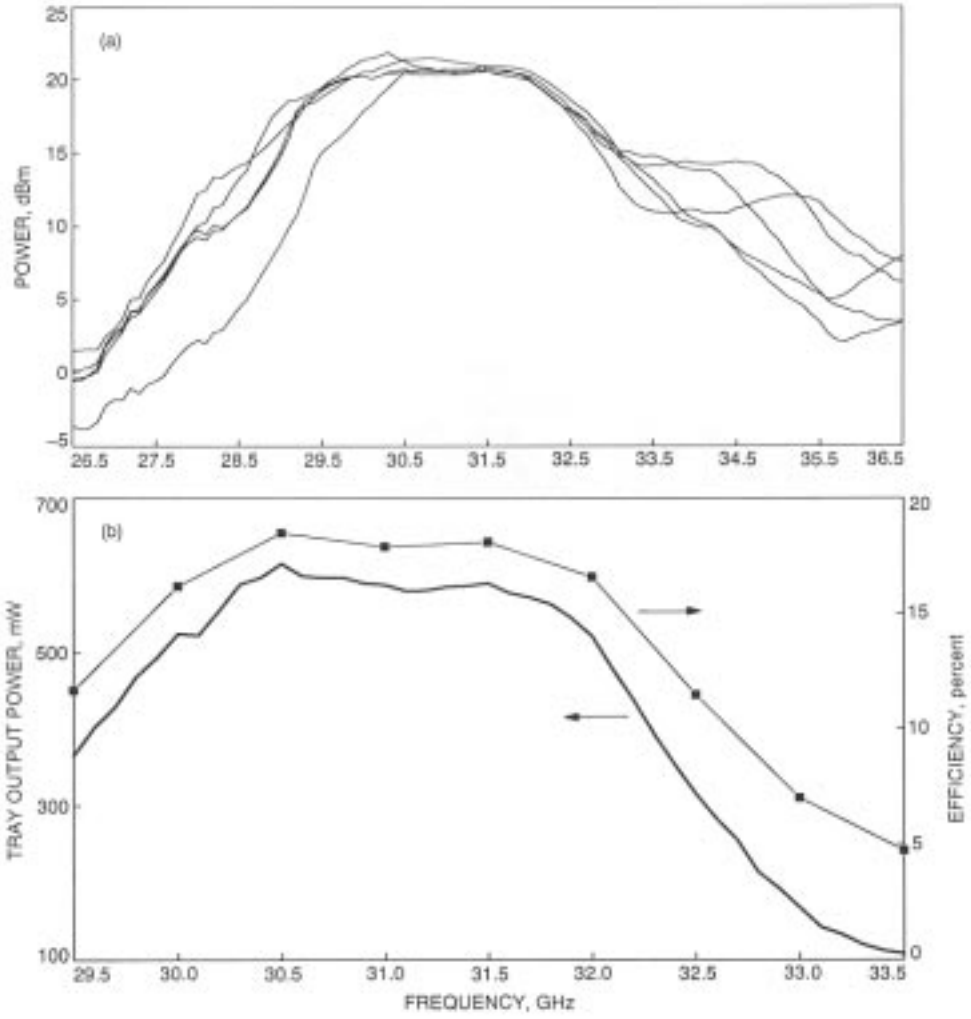


Fig. 9. Amplifier module measurements: (a) output power of each of five paths on an amplifier module over the 26.5- to 36.5-GHz range with 2-dBm input power and (b) total power and efficiency of the amplifier module.

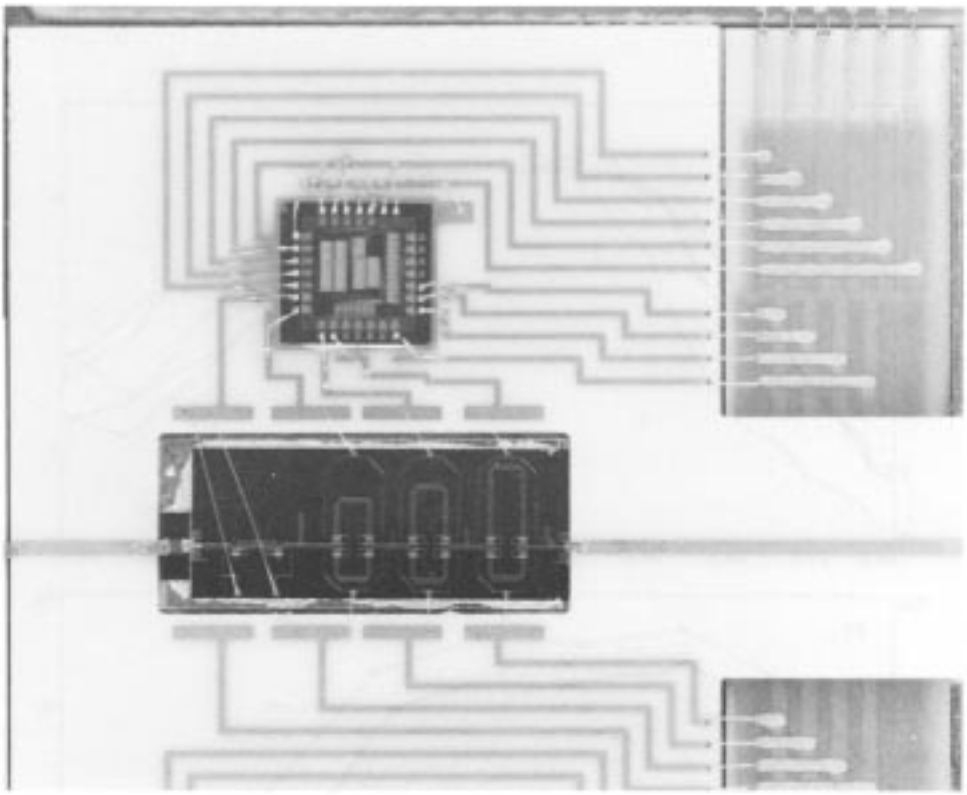


Fig. 10. A single path on a phase shifter module containing the phase shifter MMIC from Honeywell, the controller ASIC, and RF, DC, and control signal lines on the alumina substrate.

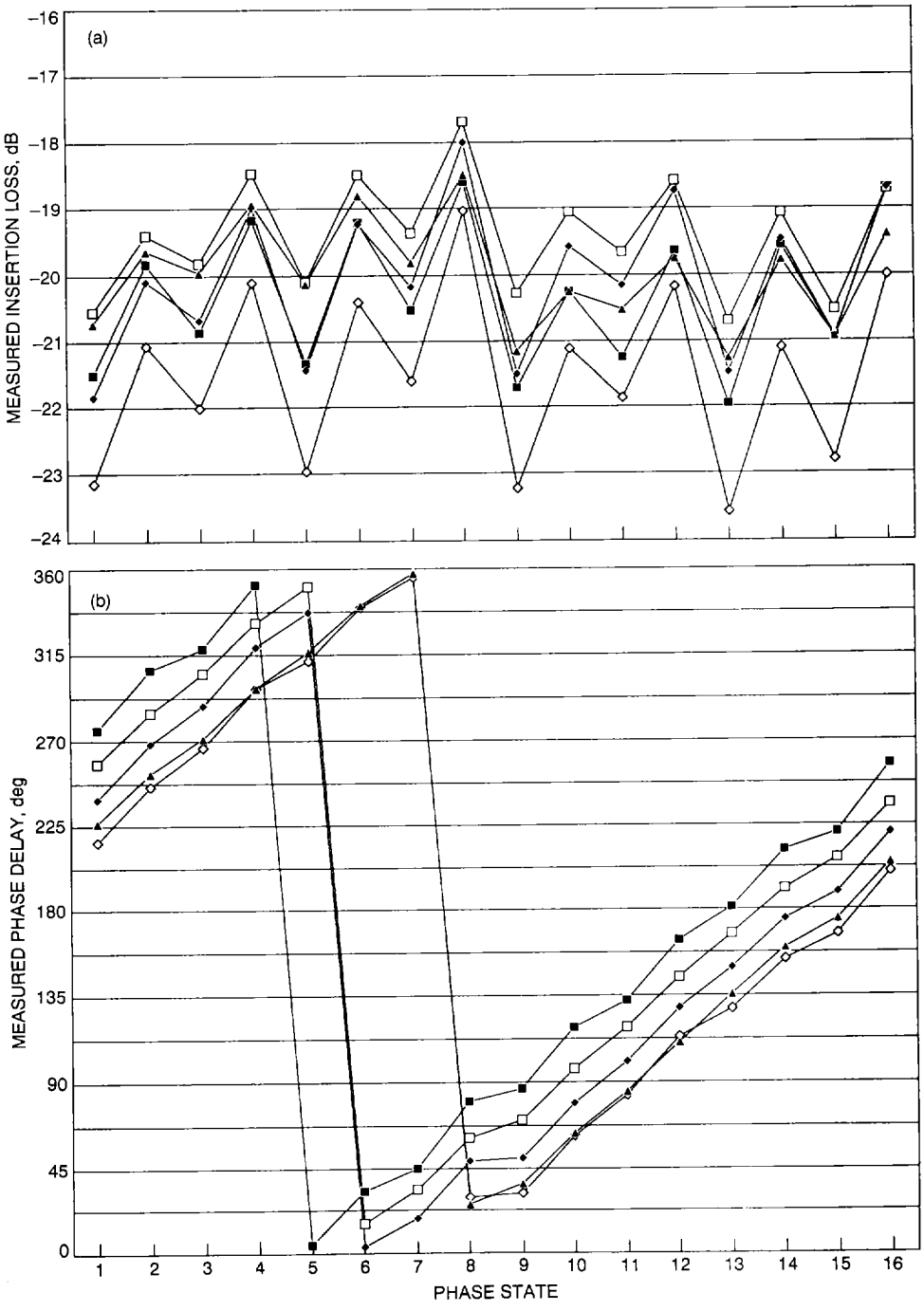


Fig. 11. Phase shifter module measurements: (a) insertion loss and (b) phase for each of five paths in each of 16 states at 32 GHz; (c) output return loss of a single path in each of 16 states over the 26.5- to 36.5-GHz range.

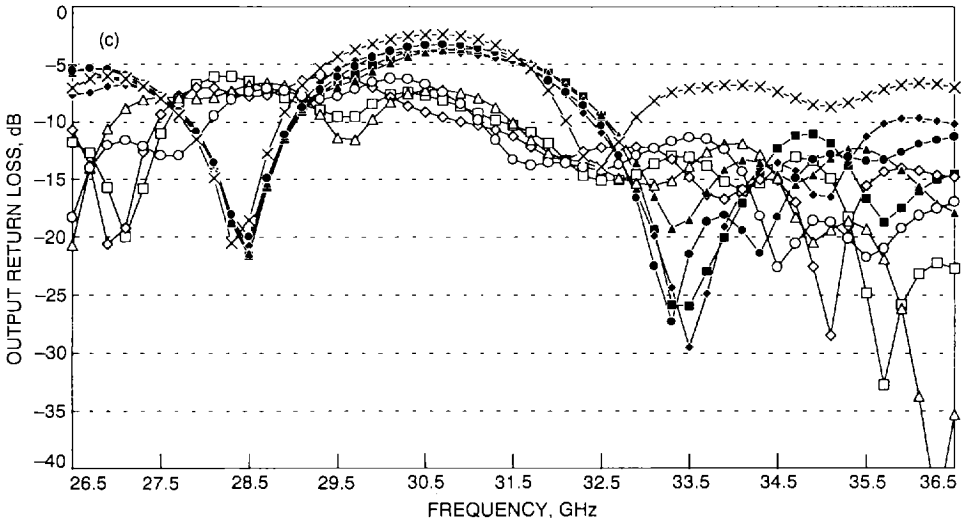

(c)
0
−5
−10
−15
−20
−25
−30
−35
−40
OUTPUT RETURN LOSS, dB
26.5
27.5
28.5
29.5
30.5
31.5
32.5
33.5
34.5
35.5
36.5
FREQUENCY, GHz

Fig. 11 (contd).