Further Results on a Reduced-Complexity, Highly Power-/Bandwidth-Efficient Coded Feher-Patented Quadrature-Phase-Shift-Keying System with Iterative Decoding

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Based on a representation of Feher-patented quadrature-phase-shift keying (FQPSK) as a trellis-coded modulation, this article continues the investigation of the potential improvement in power efficiency obtained from the application of simple (small number of states) outer codes to form a concatenated coding arrangement with iterative decoding. For the additional two of the three concatenation configurations previously suggested, specific numerical results are presented for rate-1/2 outer codes. These results are then compared with the coding gains previously reported for the first of the three configurations, all of which are based on using a reduced-complexity FQPSK receiver. Finally, in an attempt to trade power-efficiency improvement with the bandwidth expansion associated with the outer code rate, we consider the performance of the coded FQPSK system using rate-3/4 outer codes.

I. Introduction

In a previous publication [1], the authors demonstrated that, by coupling (through an interleaver) very simple, short constraint-length outer codes with the convolutional inner coding inherent in Feher-patented quadrature-phase-shift keying (FQPSK) itself [2] and using iterative decoding at the receiver, one is able to obtain a significant signal-to-noise ratio (SNR) improvement above that achieved by FQPSK alone while at the same time preserving the bandwidth efficiency of the modulation.[2] Three schemes were suggested for the concatenated coding/iterative decoding arrangement (two of which were serial and one of which was parallel); however, specific results were presented for only one of the three schemes as a means of demonstrating the gain that could be achieved. Furthermore, only rate-1/2 outer codes were considered.

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[1] Communications Systems and Research Section.

[2] Needless to say, there is an inevitable bandwidth expansion that occurs proportional to the inverse of the code rate. However, the coding (power) gain obtained from the concatenation of the outer code with the inner code inherent in FQPSK more than compensated for this bandwidth expansion.

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In this article, we investigate the performance of the other two coding schemes suggested in [1] and also consider higher rate (i.e., 3/4) outer codes constructed from punctured versions of rate-3/6 codes. The use of a rate-3/4 code as opposed to a rate-1/2 code reduces the bandwidth expansion of the coded modulation from a factor of 2 to a factor of 4/3 at the cost of a reduction in SNR improvement. As pointed out in [1], while the full benefit of the power-efficiency improvement would be obtained using the optimum receiver, i.e., one that implements a 16-state trellis [2], a reduced-complexity Viterbi receiver with only 2 states per in-phase (I) and quadrature (Q) channel [3] yields uncoded FQPSK performance within a few tenths of a dB of the optimum one. Using this as motivation, the receivers considered in [1] for the coded case were based on this simplified (reduced-complexity) architecture, and we shall once again follow the same consideration here.

II. Error-Correction Coded FQPSK with Iterative Decoding

Motivated by the potentially large coding gain achievable with iterative decoding of concatenated codes using a soft input–soft output (SISO) a posteriori probability (APP) algorithm, the authors set out in [1] to apply this technique to FQPSK, which by virtue of its inherent coding supplies the inner code. As mentioned in the introduction, to keep matters simple, the investigations considered applying the outer code to an FQPSK system using the simplified receiver of [3], where the 2-state Viterbi algorithms (VAs) are now replaced with 2-state SISO algorithms [4], which in a max-log version are equivalent to modified soft-output VAs (SOVAs) [5]. In order to have a coding gain resulting from the interleaving process between the inner and outer codes, the I and Q FQPSK nonrecursive inner codes were remapped to recursive types [6]. This remapping was aimed at providing recursiveness for the parts of the FQPSK encoders that are matched to the reduced 2-state SISO decoder for the inner code (see [1] for further details).

With regard to the manner in which the outer code is applied to the FQPSK modulator/demodulator, we proposed in [1] three different concatenation schemes, each of which incorporates iterative decoding [see Figs. 1(a) through 1(c)] but only presented performance results for the scheme in Fig. 1(a). Here we present results for the configurations in Figs. 1(b) and 1(c), assuming first the same rate-1/2 outer codes [see Figs. 2(a) and 2(b)] as those considered in [1].

Comparing Figs. 1(a) and 1(b), we observe that both of these schemes are of the serial concatenation type, the difference being that in the latter a single outer code is used to generate the inputs to the I and Q FQPSK channels whereas in the former independent outer codes are used for these same channels. As such, the symbol rate of the encoder output in Fig. 1(b) is $2R_b$, whereas the symbol rate of the I and Q encoders in Fig. 1(a) is R_b. In both cases, the symbol rate of the I and Q inputs to the FQPSK modulator is R_b; hence, they produce transmitted signals with the same power spectral density (PSD) or, equivalently, identical bandwidths. Also, whereas in Fig. 1(a) the iteration at the receiver is performed independently on the I and Q channels, i.e., the SISO outer decoder outputs are fed back only to their respective SISO FQPSK (inner) decoder inputs, the iteration in the receiver of Fig. 1(b) affects both the I and Q channels, i.e., the single SISO outer decoder output is fed back (after demultiplexing) to both the I and Q SISO FQPSK (inner) decoder inputs. Assuming interleaver block sizes of $N = 2048$ and $N = 16,384$ symbols (corresponding to blocks of 1024 and 8192 input bits) and 5 iterations, Fig. 3 illustrates a comparison between the average bit-error probability (BEP) performances of the schemes in Figs. 1(a) and 1(b). We observe from Fig. 3 that the two schemes have virtually identical performances. Thus, the choice between the two schemes becomes a matter of implementation complexity and encoder speed rather than performance.

The third scheme in Fig. 1 is a parallel concatenated coding scheme of the turbo-coding type. Here there are no explicit SISO outer decoders but rather the I and Q SISO FQPSK (inner) decoder outputs are fed back (after suitable interleaving and deinterleaving) to the opposite (I to Q and Q to I) SISO FQPSK decoder inputs to produce the desired iteration. After the desired number of iterations, the

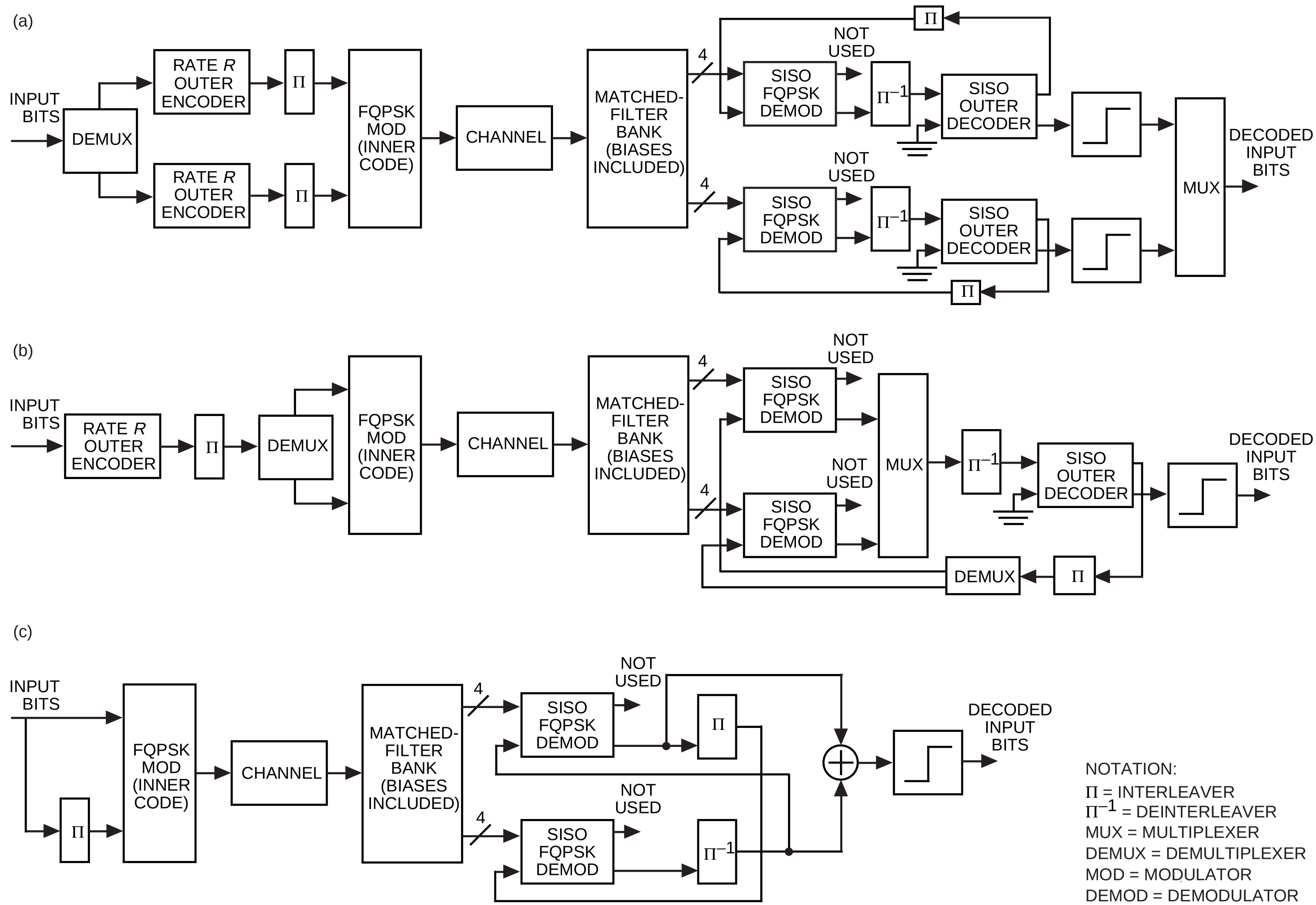

Fig. 1. Several transmitter–receiver combinations for coded FQPSK with iterative decoding: (a) serial concatenation scheme 1, (b) serial concatenation scheme 2, and (c) parallel concatenation scheme.

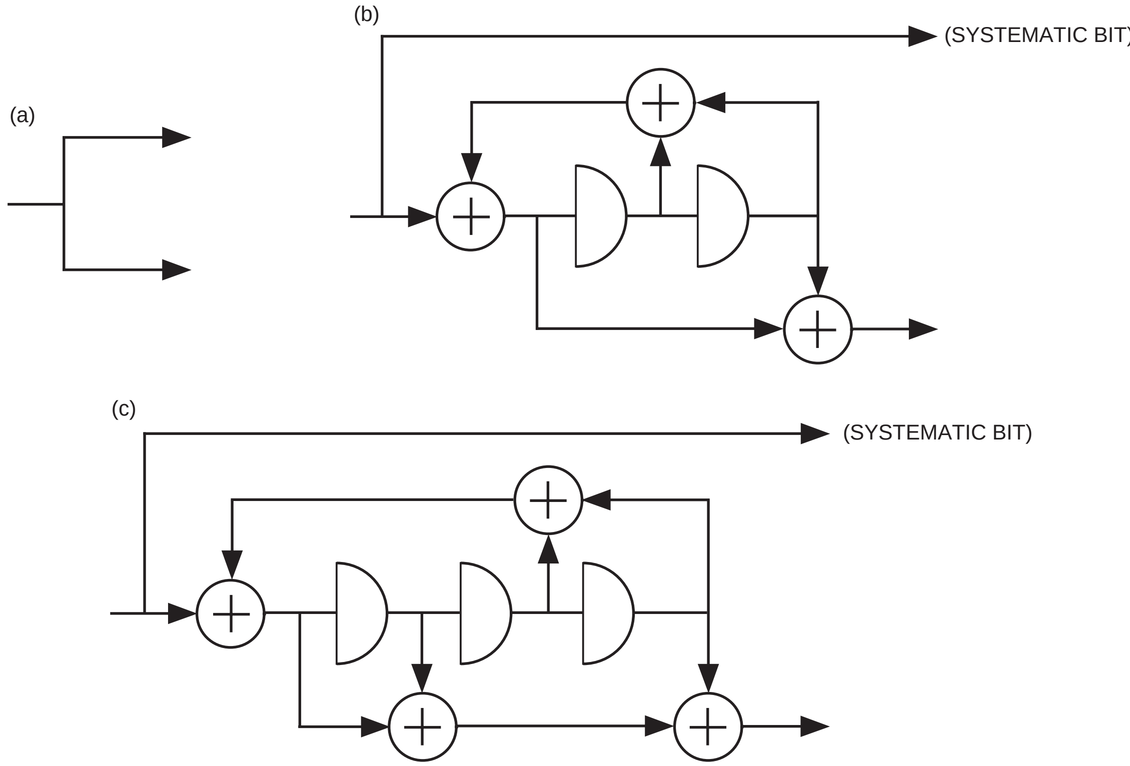

Fig. 2. Outer codes: (a) repetition code, (b) optimum 4-state encoder (recursive version), and (c) optimum 8-state encoder (recursive version).

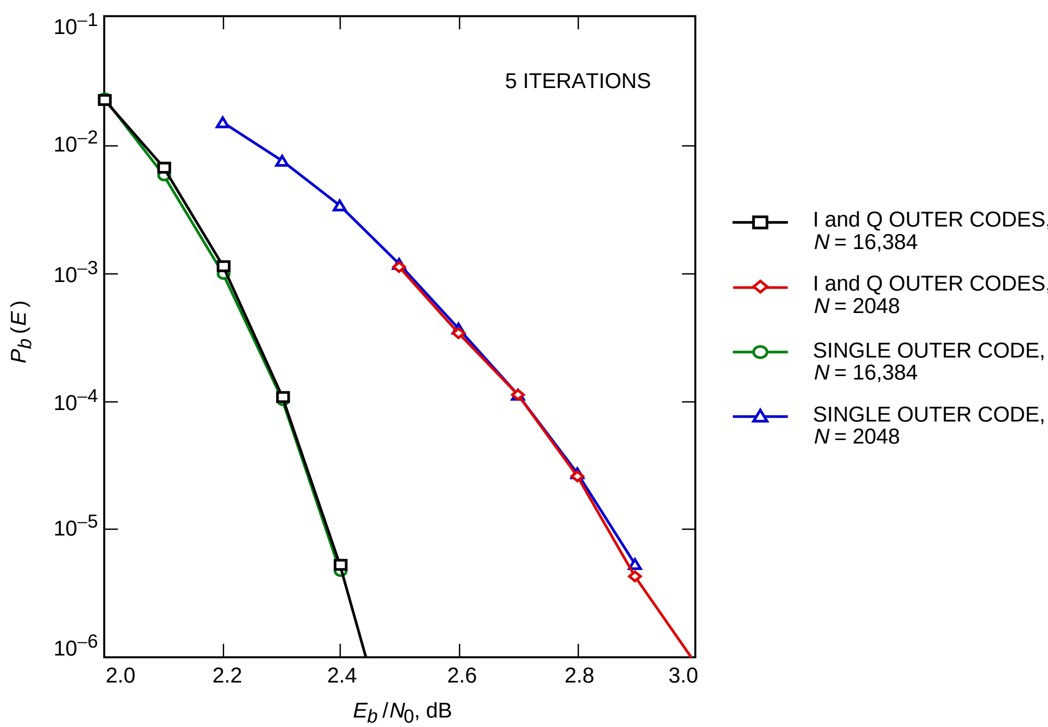

Fig. 3. A comparison of the BEP performances of two different serial concatenated coded FQPSK systems: optimum 4-state outer code.

I SISO FQPSK decoder output is combined with the deinterleaved Q SISO FQPSK decoder output to allow for a hard decision on the input bits. Figure 4 is a comparison of the BEP performances of the serial scheme of Fig. 1(a) using the rate-1/2 repetition code of Fig. 2(a) and the parallel scheme of Fig. 1(c) for the same interleaver sizes and the same number of iterations as in Fig. 3. We observe from these results that the turbo-coding scheme always outperforms the serial scheme, the difference between the two being about 1 dB at a BEP of 10^{-5}. Of course, when compared with the serial scheme using the optimum 4-state outer code, the turbo-coding scheme is still inferior.

Finally, the performance of the serial concatenation scheme of Fig. 1(a) with a rate-3/4 outer code was evaluated and compared with that of the same scheme using a rate-1/2 outer code. The rate-3/4 codes were obtained by treating the optimum 4-state and 8-state codes of Figs. 2(b) and 2(c) as rate-3/6 codes and then puncturing two of the output bits. Also, to obtain integer symbol interleaver sizes, the input bit block sizes used previously were changed by one to 1023 and 8193. This resulted in symbol interleaver sizes of $N = (4/3) \times 1023 = 1364$ and $N = (4/3) \times 8193 = 10,924$, respectively. Figure 5 is a comparison of the above-mentioned performances. We observe that although, as expected, the rate-1/2 codes outperform the rate-3/4 codes, the latter are still quite power efficient (relative to the uncoded FQPSK case) and now only expand the bandwidth by a factor of 4/3.

III. Conclusions

We have again shown that, by applying simple outer codes to an FQPSK modulation to form a concatenated coding arrangement with iterative decoding, it is possible to achieve a highly power- and bandwidth-efficient system. Two serial and one parallel concatenation configuration have been discussed, and comparisons of BEP performance among the three schemes have been presented. Consideration of higher-rate (3/4 as opposed to rate-1/2) codes to reduce the bandwidth expansion proportional to the inverse of the code rate has led to the conclusion that a high level of power efficiency (relative to uncoded FQPSK) is still achievable.

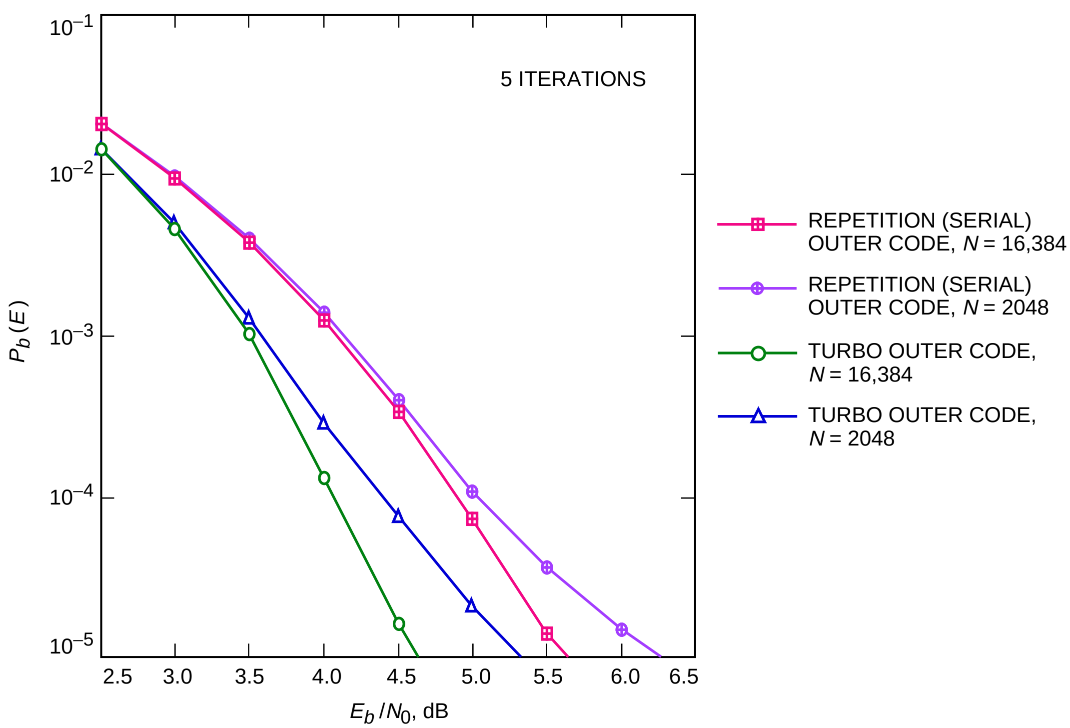

Fig. 4. A comparison of the BEP performances of serial and parallel (turbo) concatenated coded FQPSK systems: repetition outer code.

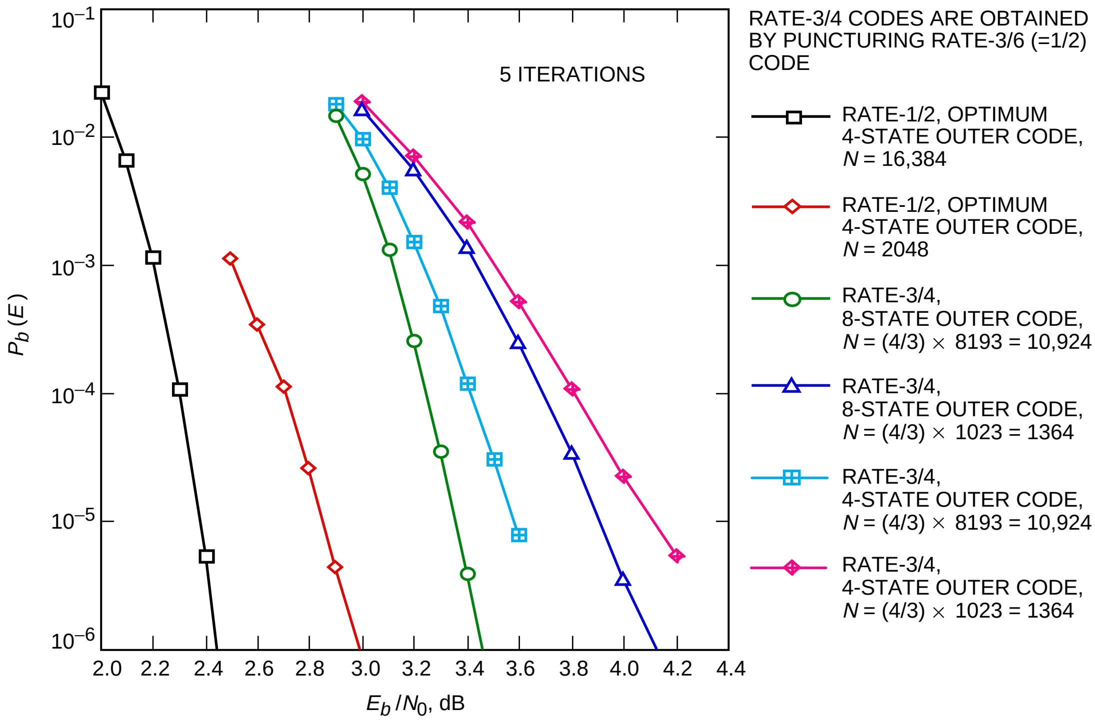

Fig. 5. A comparison of the BEP performances of serial concatenated coded FQPSK systems: rate-3/4 and optimum rate-1/2 outer codes.

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