Signal Processing in the Deep Space Array Network

R. Navarro[1] and J. Bunton[2]

This article describes the requirements and architecture of a signal processing subsystem for a Deep Space Array Network being designed for the Deep Space Network. The emphasis is placed on hardware structures and signal flow. A methodology for sampling a 500-MHz bandwidth signal at 1280 MHz is examined. Two possible architectures for the digital signal processing are presented.

I. Introduction

The JPL Deep Space Network (DSN) is currently investigating the use of a large number of relatively small (12-m) antennas arrayed together to both augment and replace the current 34-m and 70-m antennas. Another goal is to provide dramatically increased data rates for future missions. Because of the antennas' smaller size as compared with the current 34-m and 70-m antennas, they can be produced for a reduced cost. Also, the use of many antennas instead of one antenna gives greater fault tolerance. Losing one antenna would result in only a small loss to the signal-to-noise ratio (SNR) rather than in loss of an entire pass. In addition, with an array of antennas, it is now easier to break up the collecting area of this array to support various missions at the same time. The signal processing hardware necessary to support arraying a large number of antennas is much greater than for a single large antenna. However, advances in integrated-circuit densities make it feasible to consider arraying as many as 400 antennas in one geographically close (1-km) cluster.

The DSN has much past experience with antenna arraying. Arraying was used during the Neptune and Uranus encounters of the Voyager mission. Also, the Galileo mission used the full-spectrum arraying technique to obtain acceptable telemetry rates after its high-gain antenna failed to deploy. Currently, all the stations of the DSN are equipped with hardware to array up to four antennas as a backup to the 70-m antenna and to provide a scalable link to flight projects.

This new array would be a significant step forward in both performance and complexity. The current full-spectrum processor array (FSPA) supports up to four antennas, samples data at 256 MHz, and provides full-spectrum arraying of selectable 16-MHz bandwidths. The DSN Deep Space Array-Based Network (DSAN) will combine up to 400 co-located antennas, sample intermediate frequency (IF) data at 1280 MHz, and support arraying of signals with a 100-MHz bandwidth.

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[1] Tracking Systems and Applications Section.

[2] Commonwealth Scientific & Industrial Research, Sydney, Australia.

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Work is now being performed to determine the architecture for the array signal processing subsystem (ASPS) of the DSAN and to build a three-antenna breadboard with 6-m antennas to test the performance of the antennas, develop new technologies, and develop cost models of the system. Results from this breadboard will be used to develop a larger 12-m antenna prototype array.

This article describes the current designs and plans for the ASPS in the DSAN.

First, an overview of the functions, requirements, and components of signal processing in the DSAN is given. Then, the current design of the IF sampler is described. Next, a design for the digital portion of the ASPS is described that is based on the one used for the FSPA. It features a separate beamformer optimized for phasing the antenna signals and a wideband correlator for radio astronomy applications. Finally, an alternative design for the digital portion of the ASPS is described that uses a frequency-domain-based approach to combine the wideband correlator and beamforming hardware into one data flow.

II. Array Signal Processing Overview

The DSAN defines a cluster as a set of antennas co-located in a close geographic area, usually within 1 km. This cluster of antennas can be as large as 400. The first prototype array may contain only 12 antennas to have performance roughly equivalent to a 34-m antenna, but the system design needs to be scalable to sizes up to 400 antennas.

The functional design description of the DSAN imposes requirements on the array signal processing subsystem (ASPS). The antenna radio frequency (RF) subsystem can receive both X-band (8- to 8.8-GHz) and Ka-band (31- to 38-GHz) inputs at either right- or left-circular polarization. These signals will be converted to an intermediate frequency, and two will be sent to the ASPS. Each analog IF input of the ASPS will have a 1-dB bandwidth of 500 MHz centered at 950 MHz. Also, the group delay must be less than 1 ns over any 100-MHz bandwidth. In order to handle both high and low SNR signals, the digitized IF samples must have a dynamic range of at least 45 dB, which requires 8-bit sampling. The ASPS needs to provide phased-array signals with a sampling bandwidth of 125 kHz to 128 MHz from anywhere in the IF passband. The current design calls for 16 phased-array signals to be produced. Each individual antenna contributes to at most four phased-array signals. Also, a wideband (500-MHz) correlator must be provided for each of the two IF signals of an antenna for use in calibrating the array antennas, phasing an array using radio sources, and developing a catalog of radio sources for navigation purposes.

Figure 1 shows a block diagram of the main components of the ASPS. The IF sampler module receives two analog optical-fiber outputs from the RF–IF converter and digitizes these signals. The beamsplitter module takes the digital IF data at the full 500-MHz bandwidth and produces multiple copies of the signal at lower bandwidths. In each of these copies, the appropriate delay and phase for the direction of interest is applied so the signals from various antennas can be coherently combined in the beamformer. The beamsplitter also supplies a stream of data for use in a wideband correlator to support antenna calibration and other radio astronomy uses. The next modules are a beamformer and a wideband correlator. Both devices actually perform cross-correlation of the antennas pairwise or each against the sum of the others, but only the beamformer does the coherent combining of antenna signals. The beamformer and correlator may be the same actual hardware configured differently, or separate optimized hardware modules. Current telemetry systems accept only an analog input. To interface to them, we need to build a digital-to-analog output module for each phased-array digital signal output. Next-generation telemetry receivers may be able to use the digital output of the DSAN directly.

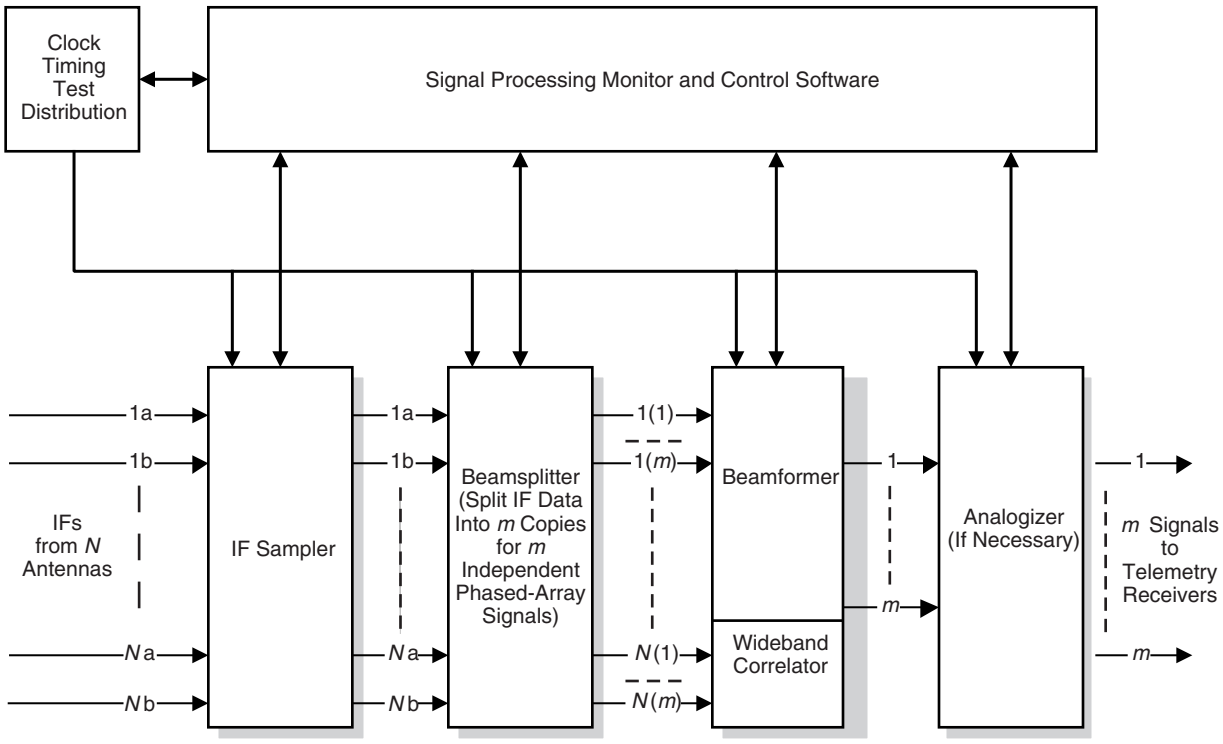

Fig. 1. DSAN array signal processing subsystem block diagram.

III. IF Sampling

The IF sampling module converts the optical signal back to an analog voltage and then performs analog anti-alias filtering. The output of the anti-aliasing filter then is passed on to the analog-to-digital converter (ADC) chip. The ADC chip is clocked by a 1280-MHz signal and samples the signal with 8 bits of resolution. The 8-bit data from the ADC, along with the 1280-MHz clock and one pulse-per-second (1-PPS) time tag, are converted into digital fiber-optic signals and sent to the digital portion of the signal processing hardware. A diagram of this system can be seen in Fig. 2.

To design a realizable anti-aliasing filter with both good amplitude and group delay characteristics, sampling must be done at a rate of at least 1280 MHz. Sampling at a higher rate would make the anti-aliasing filter design easier but would require more digital hardware. There are not many commercial samplers available at such high sampling rates. However, two good candidates were found. The Maxim MAX108 is a 1.5 gigasamples per second (Gsps) 8-bit ADC with an input bandwidth of 2.2 GHz. The Atmel TS83102G0 is a 2-Gsps 10-bit ADC with a 3-GHz input bandwidth. Because the amplitude response of the Atmel chip is flatter around the top of our desired sampling band (around 1200 MHz), it was decided to use the Atmel chip. Only the most significant 8 bits of the Atmel ADC will be used.

A prototype analog filter has been designed and tested that meets the required amplitude and group delay specifications. Figures 3 and 4 show measurements taken of two prototype filters. The plots confirm that both filters meet specifications and have good repeatability.[3] The filter has the required 1-dB bandwidth from 700 to 1200 MHz. It also has a 0.2-dB bandpass ripple and 30-dB attenuation of images at 580 MHz and 1360 MHz. Also, group delay variations are within ±1 ns over the passband.

[3] Design and test of the IF sampler anti-aliasing filter was performed by B. Rayhrer, Tracking Systems and Applications Section, Jet Propulsion Laboratory, Pasadena, California.

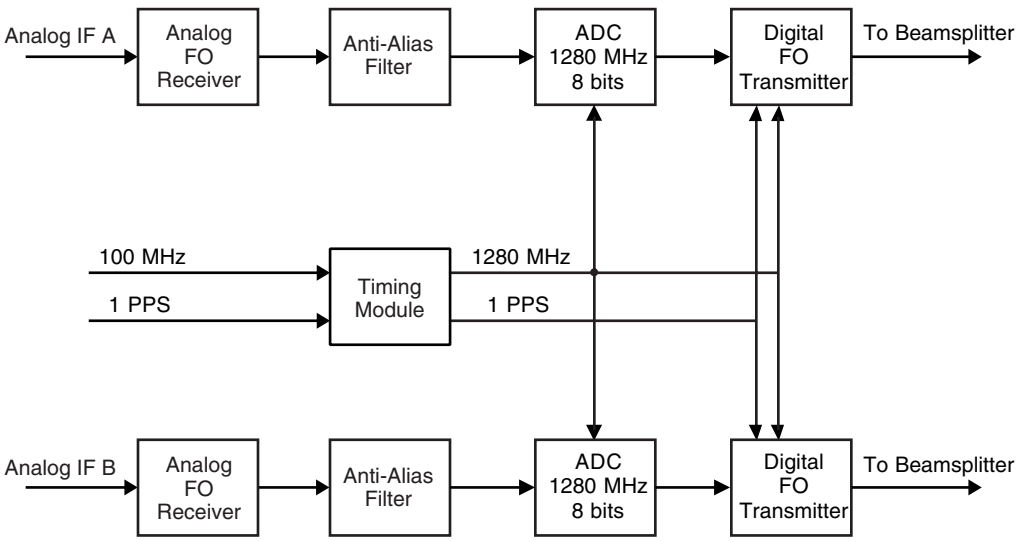

Fig. 2. IF sampler module.

The data going from the IF sampling module to the digital signal processing chassis will be transmitted via an optical link. Originally, the plan was to use five 2.5-gigabit per second (Gbps) serial optical links to perform the data transfer from the IF sampler to digital modules. However, serializing the data would have required high-speed digital logic to frame, encode, and serialize the data. Since the IF sampling is such a critical component of the signal processing infrastructure, it was decided instead to use the Infineon PAROLI 2 transmitter/receiver modules to send data from the IF sampler to the digital processing modules. The PAROLI modules have twelve 2.7-Gbps optical transmitters/receivers integrated together to transmit data over a 12 fiber-optic ribbon cable. The 8-bit data will be sent together with a 640-MHz clock and a 1-PPS timing signal. The optical-fiber link also has the advantage of providing excellent isolation of the IF sampler from interference generated in the digital portions of the system.

The 1280-MHz ADC sample clock will be generated by a surface acoustic wave (SAW) oscillator phase locked to a stable 100-MHz reference provided by the frequency and timing subsystem. The SAW oscillator was chosen to give excellent short-term stability with long-term stability provided by the 100-MHz reference.

IV. Time-Domain Beamformer with Separate Wideband Correlator

In this section, an architecture will be described that uses a beamsplitter to provide data to a beamformer that forms phased-array signals in the time domain and also to a separate wideband correlator. Each antenna will have its own beamsplitter. Each beamsplitter will choose up to four independent 125-kHz to 128-MHz bandwidth signals from within the 500-MHz digital input bandwidth from either antenna IF and apply the delay and phase model corrections to coherently add antenna signals. In addition, a full 500-MHz bandwidth signal will be provided for use in a wideband correlator for each antenna IF. The correlator will be an FX-type correlator, which first breaks the signals into frequency-domain components (F) before doing the cross-multiplication (X). The beamsplitter will break the data up into frequency-domain components for the FX correlator but will keep the signals in the time domain for the beamformer. The beamformer will coherently add antenna signals from the beamsplitter to form up to 16 phased-array signals or "beams."

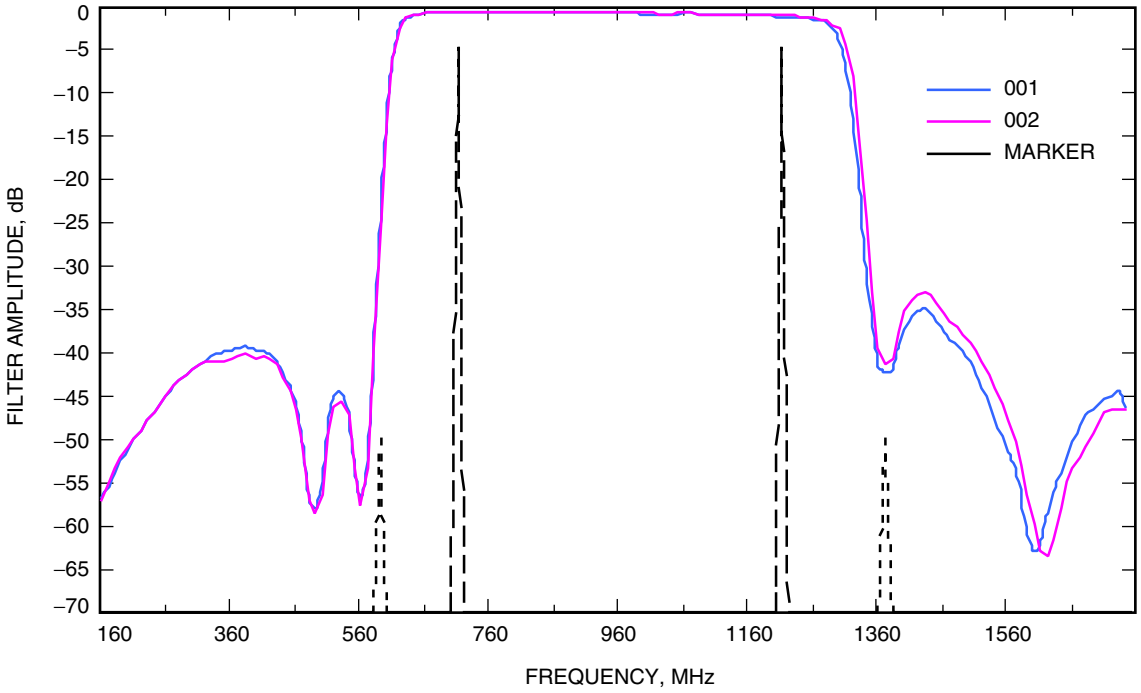

Fig. 3. Anti-alias filter amplitude response.

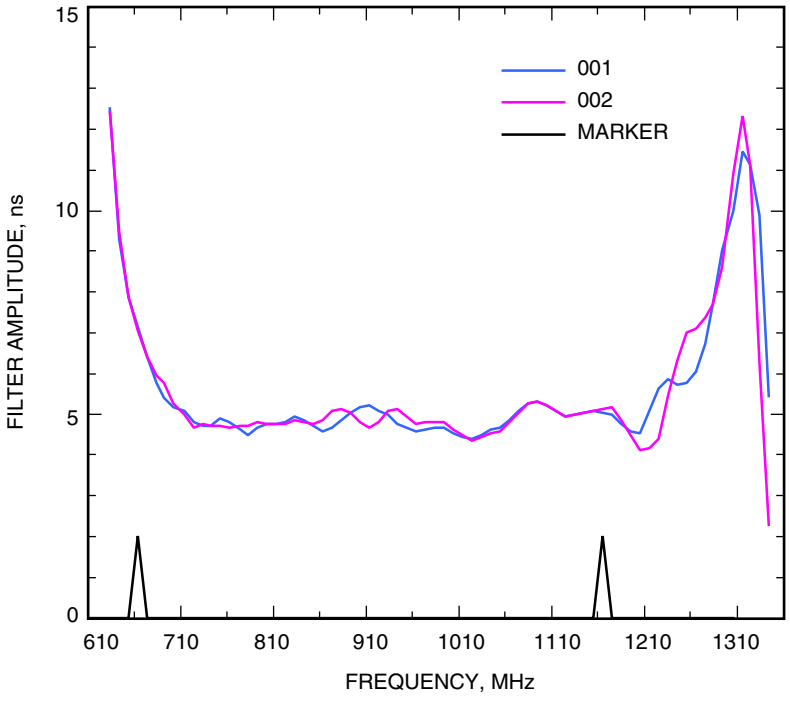

Fig. 4. Anti-alias filter group delay.

A. Beamsplitter and Beamformer

Figure 5 shows the connections between the beamsplitter, beamformer, and wideband correlator modules for a time-domain beamformer. Each beamsplitter produces four independent bandwidth signals for the beamformers and two wideband signals for each IF input for the wideband correlator. Each of the four independent beamformers can produce one phased-array signal of all the input antenna signals or up to four phased-array signals from smaller subsets of the input antenna signals. The maximum bandwidth of any beamformer signal is 128 MHz (sampling bandwidth), but a decimating filter in the beamsplitter can lower the bandwidth of any signal to as low as 125 kHz. The beamsplitter also makes two 512-MHz (sampling bandwidth) signals for use in two wideband correlators, one for each of the two antenna IF inputs.

A more detailed view of the beamsplitter module is seen in Fig. 6. A coarse integer delay line follows each IF input to correct for delays common to all signals in the beam of the antenna. Then, the four 125-kHz to 128-MHz signals can be chosen from either of the two IF inputs. A fixed-phase numerically controlled oscillator (NCO) picks the frequency band of each signal and changes the signal from real to complex. Then the signal is downsampled with a decimating finite impulse response (FIR) filter that

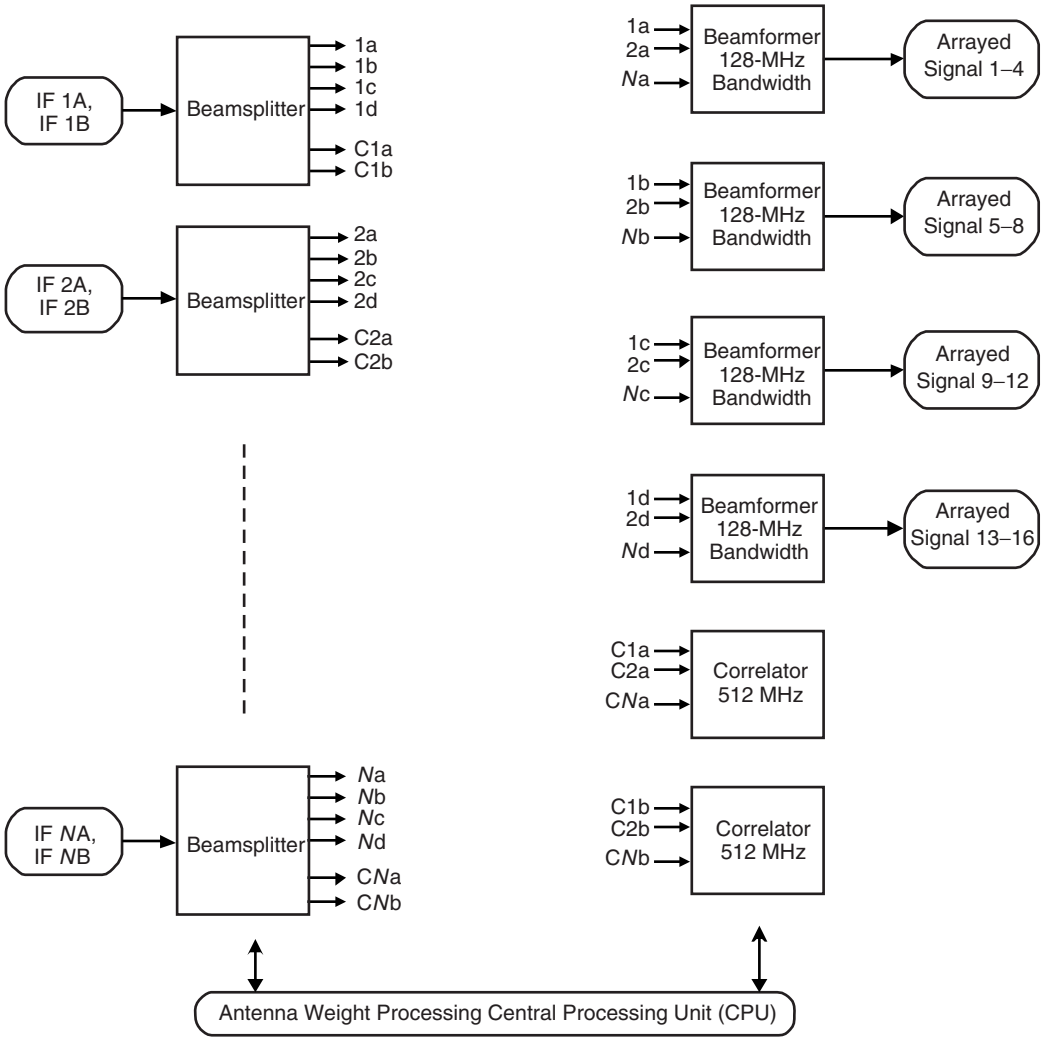

Fig. 5. Beamsplitter-to-beamformer connections for the time-domain beamformer.

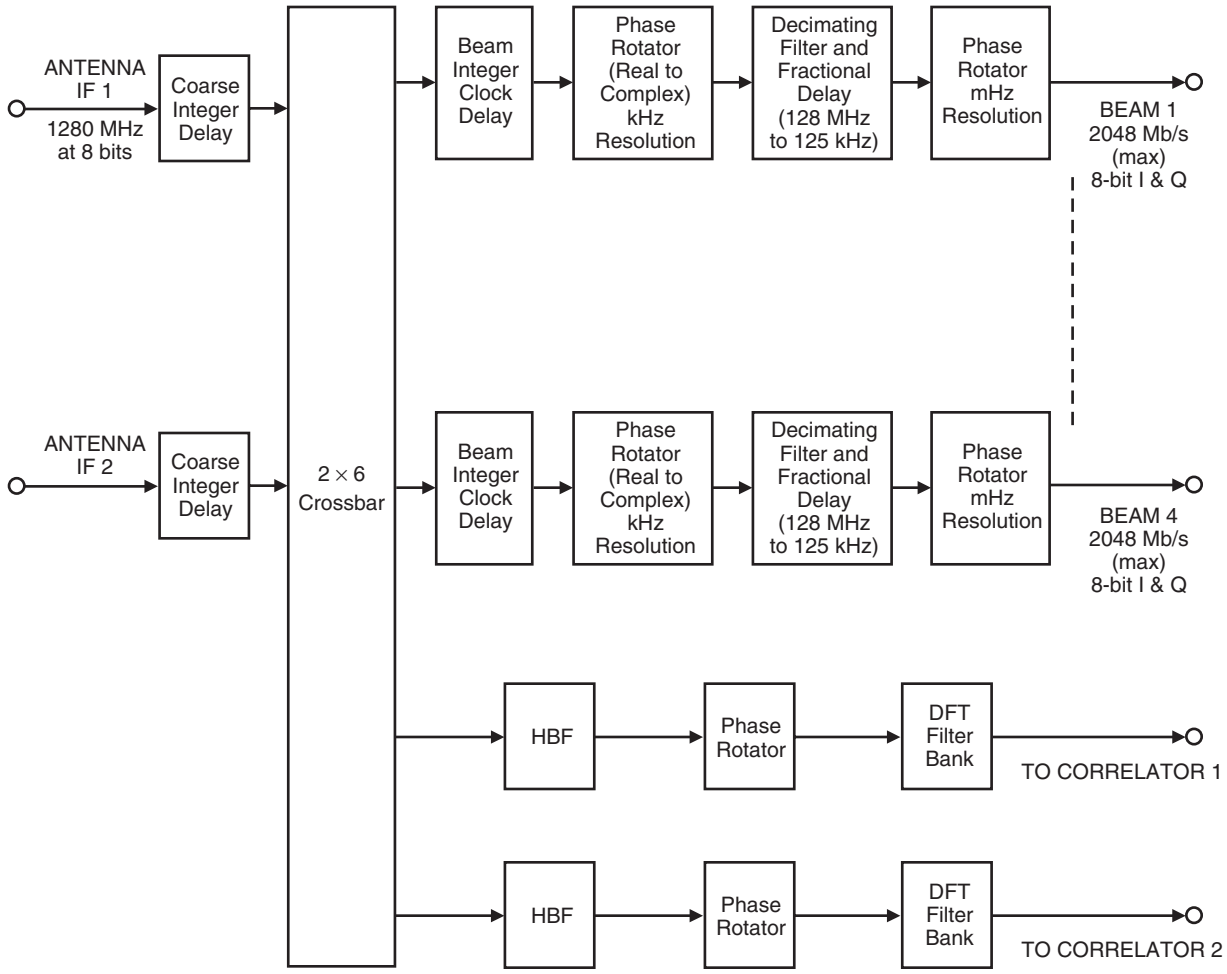

Fig. 6. Beamsplitter for the time-domain beamformer.

selects the bandwidth of each particular signal. This decimating FIR filter may actually be a cascade of FIR filters that can also implement the fractional sample delay. The fractional sample delay is necessary because, for a 128-MHz bandwidth signal with 1/2 clock cycle error in delay, the phase error at the edges of the band will be greater than 15 deg. The plan is to implement fractional delay to get at least 16 times better delay resolution to control the phase error over the band to less than 1 deg. After the fractional sample delay, another NCO phase rotator will be used for fringe rotation of each signal as well as for applying the phase corrections sent from the antenna weight processing software that monitors and controls beamsplitters and beamformers.

The two signals going to the correlator will have slightly different processing. After the coarse digital delay, the data will be transformed from real to complex using a half-band filter (HBF). A fringe rotator will follow to apply phase and frequency corrections. Then the data will be passed through a filter bank to make the first part of an FX correlator.

The choice of arraying algorithm has a definite impact on the hardware costs for the array. The Galileo S-band (2.3-GHz) mission and the full-spectrum processor array subsystem both use an array algorithm known as SUMPLE. The SUMPLE algorithm is a modified form of the SIMPLE algorithm in which each antenna is correlated against a reference antenna in order to phase each antenna up with the reference antenna. In SUMPLE, each antenna is cross-correlated against the weighted sum of all the other antennas [1]. A main feature of this algorithm is that the correlation processing is proportional to N, the number

of antennas. This is in contrast to other arraying algorithms that require the full correlation matrix of all the pairwise signals to be formed. These methods use least squares or eigenvalue techniques to find the optimal weights, but require order N squared processing [2]. By using a SUMPLE approach to beamforming, the hardware costs of complex multipliers and high-speed signal interconnections are cut by a factor of $N/2$ in the beamformer modules.

The SUMPLE method is an iterative algorithm where the complex weights are started from an initial value, such as zero phase, and updated periodically based on the phases measured in the correlators. After a few iterations, assuming uncorrelated noise, the weights converge to a nearly constant set of phases that align the array. In Fig. 7, the digitized input from the antennas is given by $X_i(n)$, where n is updated at the sample rate of the signal being arrayed. The complex weights, w_i, are updated on a much longer time scale, usually on the order of once a second. The signals after the complex weights are applied, $Y_i(n)$, can be expressed as

$$Y_i(n) = w_i \left(\frac{n}{T} - 1\right) X_i(n) \tag{1}$$

where T is the update interval of the complex weights.

The SUMPLE algorithm requires that, for each antenna signal, a sum be formed of all the other antennas. This sum is given by

$$S_i(n) = Z(n) - Y_i(n) \tag{2}$$

where $Z(n)$ is the sum of all the antennas.

The complex weights are updated every interval T, using the following correlation:

$$w_i \left(\frac{n}{T}\right) = \sum_{l=n-T}^{n} Y_i^*(l) S_i(l) \tag{3}$$

An adder tree circuit will be used to combine antennas to form each phased-array signal (Fig. 8). Each arrayed sum will be output to a telemetry receiver either directly in digital form or through a digital-to-analog converter. In addition, the phased-array sums will be fed back to the SUMPLE correlation units to form the signals needed for the SUMPLE algorithm.

The correlation units (Fig. 9) will have their own phase rotators to move the harmonics and the carrier of the telemetry to baseband and will apply matched filters to maximize the SNR before correlation [3]. For weak narrowband signals, the matched filters can also contain multiple time-shifted copies of the filter in order to try to find the bit boundaries of the telemetry signals. The matched filters that provide the highest correlation SNR are presumed to be those on the bit boundary. By finding the bit boundaries, an additional 3 dB of SNR can be gained before the correlation process. By looking at the phase error of the correlation sums for the different frequency bands, a phase slope can be calculated that provides a measure of the delay error [4].

The beamformer is made up of the adder tree and SUMPLE correlation units. The adder tree handles all the antenna signal, but does rather simple processing, addition only. The computation-intensive correlation units handle only two signals, the antenna signal of interest and the sum of all the antenna signals. Because these two pieces of the beamformer are so different, the hardware likely will be distributed to two different kinds of circuit boards.

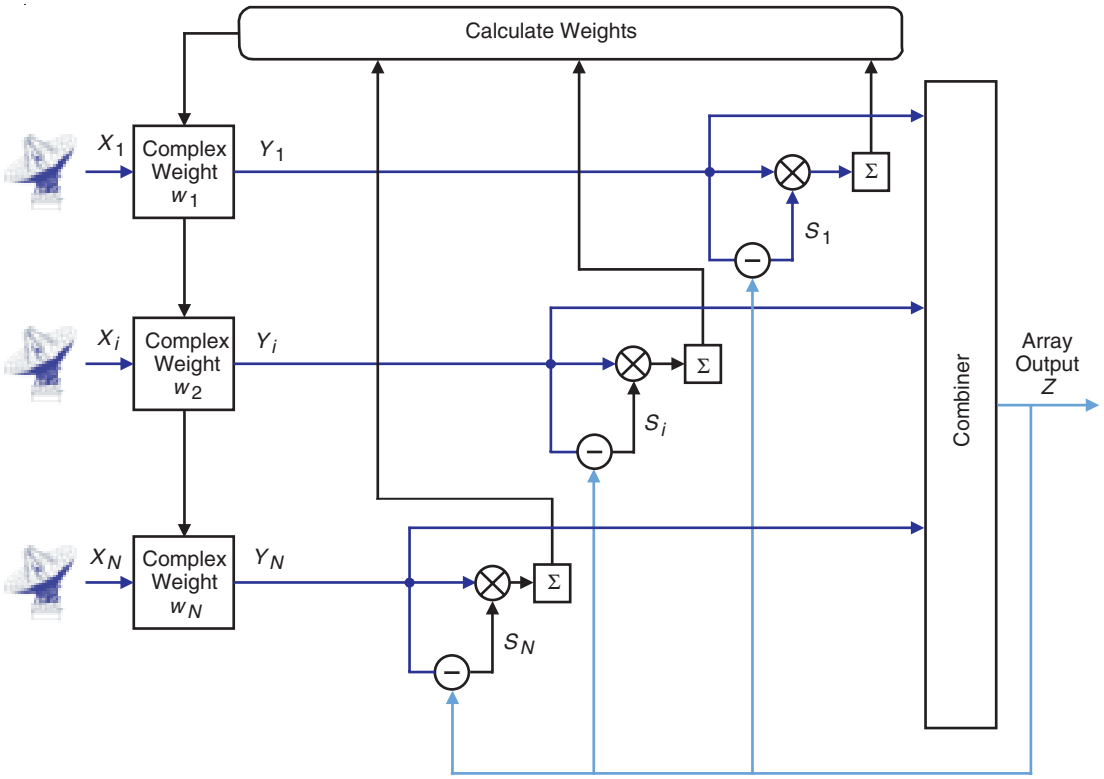

Fig. 7. Diagram of the SUMPLE algorithm for beamforming.

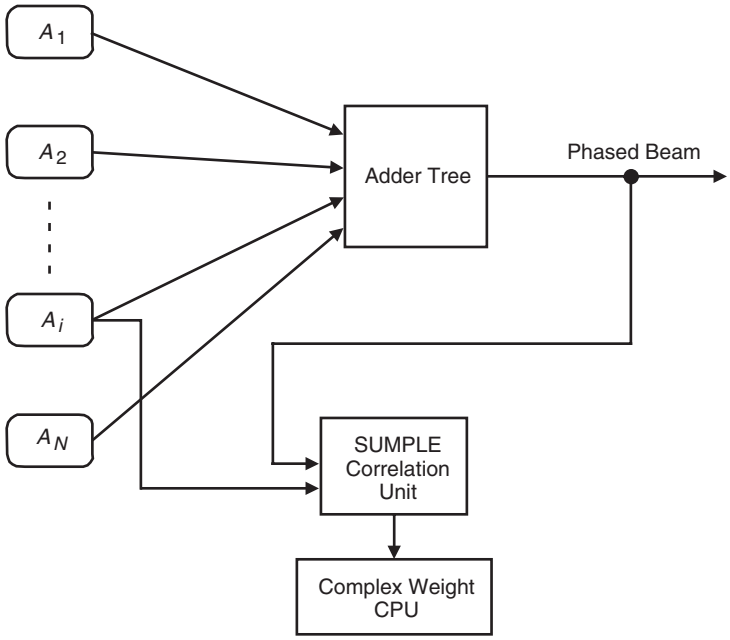

Fig. 8. Adder tree for the time-domain beamformer.

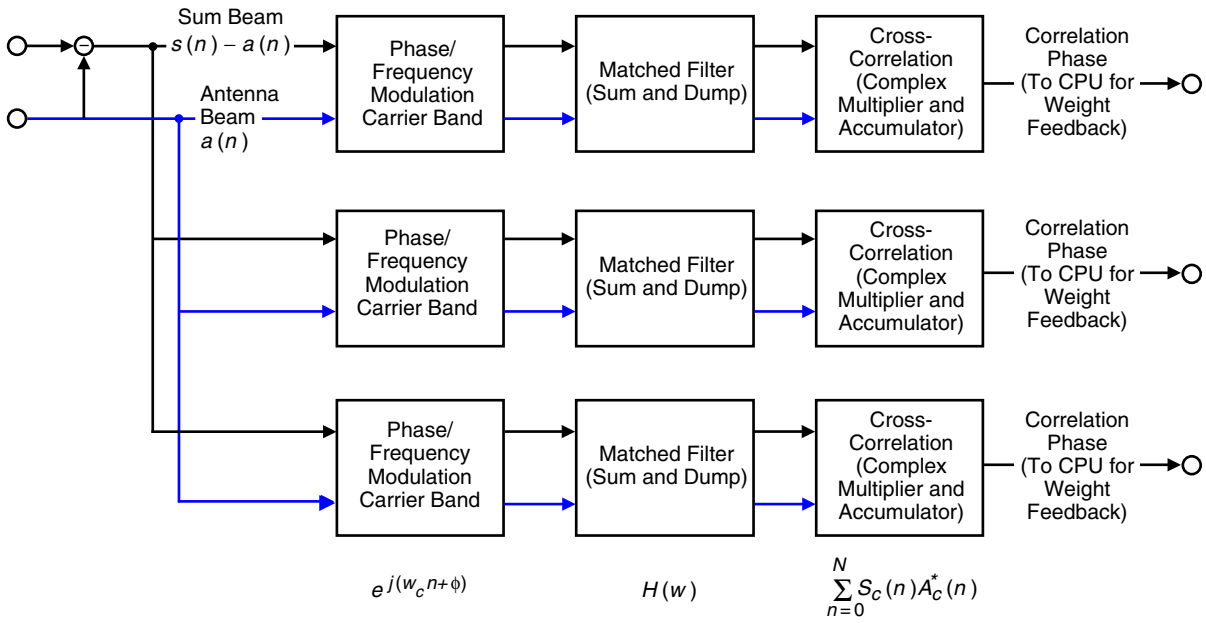

Fig. 9. SUMPLE correlation unit for the time-domain beamformer.

B. Wideband Correlator

The plan is to implement the wideband correlators using an FX architecture similar to those being designed for the Square Kilometer Array (SKA) and the Atacama Large Millimeter Array (ALMA). An FX correlator uses the fact that the cross-power spectrum of two signals is the Fourier transform of their cross-correlation. Thus, instead of using time lags to get the cross-correlation function, the cross-spectrum of the signals is determined by dividing them up into a number of frequency channels and cross-correlating each channel separately. One method many FX correlators use to form the frequency channels is to use a fast Fourier transform (FFT) as a filter bank. The FFT is a very efficient filter bank. Its main disadvantage is the poor filtering, a sinc filter, applied to each channel. The style of FX correlator used for the SKA and ALMA improves on the usual FFT filter bank by using a polyphase filter to implement a large windowing function before the FFT. Together, the polyphase filter and FFT form a discrete Fourier transform (DFT) filter bank. The polyphase filter combines with the FFT to provide a much flatter amplitude response than the traditional sinc function response of an FFT-only filter bank [5].

Figure 10 shows the filter-bank processing for the wideband correlator of the time-domain beamformer of the DSAN. If only an FFT filter bank were used, then a channel output, $X_k(m)$, would be given by

$$X_k(m) = \sum_{n=0}^{M} x(n + mM)e^{-j2\pi kn/M} \tag{4}$$

By using the polyphase filter in front of the FFT, the channel output becomes

$$X_k(m) = \sum_{n=0}^{M} \left[\sum_{r=0}^{Q} h\big(n + (m-r)M\big)x\big(n + (m-r)M\big) \right] e^{-j2\pi kn/M} \tag{5}$$

and the polyphase filters are related to the windowing function, $h(n)$, by

$$p_p(m) = h(p + mM) \tag{6}$$

The two correlator units will receive DFT filter-bank data from the beamsplitters. In order to minimize the number of interconnections in the correlator, the data from all the antennas will be gathered together and transposed so that each data stream will consist of all the antennas for a particular frequency channel instead of all the frequency channels for a given antenna, as shown in Fig. 11. This operation is known as a data router or corner turner, and its main advantage is that the data for all the baselines in a given frequency channel are gathered together. This facilitates the formation of all the cross-correlation baselines for that channel [6]. Basically, one can think of the corner turner as performing the matrix transpose of a block of data. Also, it reduces the interconnections for an N antenna full-baseline correlator from order N-squared to order N.

Once the data have been rearranged in the data router, each stream of antenna data for a given frequency can be correlated independently. Figure 12 shows an architecture for processing the serial stream of antenna data. The antenna data will be read into two dual-port register files or data buffers so that data can be written in and read out in any order. A buffer address control unit will cycle through the

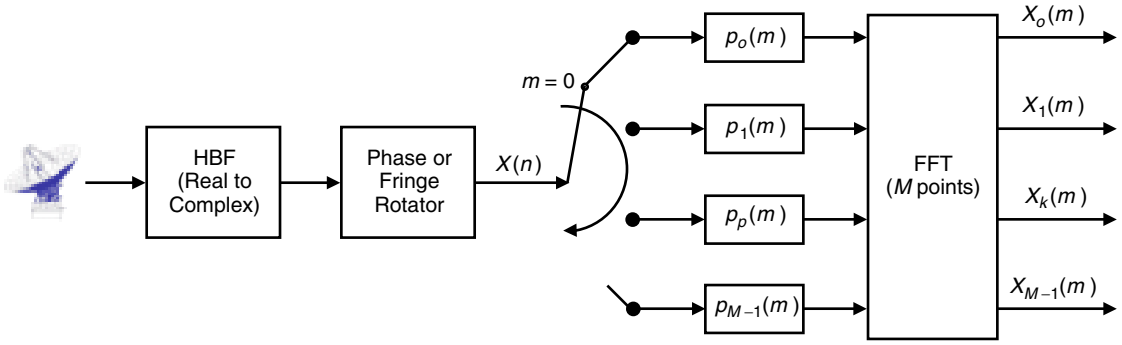

Fig. 10. FX correlator filter-bank processing.

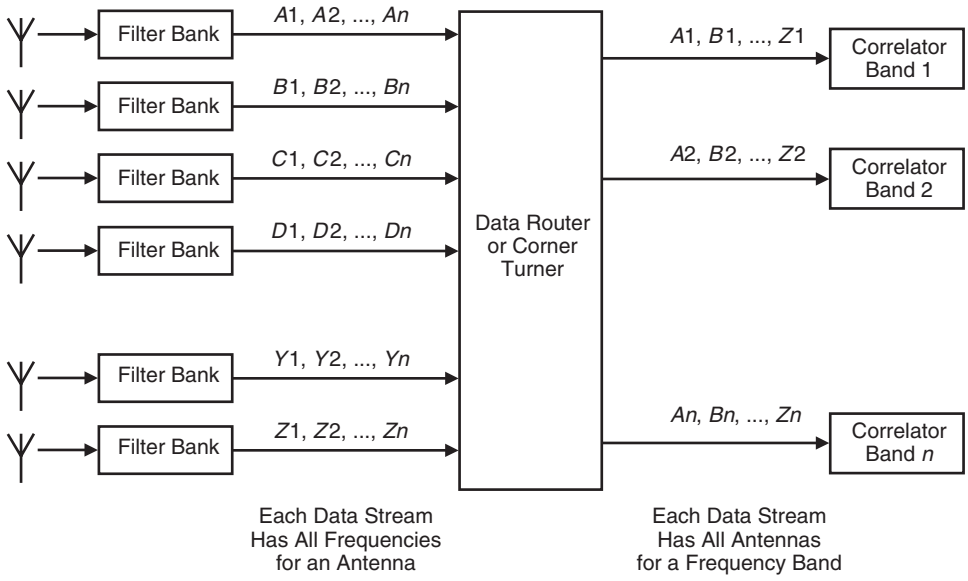

Fig. 11. FX correlator architecture using a corner turner.

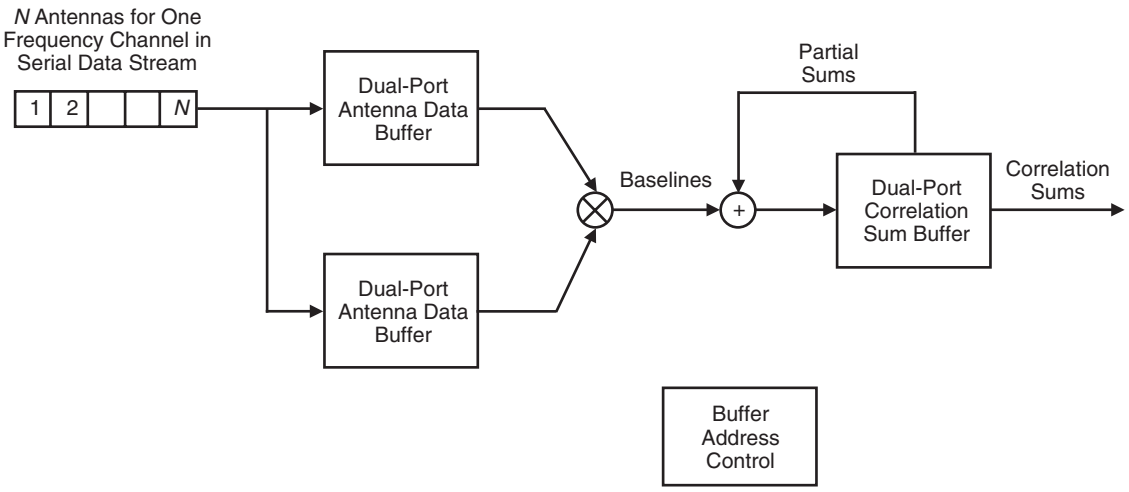

Fig. 12. Correlator for one frequency band.

addresses for all the different antennas in order to form all the pairwise combinations for cross-correlation. This same buffer address control unit will access a buffer with partial correlation sums to feed back into an accumulator. Completed correlation sums can be sent to a microprocessor for further processing and storage.

V. Integrated Frequency-Domain Beamformer

Another way to do beamforming is to break up the signal into different frequency channels and analyze each frequency channel separately to obtain phase and delay feedback information. Each frequency channel is independently combined to form a phased-array signal for that frequency channel, and then all the frequency channels in a specified bandwidth are synthesized back into one signal in the time domain. While there is some additional processing necessary to break up the data into separate frequency channels and put the data back together again, this method opens up new options for processing the data and allows very efficient use of available bandwidth. Also, as will be seen, the structure of this frequency-domain beamformer is very similar to an FX correlator, and the data path of the two structures can be shared and combined.[4]

A very efficient way to break time-domain data into separate frequency channels is the discrete Fourier transform (DFT) filter bank. Figure 13 shows a diagram of such a filter bank [7]. The analyzer uses complex modulators to move equally spaced frequency bands to baseband, and the analysis filter, which is the same for each downconverted band, filters out signals outside that band. The decimator reduces the sampling rate of the band-limited signal. In the synthesis portion, the data are upsampled again, and the synthesis filter eliminates the images generated by the upsampling. At this point, the frequency channels can be added back together to obtain the original signal.

The computations necessary for this DFT filter bank can be greatly reduced by using two constructs, the polyphase FIR filter and the FFT. This representation of the DFT can be obtained by transposing the order of operations for the analyzer and synthesizer, as seen in Fig. 14.

The main design criteria for DFT filter banks are the decimation rate used for the individual frequency channels and the design of the analysis, $h(n)$, and synthesis, $f(n)$, filters. Using oversampling by a factor

[4] J. D. Bunton, *CSIRO Support for DSN Large Array Study*, Work Package 3, Overall Systems Design & Electronics, Commercial-in-Confidence Report to JPL (internal document), Commonwealth Scientific & Industrial Research Organization, Sydney, Australia, January 2004.

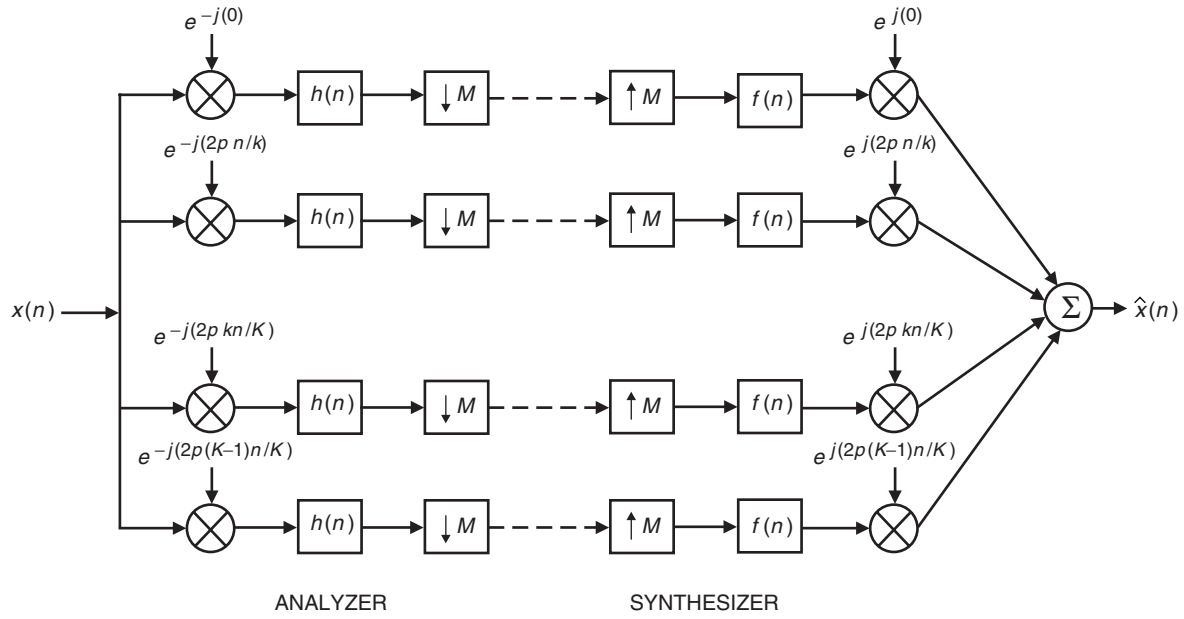

Fig. 13. Basic DFT filter bank.

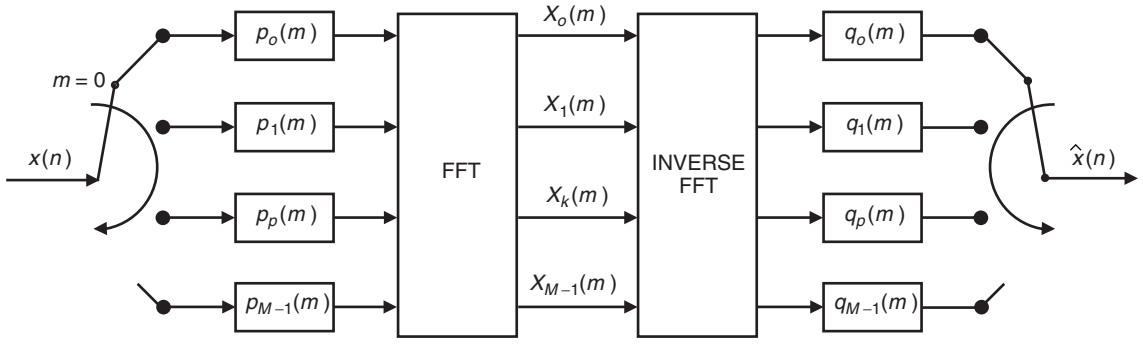

Fig. 14. DFT filter bank using polyphase filters and the FFT.

of 1.2 to 1.5 and identical analysis and synthesis FIR filters with a square-root raised-cosine characteristic, the combination of the two filters gives an approximately power-complementary response that is flat over the entire band of frequency channels [8]. Simulations with Matlab have shown that for a 512-channel filter bank an acceptable prototypical FIR filter for analysis and synthesis can be made from 6144 coefficients with oversampling of 1.5 and from 10,240 coefficients with 1.2 oversampling.

The first part of the DFT filter bank, the analyzer filter bank, is exactly what is required for the first part of an FX correlator. If the correlator also forms the sums of the data for each frequency channel and then passes these sums to synthesis filter banks, then we have an architecture for a frequency-domain beamformer that combines beamforming with an FX correlator, as shown in Fig. 15.

Each beamsplitter/filter bank first takes both IF signals and feeds them through a digital delay line. The delay lines can implement delays to a precision of 0.781 ns or one 1280-MHz clock cycle. After integer delay, the data will be converted into complex data and downsampled by 2 via a half-band filter (HBF). To handle large fringe rate differences between antennas in an array, a numerically controlled oscillator

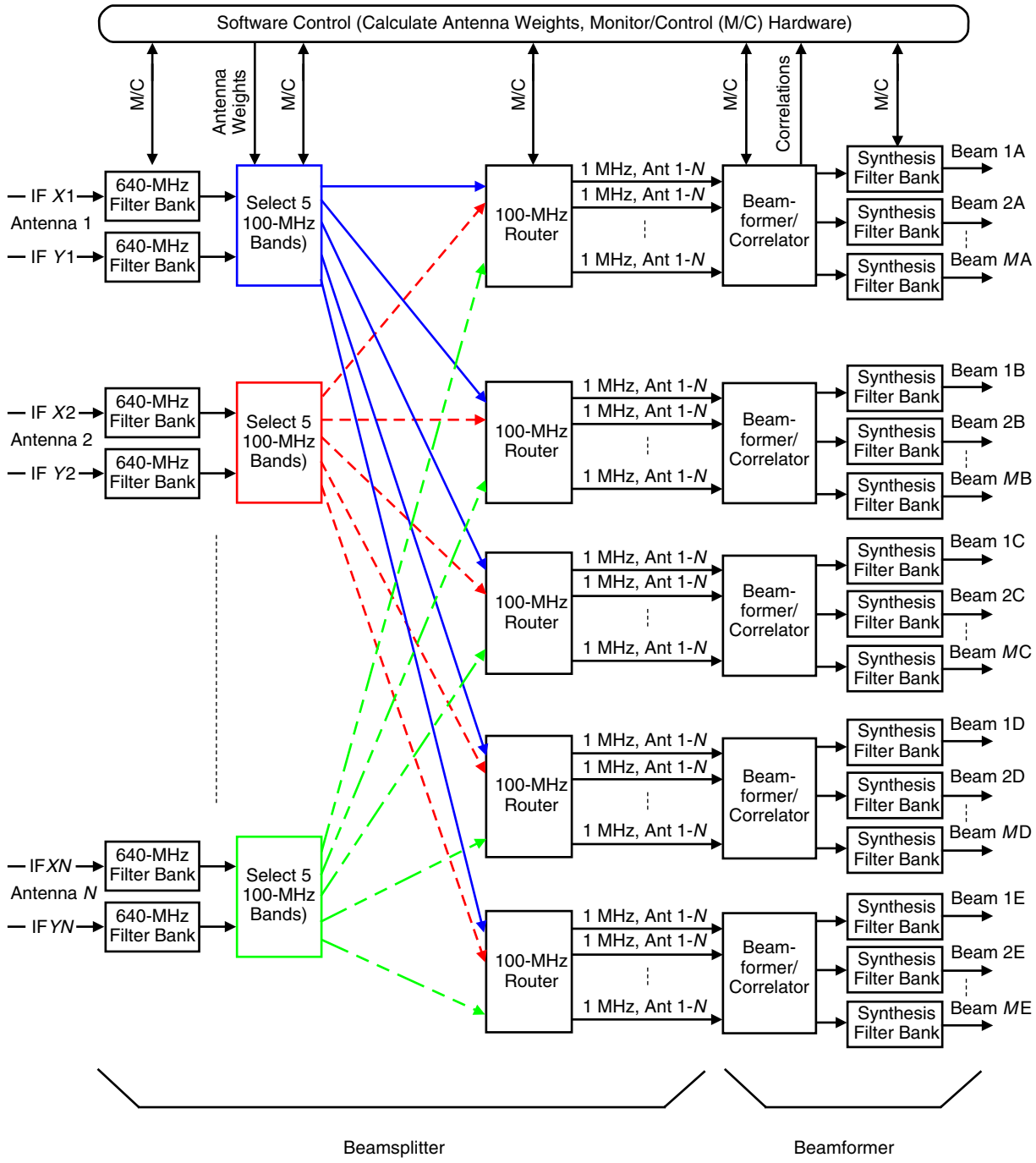

Fig. 15. Overall block diagram of the frequency-domain beamformer.

may be used after the HBF to rotate out large Doppler differences common to all received signals in a 12-m antenna beamwidth. The signals for each IF then will feed into their own polyphase filter bank. The filter bank will divide up the signal into between 256 and 1024 equally spaced frequency channels. Each of the channels will be slightly oversampled (by a factor of 1.2 to 1.5) to facilitate near-perfect re-synthesis of any contiguous section of the original bandwidth. One of the main advantages of the polyphase filter bank over a straightforward FFT filter bank is the approximately flat amplitude response of each frequency channel with only a small amount of oversampling. An FFT filter bank could achieve

similar results with windowing and an oversampling factor of 4 or more, but the cost of the hardware following the filter bank would be multiplied by the same amount.

These frequency channels then will be sent to five band-select multiplexers. Each band-select multiplexer will be able to choose either 100 MHz of bandwidth at 8 bits of in-phase data (I) and 8 bits of quadrature data (Q) or 200 MHz of bandwidth at 4 bits of I or 4 bits of Q. For very wideband signals, one could even support 2 bits of I and Q at 400 MHz. The five band-select multiplexers provide both redundancy and flexibility. If any one of the data routers or correlator modules following the band-select were to develop a problem, the data could be re-routed over to another band-select data router that had spare capacity.

The 100-MHz bandwidth capacity was chosen because, with a 1.2 oversampling rate and 16 bits worth of I and Q data, all the data can fit over a single 2.5-Gsps serial data link, simplifying the hardware implementation.

After the band-select multiplexers, phased-array beam-specific phase and fringe rate corrections can be made. Also, because the data are broken up in frequency, magnitude corrections for distortions in the passband shape can be applied. In addition, fractional 1280-MHz sample clock delay corrections can be made by adjusting the phase in each channel to approximate a phase slope across the band.

As in the FX correlator for the time-domain beamformer, a data router or corner turner is used to transpose the data from streams of frequency bands for each antenna into streams of antenna data for each frequency band. This data representation has a number of benefits. First, it eliminates the need for separate adder tree hardware in order to form the sum of all the antennas for an arrayed signal. Since the data for all the antennas for a frequency channel are present, the sum of the signals can be formed in the same place as the correlations. Second, since all the antenna signals are present in a frequency channel, many different types of correlations can be formed, including all the pairwise baselines and each signal against the sum of the other signals. This will allow other arraying algorithms that require all the pairwise correlations to be formed.

The beamformer/correlator module performs two functions. First, it combines many antenna signals to form a single arrayed signal for each frequency channel. Also, it cross-correlates the signals pairwise or each antenna signal against the sum of the other signals. In one mode, the beamformer/correlator can serve as a correlator only for a radio astronomy or antenna calibration function. In another mode, when it is keeping the array in phase, it could only calculate the correlation of each antenna signal with the sum of the other signals for a SUMPLE type of array algorithm. In this mode, the hardware can sum up all the data for SUMPLE, or all the baseline correlations can be sent to the software, and it can calculate the SUMPLE summations. To reduce the data bandwidth sent to the antenna weight processing software, it would be best to do the summations for a SUMPLE type of algorithm in hardware, even if all the baselines were available.

For narrow bandwidth signals (less than 1 MHz), the telemetry will be in one or two bands only. These narrow bandwidth type of signals can be passed through a second-stage polyphase filter bank [9] in order to better analyze them. Since the data for these small frequency channels is at a much lower sampling rate (a factor of 500 to 1000), the cost for these second-stage filter banks is much less.

For each frequency channel, a combined signal is produced at the output of the beamformer/correlator. These outputs are fed to a synthesis unit that has up to four synthesis polyphase filter banks. Each synthesis filter bank synthesizes the selected frequency channels into one signal in the time domain.

Each synthesis filter bank does about the same amount of processing as one input analysis filter bank, but at a lower maximum bandwidth. A synthesis filter bank will synthesize only up to a 100-MHz signal. Note that, if required, the output of multiple synthesis units from different correlator/beamformer units

could be synthesized into bandwidths of greater than 100 MHz, but there is currently no requirement for telemetry outputs greater than 100 MHz.

The output of each synthesis unit is a digital signal for a particular phased-array beam. This output can be sent over a digital link directly to a telemetry receiver or it can be converted back into an analog signal before going into the telemetry receiver. The current telemetry receivers of the DSN use an analog input with a center frequency of 200 MHz, and they accept an input noise bandwidth of 80 MHz. An analog output would provide the benefit of compatibility with existing systems but would add cost to the DSAN. An all-digital approach would have the next-generation telemetry receiver accept the direct digital output of the DSAN. This would save hardware costs in the telemetry receiver because it would not need its own analog-to-digital conversion circuitry. In addition, the signal-to-noise loss from the digital-to-analog and back-to-digital conversion could be eliminated.

VI. Conclusion

In this article, the basic signal processing architecture of a large array of antennas is described. The system is designed to handle both spacecraft signals and radio source signals up to a bandwidth of 500 MHz. The architecture chosen can be implemented using parts that are available today.

A time-domain approach to beamforming was described and has been demonstrated in the full-spectrum processor array currently installed in the DSN. This approach also requires a separate correlator for each IF that can form all the pairwise correlations over the full 500-MHz bandwidth. By using SUMPLE, an order N-type algorithm, in the beamformers, the cost of the hardware in the beamformers is minimized.

A new architecture for beamforming also is being considered. Because this approach first breaks up the signals into small frequency channels and combines the channels separately, it also can be used as an FX correlator. It adds synthesis filter banks to form output-combined signals at the bandwidths desired. The beamformers in this system are higher cost because they require $N^2/2$ complex multipliers as opposed to N complex multipliers for SUMPLE. However, no separate wideband correlator is required.

The frequency-domain approach to beamforming adds hardware and software design complexity as compared to the time-domain approach. In exchange, it adds flexibility to the use of bandwidth resources, and it allows arraying algorithms other than SUMPLE to be considered. These trade-offs currently are being evaluated. In addition, more work needs to be done on the frequency-domain approach to compare its performance with the time-domain approach.

Hardware is now being developed for a three-antenna test bed. It will be used to help further develop both arraying approaches as well as to test the new IF sampler. The lessons learned from this system will be used in designing the final system.

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