Development of a Multi-Channel Dielectric Resonator Oscillator for Space Communication Applications

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A novel multi-channel dielectric resonator oscillator (DRO) for Advanced Transponder use is developed for deep-space communication applications. The Advanced Transponder receives a 7.2-GHz (X-band) uplink signal and generates an 8.4-GHz (X-band) coherent or non-coherent downlink signal. The Advanced Transponder architecture incorporates two miniature DROs. These DROs are used in receiver and exciter frequency synthesis phase-locked loops (PLLs) in the Advanced Transponder. The DRO is capable of tuning over 27 Deep Space Network (DSN) X-band uplink channels (30 MHz). The DROs are designed with custom monolithic microwave integrated-circuit (MMIC) negative-resistance voltage-controlled oscillator chips. The receiver DRO design demonstrated a free-running single-sideband phase noise of -107 dBc/Hz at 100 kHz off the carrier frequency, a tuning linearity of ± 3 percent over the channel locking range, and output power of $+10$ dBm $\pm$ 1 dB.

Advantages of the multi-channel DRO include in-flight selection of transponder channel frequency, the enabling of novel mission operations techniques, frequency agility, and a single transponder design that will serve many missions and simplify hardware sparing strategies.

I. Introduction

This article summarizes the design and performance results of a multi-channel dielectric resonator oscillator (DRO) developed for Advanced Transponder application [1,2]. It provides significant improvement and flexibility over the current transponders for deep-space missions. The DROs are used in the 7.2-GHz (X-band) receiver local oscillator DRO phase-locked loop (PLL), 8.4-GHz (X-band) synthesizer DRO PLL, and 32-GHz (Ka-band) synthesizer DRO PLL. DROs are a desirable choice for microwave PLLs used in high-sensitivity receiver front ends. The high Q of the resonator provides a stable frequency, and the varactor in the coupling circuit provides the narrowband tuning and phase-locking capability. In addition, the DRO puck thermal coefficients can be selected to compensate for the device and cavity frequency drifts over the design temperature range of -55 deg C to $+75$ deg C.

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The current Advanced Transponder design requires a DRO circuit that is capable of both electronic tuning over a wider multi-channel bandwidth and phase locking within the channel capabilities. The deep-space X-band uplink and downlink spectral allocations are approximately 50-MHz wide and are divided into 1.16-MHz-wide channels.

In the current Small Deep Space Transponder (SDST), NASA's primary deep-space transponder, DRO PLLs are used in the receiver and transmitter circuits. The free-running channel frequency is set by the DRO puck properties and its placement in the DRO circuit. The DRO must be modified and tested for each transponder that has a new channel assignment. This impacts the recurring cost of the transponder. With this new DRO used in the transponder, the mission can dynamically select a channel, and a single transponder design can serve many missions.

In our novel multi-channel DRO design, we added two orthogonal varactor circuits coupled to the dielectric resonator—one for coarse tuning and the channel-setting function and the other for fine in-channel phase locking. The DRO design and measured performance are discussed in Sections II and III, respectively.

II. Multi-Channel DRO Specification and Design

A. Multi-Channel DRO Design Specifications

The design specifications for the multi-channel DRO are given in Table 1. The DRO must be capable of generating receiver and exciter local oscillator frequencies around 7 GHz and 8.4 GHz. The design must provide a tuning range of ±25 MHz to cover the Deep Space Network (DSN) X-band channels,

Table 1. Multi-channel receiver/transmitter DRO specifications.

DRO parameter	Specification
X-band RF Frequency Range:	
X-band Receive DRO frequency range	7019 MHz to 7069 MHz
X-band transmit DRO frequency range	8400 MHz to 8450 MHz
Course electronic tuning range (receiver)	7039 MHz ± 25 MHz
Fine-tuning range (PLL capture range)	±2 MHz
Tuning linearity	±10% or better
Output power level	+10 dBm ± 1.0 dB
Free-running DRO SSB phase noise	< -45 dBc/Hz at 1 kHz off carrier < -105 dBc/Hz at 100 kHz off carrier
Frequency stability versus temperature	±2 ppm/deg C maximum
Frequency pushing (±5% V_{dc})	100 kHz maximum
Frequency pulling (2:1 voltage standing wave ratio (VSWR) all phases)	100 kHz maximum
Harmonics	< -33 dBc
Spurious signals	< -80 dBc
Operating temperature range	−55 deg C to +75 deg C
Output impedance	$50 \pm 5\Omega$, nominal
DC bias current at +5 V DC	30 mA
Coarse electronic tuning control voltage	+3 V ± 2 V maximum
Fine-tuning control voltage	+3 V ± 2 V maximum

good phase-noise stability of less than −105 dBc/Hz at 100 kHz off the carrier frequency, and a buffered output of approximately +10 dBm at low DC power consumption. The tolerance on the tuning linearity is ±10 percent. The design approach utilizes a custom-designed GaAs microwave monolithic integrated-circuit (MMIC) negative-resistance oscillator in a DRO compact package.

B. Multi-Channel DRO Design

The schematic for the hybrid X-band receiver DRO [2] is shown in Fig. 1. The desired operating frequency of the receiver DRO is from 7020 MHz to 7080 MHz. The circuit is implemented on a 0.635-mm- (25-mil)-thick alumina substrate, as shown in Fig. 2. A photograph of the DRO is shown in Fig. 3. It consists of a negative-resistance voltage-controlled oscillator (VCO) MMIC and two GaAs varactors. The DRO layout size is 17.8 mm × 17.8 mm, and the cavity height is 8.9 mm. The enclosure box size is 24.2 mm × 24.2 mm × 15.3 mm. The DRO puck diameter is 8.89 mm, and its height is 4.01 mm.

The Hittite Microwave Co. developed the negative-resistance VCO MMIC, under contract with the NASA Small Business Innovation Research (SBIR) Program. The VCO MMIC chip incorporates a negative-resistance oscillator along with a buffer amplifier. The metal semiconductor field effect transistor (MESFET) used in this application is a standard 0.5-μm depletion-mode MESFET from TriQuint's analog MMIC process, HA2. This VCO was simulated using computer-aided design (CAD) tools to have large negative resistance over the frequency range of 7 GHz to 8.5 GHz. Two design and fabrication iterations were used to optimize the performance of the VCO chips. These negative-resistance VCO chips have previously been used by the Spacecraft Transponding Modem [2] Project to develop three different narrowband DRO designs operating at 7 GHz, 8 GHz, and 8.4 GHz .

As shown in Fig. 2, the DRO puck is coupled to a microstrip transmission line [3,4] feeding the negative-resistance port of the MMIC VCO. There are two varactor microstrip circuits coupling to the DRO. The microstrip lines are laid out orthogonally to each other. Each varactor microstrip line is DC-coupled to an external port using a microwave choke. The first varactor is used for coarse channel tuning, while the second varactor is used for fine tuning and as the feedback port for the phase-locked loop. There are 47 DSN channels, each with a bandwidth of 1.16 MHz. Therefore, the design objective was to provide approximately 50 MHz of channel tuning using a single coarse-tuning varactor, while the

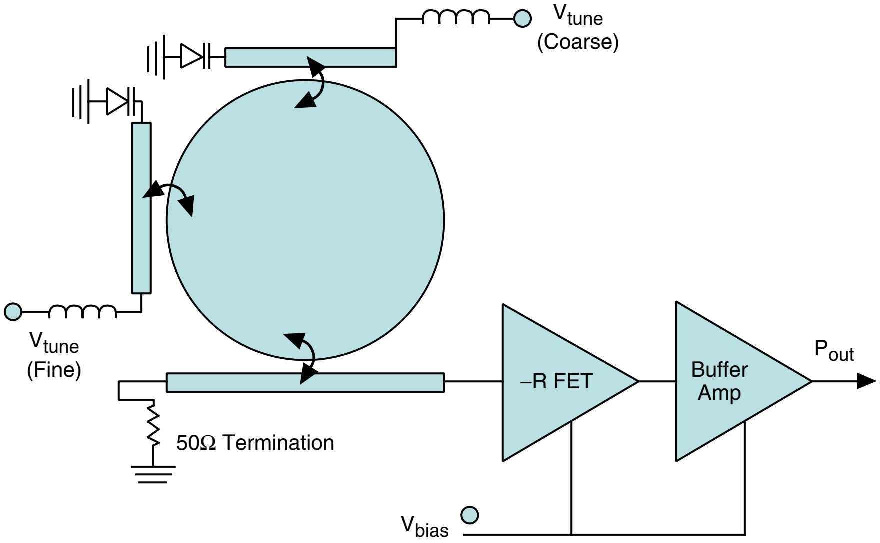

Fig. 1. Multi-channel dielectric resonator oscillator schematic.

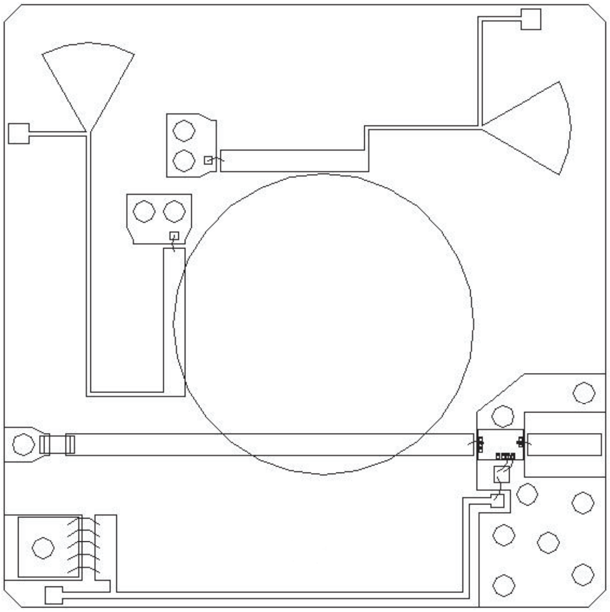

Fig. 2. Multi-channel DRO circuit layout on alumina.

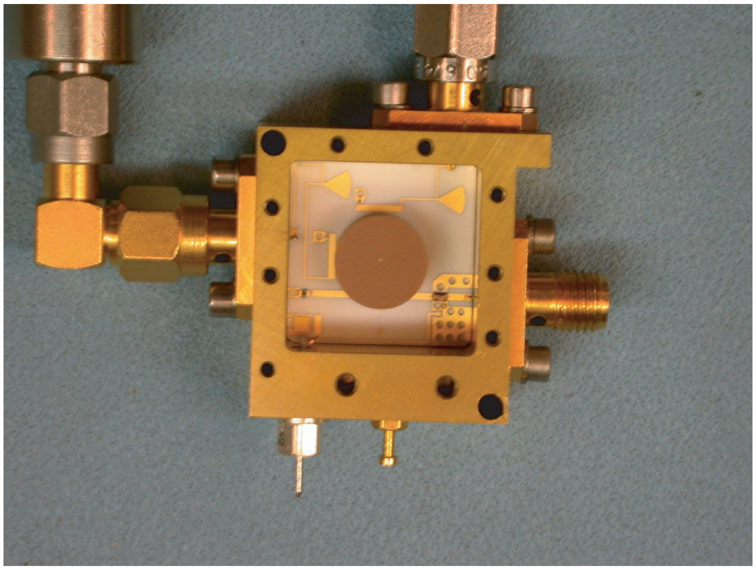

Fig. 3. Multi-channel DRO photograph.

second fine-tuning varactor is used to track the DRO PLL over 1.16 MHz. This added capability must not degrade the DRO performance requirements specified for the Advanced Transponder, as shown in Table 1.

III. Experimental Evaluation of the Multi-Channel DRO

The DRO puck, cavity height, and varactor coupling circuits, as shown in Figs. 2 and 3, determine the resonant frequency and overall tuning bandwidth. The placement of the dielectric puck was hand-tuned to optimize tuning bandwidth. The DRO puck is closer to the coarse-tuning varactor microstrip line for tighter coupling, and farther away from the fine-tuning varactor microstrip line for lighter coupling.

A metal tuning plate was used to mechanically adjust the DRO primary microwave resonant frequency to the DSN band center. The metal screw close to the DRO puck reduces the Q of the resonator and increases the tuning bandwidth. Since the substrate dimensions are held constant, the change in the microwave resonance is determined by the change in the cavity height from the alumina substrate to the metal tuner. As the spacing between the DRO puck and the metal tuner is decreased, the resonant frequency increases and the circuit Q drops, thus increasing electronic tuning bandwidth. The maximum spacing between the tuner and puck is 3.76 mm, and the tuner advances by 0.2 mm per turn. The mechanical tuning characteristic of the DRO is shown in Fig. 4. The achievable mechanical tuning range is from 6800 MHz to 7200 MHz. It was desirable to adjust the tuning screw as close to the puck as possible without decreasing performance of the DRO. The Q of the DRO puck is decreased from about 6000 to a value of about 200. This includes all of the influences of mechanical and electronic coupling circuits.

The maximum achievable electronic tuning bandwidth of this design is about 30 MHz. The DRO first is mechanically tuned to set the desired frequency within the band of interest, and then the coarse electronic tuner is used to select the desired channel. The fine-tuning varactor provides phase-locking capability within the channel. At the DSN band, the spacing between the metal tuner and the top surface of the DRO puck is 2.1 mm.

The DRO frequency-tuning characteristics as a function of coarse-tuning varactor bias at selected fine-tuning varactor bias conditions is illustrated in Fig. 5. The coarse-tuning curves have a similar transfer function and practically lie on each other for fine-tuning bias conditions of $V_{\text{fine}} = 0$ volt, $V_{\text{fine}} = -1$ volt, and $V_{\text{fine}} = -2$ volts. As shown, the maximum tuning range at any fixed fine-tuning varactor bias voltage is about 30 MHz.

Figures 6 through 8 show the measured channelization capability of the DRO for three different initial fine-tuning varactor voltage bias offset conditions: 0 volt, -1 volt, and -2 volts, respectively. These measurements also evaluate the PLL varactor capacitance effects on the DRO performance. The varactor capacitance is large and nonlinear at a 0-volt bias. As the bias is changed to -1 volt and -2 volts, the frequency tuning becomes more linear since change in the differential capacitance value is smaller. Figure 6 is for an initial 0-volt bias condition on both varactors. Since the total tuning bandwidth is approximately 30 MHz, the measurements begin at a frequency corresponding to a local oscillator for channel 10 of the

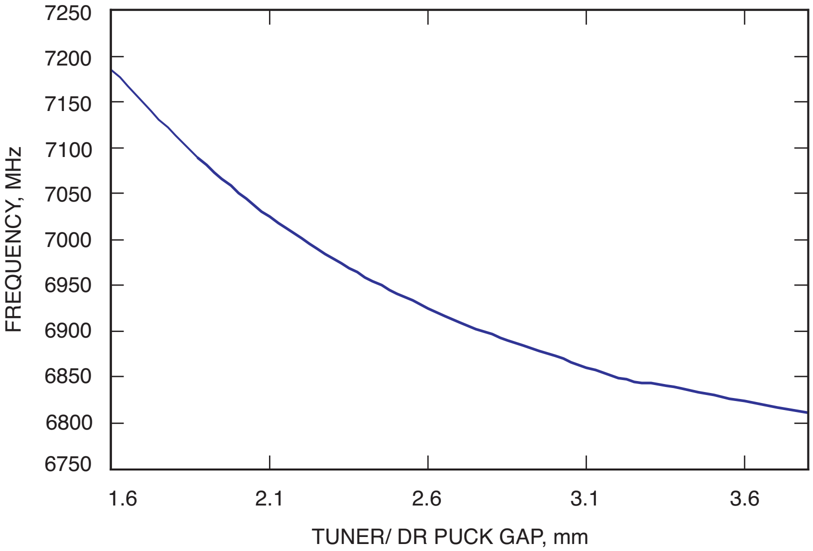

Fig. 4. DRO frequency tuning characteristic as a function of mechanical spacing between the tuning plate and the top of the dielectric puck.

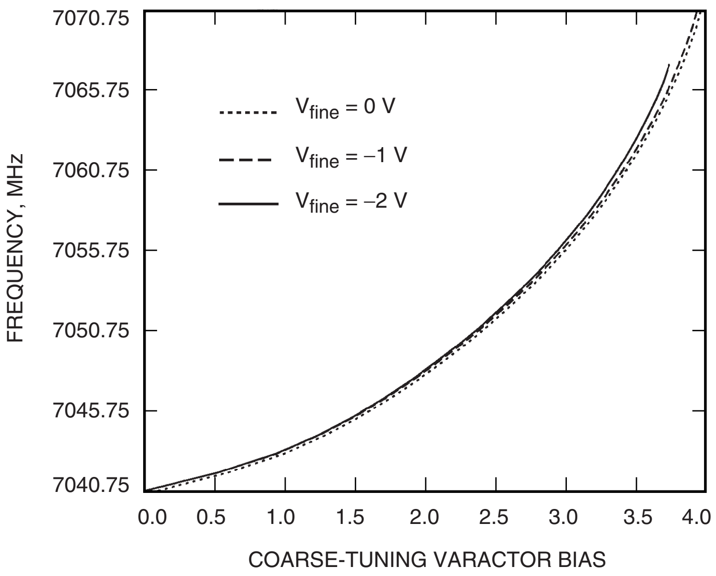

Fig. 5. DRO frequency versus coarse-tuning varactor bias in volts.

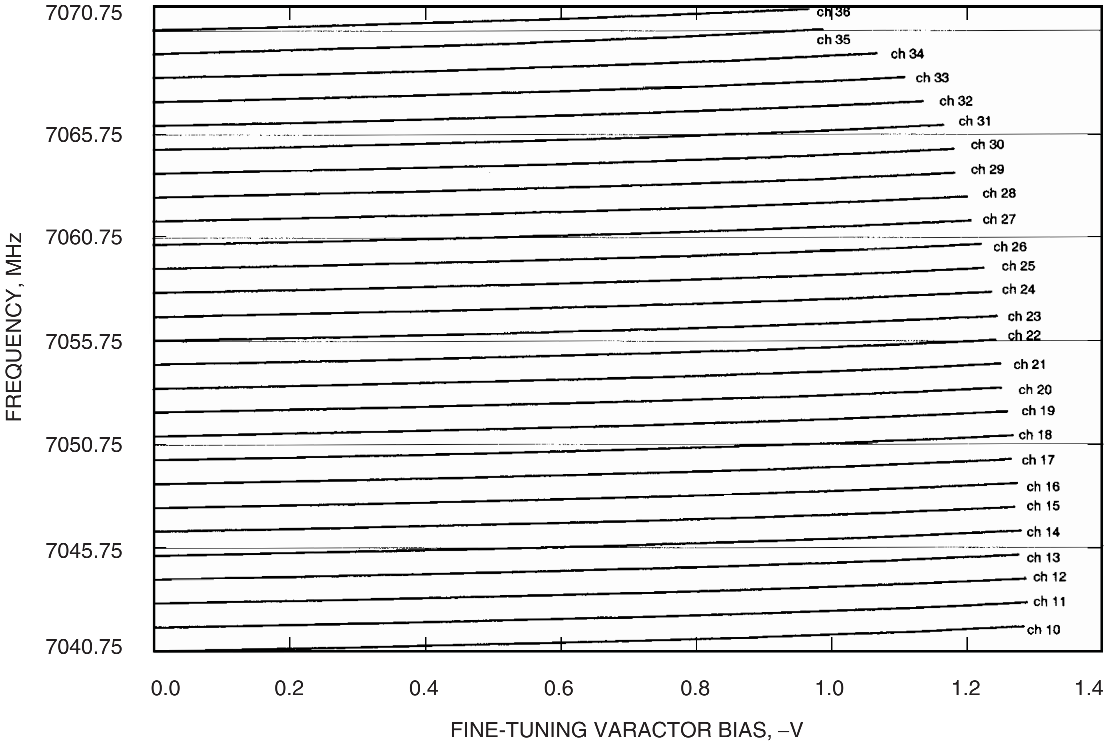

Fig. 6. DRO frequency versus loop filter varactor bias from 0 to −1.4 volts at different channels.

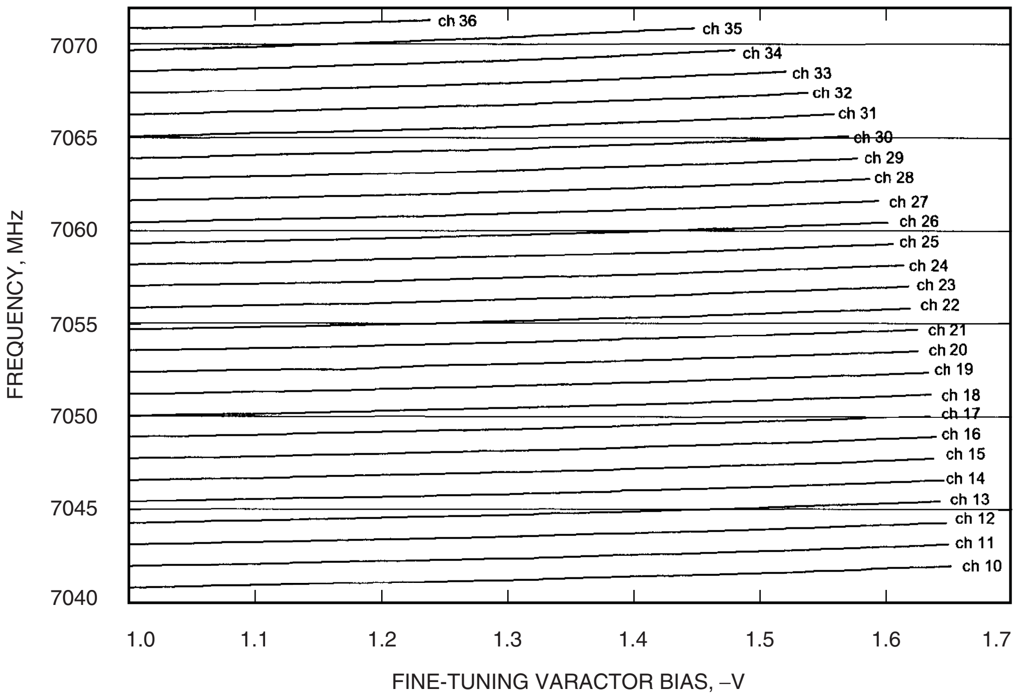

Fig. 7. DRO frequency versus fine-tuning varactor bias from –1 to –1.7 volts at different channels.

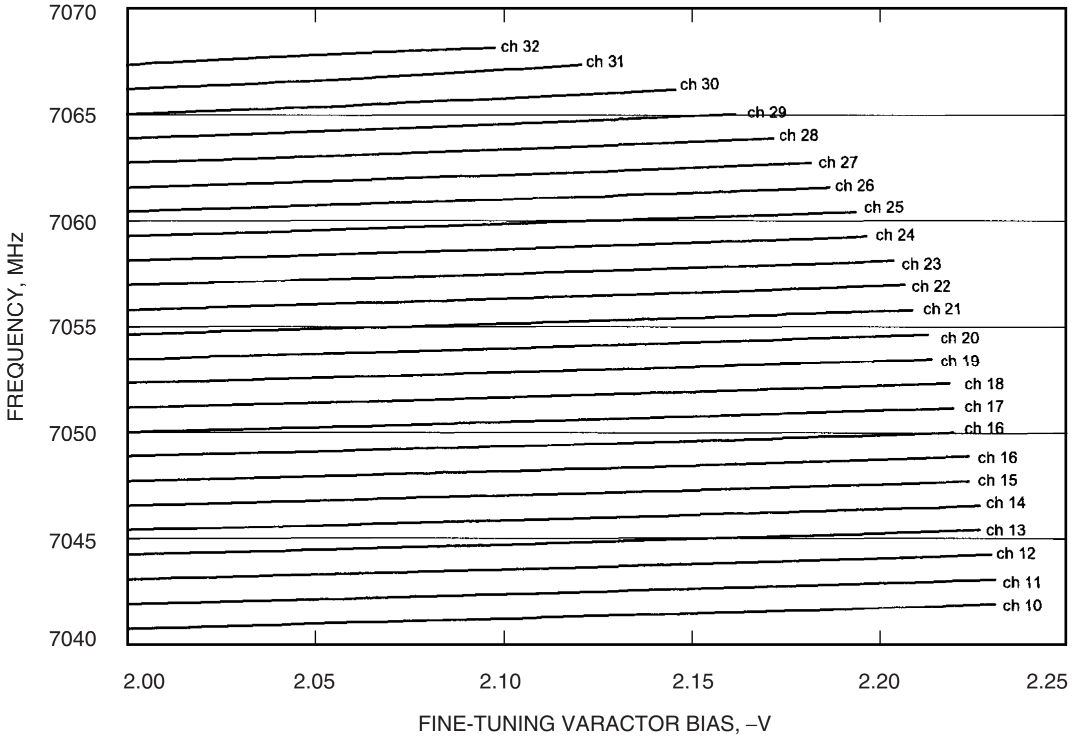

Fig. 8. DRO frequency versus loop filter varactor bias from –2 to –2.3 volts at different channels.

DSN X-band uplink band. (The Advanced Transponder architecture uses an intermediate frequency of approximately 116 MHz.) The DRO first was mechanically tuned to the DSN channel-10 frequency equal to 7040.76 MHz. This corresponds to the lowest uplink frequency of DSN channel 10. At this stage, both varactors were biased at 0 volts. The in-channel fine-tuning varactor was stepped up until the DRO output reached the highest frequency corresponding to channel 10 (7040.76 MHz + 1.16 MHz). The fine-tuning varactor then was returned to 0 volt, and the coarse-tuning varactor voltage was increased until the output frequency corresponded to the lower side of channel 11 (7041.92 MHz). This process was repeated through channel 36. At 0.70 MHz into channel 36, the DRO signal power dropped by 3 dB. The oscillator ceased to operate above channel 36. The DRO successfully tuned over a bandwidth of 30 MHz, corresponding to coverage of 27 out of 42 discrete DSN channels.

Figures 7 and 8 show the DRO output with the fine-tuning varactor biased at a −1 volt and −2 volt offset, respectively, at the beginning of each channel. Clearly the frequency response becomes more linear as the offset bias increases (in the negative direction). The DRO frequency response of the 0-volt bias offset has a maximum ±8 percent linear deviation over the 1.16-MHz channel. The −1 volt bias offset and −2 volt bias offset have ±5 percent and ±2.5 percent linear deviations, respectively. The improved tuning linearity also provides higher DRO sensitivity per channel as the channel number increased. The DRO sensitivity is the tuning effectiveness of the varactor, and it is the slope of the interpolated linear channel tuning characteristic curve, measured in MHz/V. For the 0-volt offset bias, the sensitivity at channel 10 is 0.896 MHz/V, and the sensitivity at channel 27 is 0.952 MHz/V. For the −2 volt offset bias, the sensitivity at channel 10 is 5.02 MHz/V, and the sensitivity at channel 27 is 6.15 MHz/V. At the 0-volt offset, the sensitivity changes by 6 percent, whereas the sensitivity changes by 26 percent at the −2 volt offset. All offset biases meet the specification of ±10 percent linear deviation.

The phase noise of the −1 volt bias offset DRO is shown in Fig. 9. The measured single-sideband (SSB) phase noise of the free-running DRO is −75 dBc/Hz at 10 kHz, and −107 dBc at 100 kHz off the carrier frequency with a 30-dB/decade slope. The measured phase-noise performance meets the

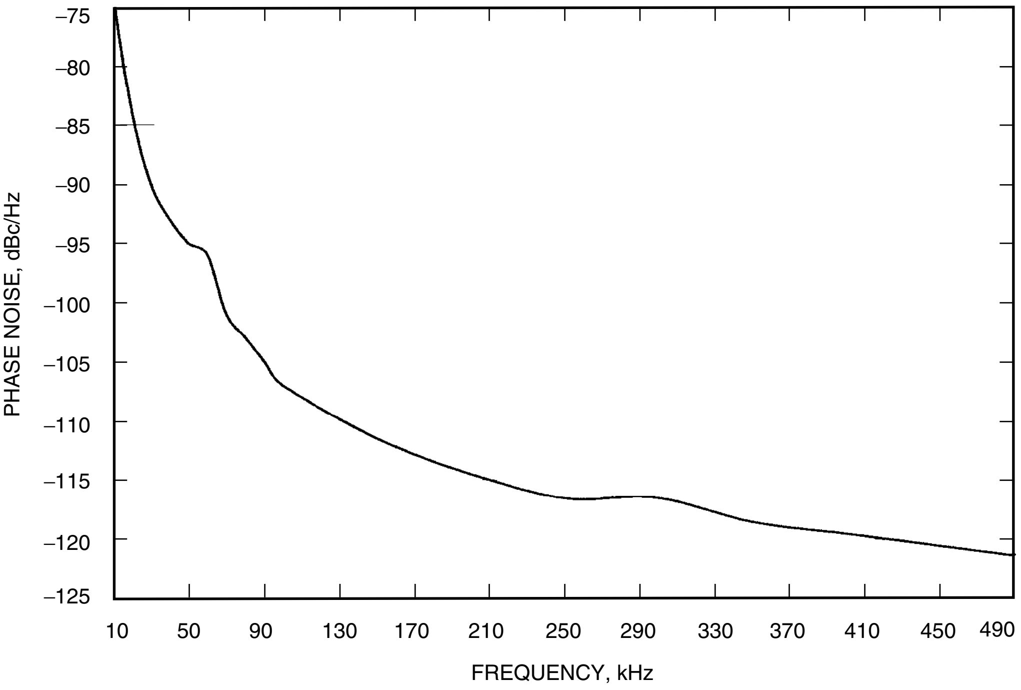

Fig. 9. Free-running DRO phase-noise characteristics.

transponder DRO specification shown in Table 1. Locked to a reference oscillator, the DRO measured a single-sideband phase noise of −117 dBc/Hz at 10 kHz away from the carrier.

IV. Conclusions

We have designed a novel X-band dielectric resonator oscillator that is capable of tuning over 30 MHz of the deep-space X-band spectrum. The DRO consists of a custom-designed negative-resistance MMIC oscillator, a dielectric resonator, and two orthogonal varactor coupling circuits. The circuit uses a 20-mil alumina substrate to lay out the orthogonal microstrip coupling circuits. The multi-channel DRO is capable of continuous tuning of 30 MHz over 27 deep-space X-band uplink receiver channels. The measured performance shows the DRO can be switched and phase locked to any one of these 27 channels. The measurements show excellent tuning linearity of ±2.5 percent and sensitivity of 6.15 MHz/V at a −2 volt bias offset voltage on the PLL varactor. The tuning linearity at a −1 volt bias offset is well within the ±10 percent requirement. The measured phase noise of the free-running DRO is −107 dBc/Hz at a 100 kHz offset from the carrier, which meets the phase-noise requirements.

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