A Ka-Band Wideband-Gap Solid-State Power Amplifier: Architecture Identification

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Millimeter-wave power-combining techniques are reviewed, and three architectures are chosen for further analyses. Although microstrip binary and serial combining are the most straightforward techniques to implement, they generally suffer from excessive circuit loss. To maximize combining efficiency, we therefore chose three architectures that use low-loss waveguide structures. The first architecture is based on non-resonant radial combiners and offers the greatest flexibility in the number of ports combined. It may be possible to combine up to 200 monolithic microwave integrated circuits (MMICs) with a combining efficiency >70 percent. The second architecture is based on a more conventional corporate combining design using a low-loss waveguide adder. Initial simulations indicate an insertion loss of 0.1 dB per adder, and greater than 30-dB port-to-port isolation may be possible. The third architecture is based on an oversized coaxial spatial combiner. Although all three architectures offer some flexibility, the approximate MMIC requirements are 1 to 4 W and >55 percent power-added efficiency. These power levels are on the upper range for gallium arsenide (GaAs) pseudomorphic high electron mobility transistor (pHEMT) technology, but are expected to be easily achieved with gallium nitride (GaN). The high efficiency, however, seems beyond the reach of GaAs and will require a focused research effort for GaN.

I. Introduction

A. Program Goals

The overall objective of this program is to investigate the feasibility of a solid-state alternative to the traveling-wave tube amplifier for space-based applications at 32 GHz (Ka-band). Performance goals of the target solid-state power amplifier (SSPA) are listed in Table 1. Assuming the output power can be achieved, the efficiency and reliability at both the component and system levels are of primary concern. The program will address both the underlying wideband-gap device/monolithic microwave integrated circuit (MMIC) technology and the overall amplifier. However, the current effort at JPL is focused more on the amplifier architecture, including the power-combining approach and amplifier topology.

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Table 1. SSPA end-of-life performance goals.

Parameter	Value	Note
Power output	120 to 150 W	—
Power-added efficiency	40 percent	At P_{1dB}
Band of operation	31 to 36 GHz	—
Bandwidth	10 percent	—
Gain	50 dB	—
Noise figure	<20 dB	—
Amplitude modulation/ phase modulation (AM/PM) conversion	<2 deg/dB	—
Phase ripple	<3 deg peak to peak	—
Input bus voltage	50 V ± 5 V	DC
Mass	<4 kg	Including electronic power conditioner (EPC)
Environment	Geosynchronous Earth orbit (GEO) or deep space	—

B. Purpose

This article presents the results of a survey of millimeter-wave power-combining techniques, and identifies several SSPA architecture options that can potentially achieve the performance goals in Table 1. To this end, an extensive literature search was conducted, and an electronic library of over 100 published articles, primarily addressing various power combiners and transitions structures, was compiled and reviewed. Limited analyses and design work also were carried out to validate the performance potential of chosen architectures.

C. Scope

This article is limited to identification of notional architectures at the overall SSPA level. MMIC design issues, including on-chip power-combining methods, are not assessed. Power-combining architectures were considered primarily on the basis of the number of MMICs that can be combined and the associated combining efficiency. Additional issues considered include mass, volume, heat dissipation, reliability implications, ease of fabrication, technology readiness, and extendability to higher frequencies. Information used is primarily from open literature and first-order calculations. Another article in this issue [18] and two articles to appear in the next issue of this publication will present results of detailed analyses and address device/MMIC issues in more detail. All performance parameters noted in this article should be taken as preliminary estimates until the more detailed analyses are performed.

II. Architecture Considerations: General Power Combining and MMIC Requirements

Although gallium nitride (GaN) is capable of relatively high power density (>2 W/mm [1] at Ka-band) compared to competing solid-state technologies, a large number of MMICs will need to be power-combined in order to meet the SSPA output power requirement given in Table 1. The challenging efficiency requirement also dictates that minimizing output combiner loss is critical. The power-combiner options should be flexible in the number of ports combined in order to accommodate the as-yet-unspecified power per MMIC. Port-to-port isolation also is highly desirable. Higher isolation between individual MMICs greatly improves the robustness of the amplifier by minimizing the risk of oscillations, making the amplifier more tolerant to amplitude and phase variations, and improving the graceful degradation

characteristics versus individual MMIC failures. Finally, the combining approach must allow easy integration of the input power divider and DC bias circuits and allow low-loss integration of MMICs with sufficient thermal path for effective heat dissipation.

For the targeted SSPA performance, Fig. 1 illustrates the first-order quantitative relationship between MMIC performance, the number of MMICs required, and the total combining loss. To determine a likely operating domain on these curves, it is necessary to make reasonable assumptions about the combiner and MMIC performance.

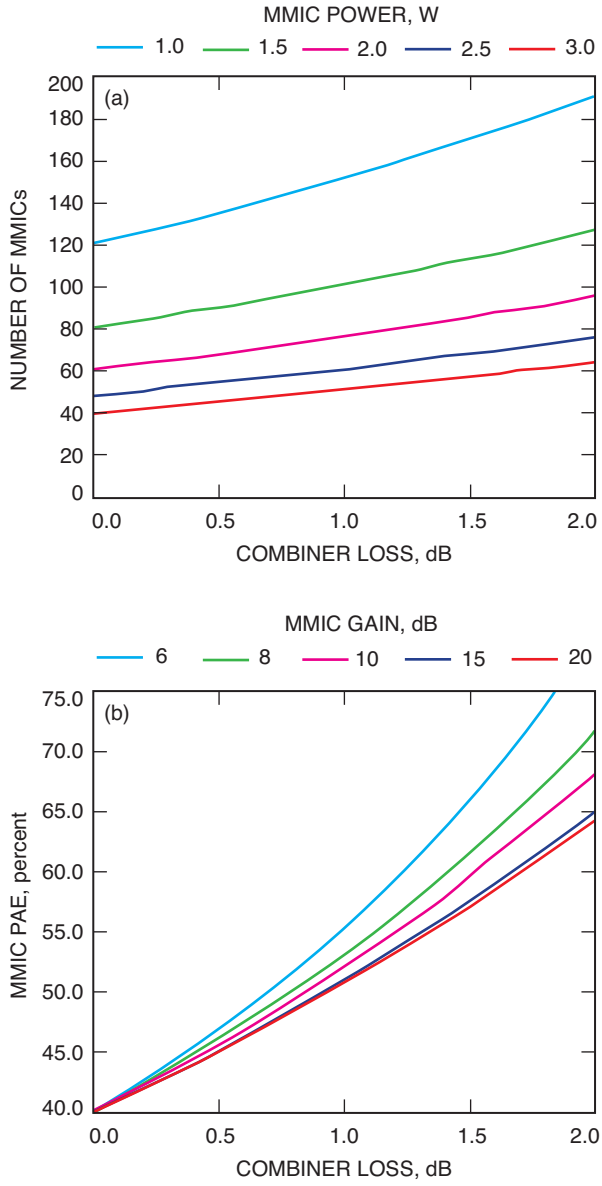


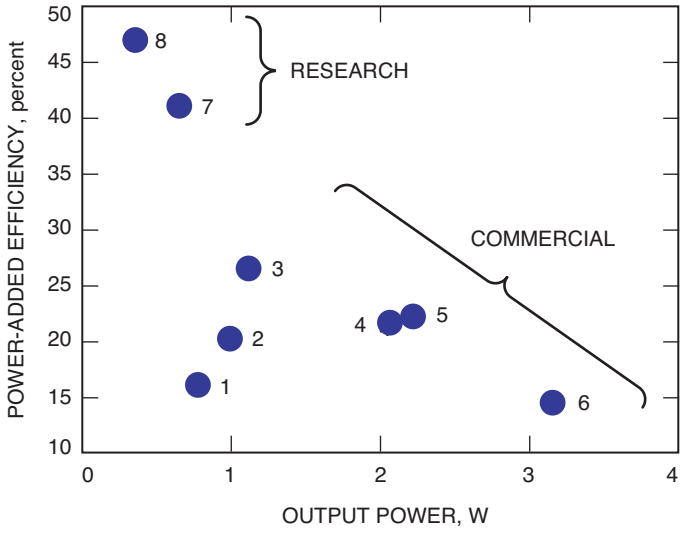
Fig. 1. The minimum (a) number of MMICs required to achieve 120-W output power as a function of total combining loss and (b) MMIC PAE required to achieve 40 percent PAE at the SSPA level as a function of total combining loss.

Given the high operating frequency, the MMIC-to-combining-circuit-transition loss, and the large number of MMICs required, it is unlikely that the total combiner loss will be less than about 0.75 dB. Depending on the actual number of combining ports and the combining method used, total loss in the range of 1.0 to 1.5 dB should be possible. This is equivalent to 70 to 80 percent combining efficiency.

If we assume a conservative MMIC gain of 10 dB, Fig. 1(b) indicates that a MMIC efficiency in the 50 to 60 percent range will nominally be required. For a given technology, lower-power MMICs in general are more efficient than larger ones. This is because smaller periphery devices have a lower quality factor (Q), are more easily terminated, suffer less from self-heating effects, and do not require lossy on-chip power combining [2]. Since external power-combining methods in general are more efficient than on-chip power combining, a solution employing a large number of low-power, high-efficiency MMICs may be preferable to a solution employing few, higher-power MMICs [3]. The more detailed analysis to follow this work should, for each chosen power-combining architecture, develop a MMIC-efficiency-versus-MMIC-power curve to define the minimum MMIC requirement for the given architecture. This curve will allow the MMIC designer to trade power versus efficiency at the MMIC level and to choose an optimum design while meeting the architecture requirements.

For further context, Fig. 2 illustrates the state-of-the-art performance of Ka-band power MMICs based on GaAs pseudomorphic high electron mobility transistor (pHEMT) technology. The highest efficiencies are achieved for <0.5-W MMICs with a corresponding device periphery of approximately 1 mm. With the same device periphery, GaN can deliver 2 to 3 W of output power. However, by employing smaller, 1- to 2-W-class devices and utilizing GaN's higher operating voltage and device impedance, it is conceivable that MMICs can be designed for sufficient power-added efficiency (PAE) to meet SSPA-level requirements. Higher voltage operation may reduce resistive losses, and higher output impedance of GaN devices may make proper termination for high-efficiency operation easier.

Referring back to Fig. 1, we note that, at the low end of the MMIC power range, approximately one hundred and fifty 1-W or seventy-five 2-W MMICs need to be power-combined to meet the minimum SSPA power goal. Even with a relatively larger 3-W MMIC, more than fifty MMICs will be required. This is well beyond the range of simple microstrip binary combining due to circuit losses.



1. Triquint TGA1172, 0.25-µm pHEMT, 0.33 W/mm
2. Fujitsu FMM5803X, 0.25-µm pHEMT
3. Triquint TGA4509, 0.25-µm pHEMT
4. Triquint TGA4513, 0.25-µm pHEMT
5. Raytheon RMPA29400, 0.1-µm pHEMT
6. Triquint TGA4505, 0.25-µm pHEMT, ~0.4 W/mm
7. Schellenberg 1996, 0.2-µm pHEMT, ~0.25 W/mm
8. Schellenberg 1998, 0.2-µm pHEMT, 0.4 W/mm

Fig. 2. State-of-the-art research and commercial Ka-band MMICs based on GaAs pHEMT.

III. Survey of Power Combiners

A. Overview

Overviews of microwave and millimeter-wave power-combining techniques have been presented by Russell [4] and Chang [5]. Major categories are illustrated in Fig. 3. Practical amplifiers typically employ a combination of these techniques at various levels, from the device to the MMIC, power module, and the complete SSPA.

At the device and MMIC levels, the designer is forced to use relatively lossy planar circuit technology, typically either microstrip or coplanar waveguide, to implement the power combiner. Examples of on-chip combiners include paralleled devices, impedance-transforming networks, and bus–bar combiners [6]. Larger combining structures such as Wilkinson and Lange couplers are practical only at millimeter-wave frequencies where circuit losses are higher. GaN's increased power density can greatly benefit the system design by significantly reducing the need for power combining at this level.

A large number of combining techniques are available at the circuit level. The designer also has a large selection of transmission line and cavity structures for implementing a given combiner. A coarse selection typically is made based on the required bandwidth and output power, i.e., the number of combining ports required. Final selection typically is made based on loss requirements and ease of fabrication.

Depending on the type, spatial combining can be considered a subset of chip-level and circuit-level combining or a hybrid of the two. This category of combiners and the various circuit-level combiners are discussed further in the following subsections. The category of combiners labeled "Other" in Fig. 3 includes more specialized techniques, such as dielectric waveguide-based combining. No techniques considered from this category were considered applicable to this program.

Resonant cavity combiners, particularly based on circular cavity, have been used extensively in the past to power combine a large number of impact ionization avalanche transit time (solid-state diodes) (IMPATT) devices [4]. Modified versions also can be used to power combine MMICs, making cavity combiners a possible candidate for this program. Although the required 10 percent bandwidth can be achieved, resonant structures are inherently narrowband and require more exact tolerances in fabrication. Moreover, the lack of isolation between combining ports eliminated resonant combiners from further consideration.

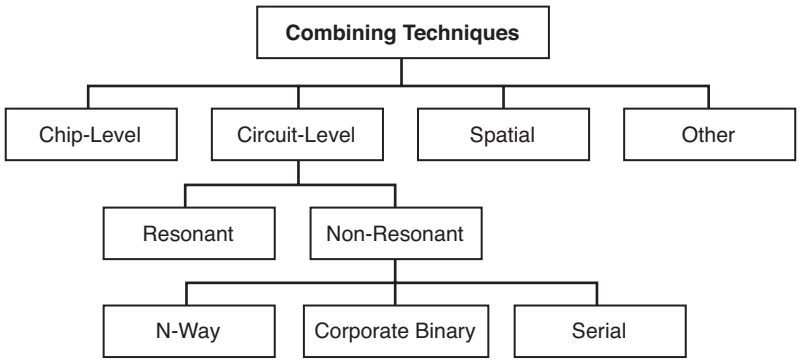


Fig. 3. Microwave and millimeter-wave power-combining techniques (adopted from [3]).

B. Corporate and Serial Combiners

Corporate and serial combiners, illustrated in Fig. 4, are widely used for combining a relatively small number of devices.

Couplers such as the in-phase Wilkinson and the quadrature Lange are used as two-way combining elements, or adders. The corporate combiner requires only one adder design while the serial combiner requires that the coupling value of the adder change at each junction. The serial combiner can, however, accommodate an arbitrary number of ports, while the corporate combiner requires that the number of ports be binary, i.e. 2^n.

The simple implementation of a microstrip binary combiner makes it an attractive option for use as the input power divider in an SSPA. Although losses in the input divider lower the SSPA gain, if the SSPA's output stage MMIC gain is greater than about 10 dB, the SSPA efficiency is not significantly affected. Multiple levels within a corporate structure also allow easy integration of driver MMICs and gain stages in a distributed manner. This helps to eliminate single-point failure modes and is a major advantage from an SSPA architecture point for view.

The key limitation for either corporate or serial combining, however, is circuit loss. As illustrated in Fig. 5, combining efficiency degrades quickly with the number of devices combined due to loss in the adder circuit. For implementation with planar transmission lines, additional losses of lines required for layout generally limit the number of combined ports to less than 16. As illustrated in Fig. 6, however, rectangular waveguide loss at Ka-band is over a factor of 30 less compared to that of microstrip. Implementation of a corporate structure in waveguide may be feasible for this program if a suitable low-loss adder with sufficient port-to-port isolation can be realized.

C. Spatial Combiners

Spatial combining is a broad category of combining techniques in which energy to be combined is not individually guided through single-mode transmission lines such as microstrip or waveguide. Power combining is achieved instead through the spatially distributed nature of energy in free space or in an overmoded waveguide. In a quasioptical plane-wave amplifier, for example, a large number of devices are integrated into an active antenna array [7,8]. Individual antenna elements provide circuit matching to the device, and the distributed nature of the array allows power combination essentially without any

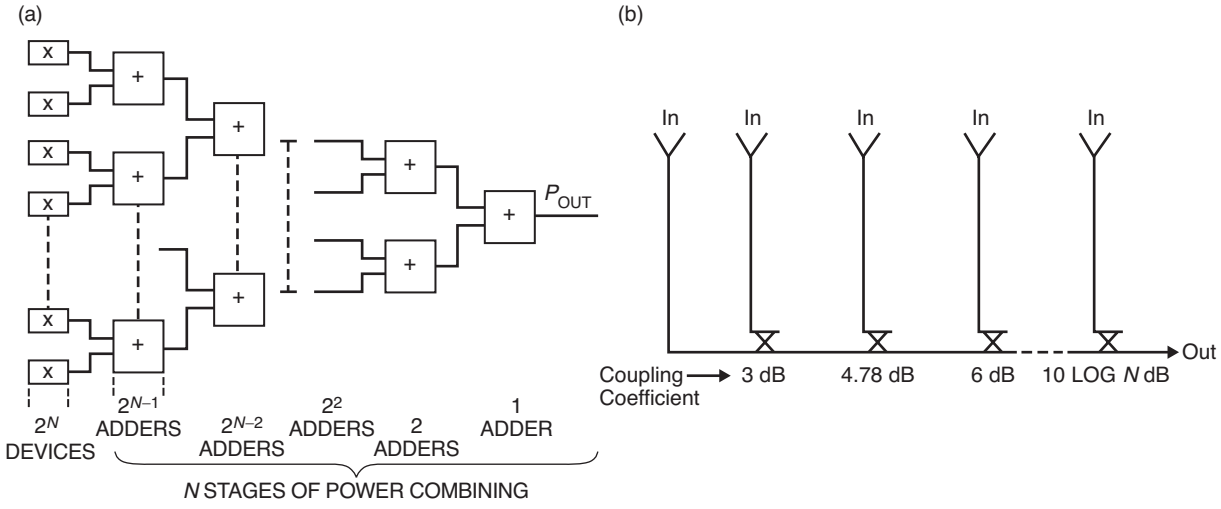


Fig. 4. Combining architectures: (a) corporate and (b) serial. From [4].

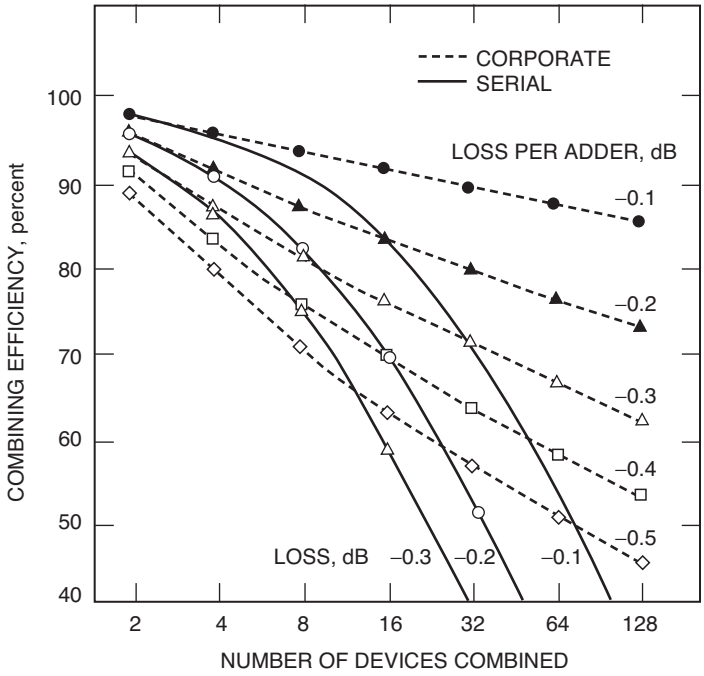


Fig. 5. Combining efficiency of binary corporate and serial combiners (from [4]). (Note that corporate combiner curves do not include significant additional losses due to lines required for layout. See Fig. 6.)

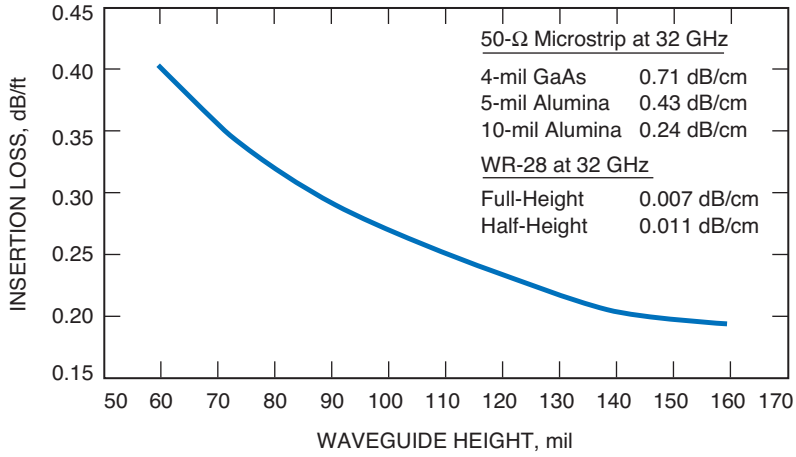


Fig. 6. Loss for WR-28 rectangular waveguide and 50-Ω microstrip at Ka-band. (HFSS simulation of WR-28 loss at 32 GHz; conductor = gold.)

circuit loss. For large arrays where the edge effects and spill-over losses can be ignored, the advantage of this approach is obvious. As illustrated in Fig. 7, the circuit loss in spatial combining is independent of the number of devices combined.

In practice, however, this approach has significant drawbacks in terms of complex design procedure, oscillation issues, and poor efficiency. Generally, there is not enough area in the unit cell of an antenna array at millimeter-wave frequencies for a multi-stage, high-efficiency amplifier design. For transmission-type plane-wave amplifiers, thermal design also becomes a limiting factor for increasing the array size. Finally, a single-stage design leads to a relatively low overall gain. This is a significant drawback since GaN device f_t (the frequency where the unilateral power gain of the device is equal to 1) generally is lower compared to competing technologies, and the available power gain at Ka-band is limited.

In a slightly different implementation of the combiner, the device is separated from the antenna element, and a multi-stage, optimized MMIC can be coupled to the antenna element instead. However, the spill-over loss and thermal considerations remain significant challenges. For these reasons, plane-wave quasioptical amplifier architectures will not be considered for this program.

In a related class of spatial combining, the active antenna array is placed in a hard horn that provides uniform illumination of the array and minimizes spill-over loss [10]. However, effective coupling between the hard horn and the array elements is difficult to achieve, and a complex design process is required. This, along with bandwidth limitations of the antenna elements and hard horn, limits the attractiveness of this approach for this program.

The final class of spatial combining employs amplifier elements embedded in oversized rectangular waveguide [9] or coaxial structures (Fig. 8). The number of ports that can be combined in the rectangular waveguide version is relatively limited. However, using the oversized coaxial combiner, power combining of 32 MMICs has been demonstrated with 80 percent combining efficiency [11]. Due to the radial symmetry in the fields in such a structure, a large number of MMICs potentially can be combined with relatively low loss. Although the radial distribution of MMICs makes the thermal design more challenging, the electrical benefits nonetheless might make this combiner an attractive option for this program.

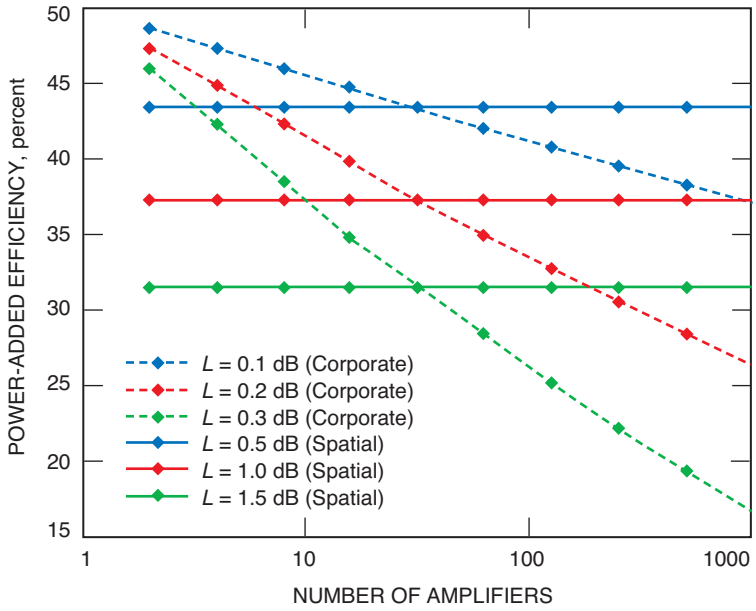


Fig. 7. Effect on PAE for corporate and spatial combining of 50 percent PAE devices as a function of the number of devices combined and circuit loss per combining stage. From [9].

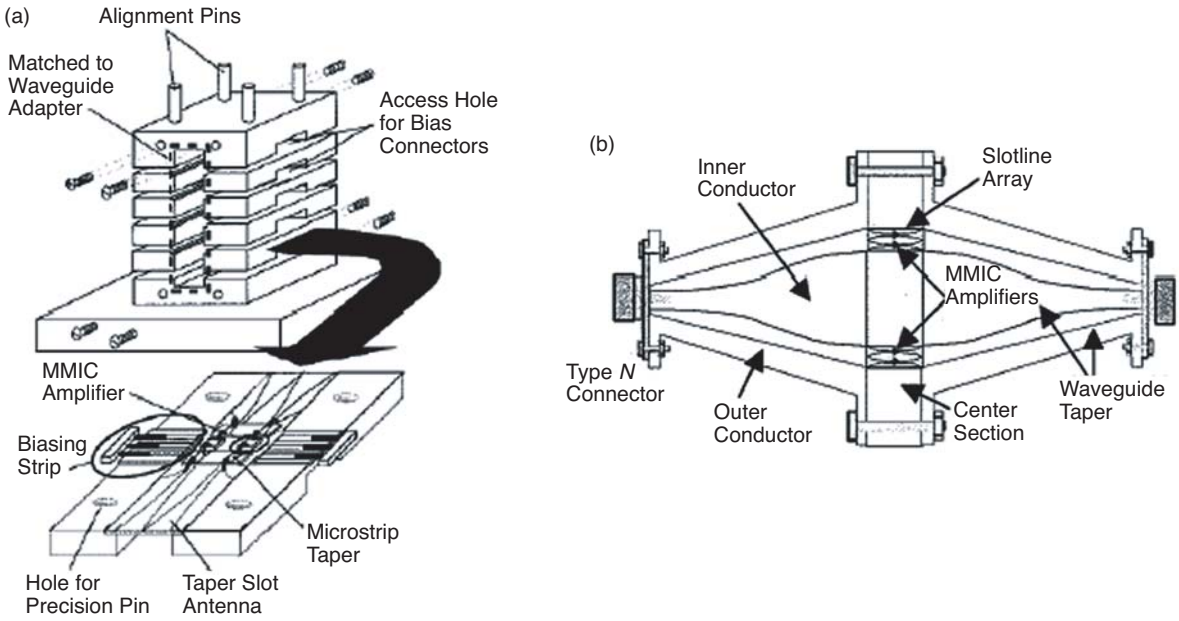


Fig. 8. Examples of spatial combining in (a) oversized rectangular waveguide (from [9]) and (b) in oversized coaxial waveguide (from [11]).

D. N-Way Combiners

Unlike corporate combiners, an N-way combiner can sum multiple ports in a single level. The reduction in line loss directly improves the combining efficiency. Reduction in the number of combining levels also may improve the phase and amplitude ripple by reducing the number of interfaces where reflections can occur. Due to the large number of MMICs required, an N-way combiner implemented in waveguide seems to be an attractive option for this program. N-way radial combiners have been used extensively, and combining of up to 110 ports has been demonstrated [12]. Combining efficiency generally is better than 90 percent at lower frequencies, and preliminary estimates suggest better than 70 percent combining efficiency should be possible at Ka-band.

The compact nature of the radial combiner makes it an attractive choice for low-mass, compact-volume applications. However, with so many MMICs in close proximity, good thermal design is critical. For this program, with respect to the impact on SSPA efficiency, the electrical benefits of an N-way combiner may make resolving any thermal challenge well worth the effort. Significant research effort, already under way to address thermal issues for wideband-gap technology in general, will benefit this program.

E. Summary

Based on the literature review, a subjective summary of the relative merits of various power-combining options is given in Table 2.

Based on output loss, bandwidth, and required MMIC power, the turnstile, radial, waveguide binary, and oversized coaxial combining methods look to be the most promising. With the Glenn Research Center investigating the turnstile combiner, JPL will focus its efforts on the latter three.

Table 2. Relative merits of various power-combining options.[a]

Combining architecture	Output loss	Bandwidth	Required MMIC power	Isolation	Thermal	Mass	Manufacturability
N-way							
Turnstile combiner	++	+	−	+	−	−	++
Radial combiner	++	++	++	+	+	+	+
Wilkinson combiners	−−	++	−	++	+	−	++
Serial combiners	+	+	−	−	++	+	+
Binary							
Waveguide binary	+	++	+	++	++	−	++
Microstrip binary	−−	++	−	++	−	−	++
Spatial							
Oversized coaxial	+	++	+	−	−−	−	−
Plane wave	−	−	+	+	−−	+	−
Waveguide	−	−−	+	+	+	+	+
Resonant cavity	+	−−	+	−−	−	+	−

[a] "++" = very good; "+" = good; "−" = poor; and "−−" = very poor.

IV. Candidate SSPA Architectures

The following SSPA architectures have been selected for further study based on the considerations described in Section II. Only a cursory description for illustrative purposes is given at this point. Detailed analyses will be performed in subsequent articles.

A. Architecture 1: Radial Combiner

1. SSPA Architecture. A block diagram of the first architecture is shown in Fig. 9. A 24-way and a 4-way microstrip power splitter based on the Wilkinson divider is employed for input power division. To make the architecture modular and to simplify assembly, the number of carriers is limited to two. The driver carrier contains two high-gain driver MMICs and control circuitry [e.g., for an automatic gain control (AGC) loop]. The power-amplifier carrier contains a third driver MMIC and two power MMICs in a balanced configuration. Lange couplers are used to combine the power MMICs on-carrier. The balanced configuration provides numerous benefits, including better stability and improved voltage standing wave ratio (VSWR) at the output of the power amplifier (PA) carrier [2]. In addition to improving the match, the balanced configuration also shields the operation of the radial combiner from individual MMIC failure. At the expense of the loss of a single Lange coupler, the required number of combining ports in the radial combiner is reduced by half.

Should the gain of this architecture be insufficient, additional driver MMICs can be inserted in the 24-way input splitter without introducing the possibility of a single-point failure. The total number of MMICs combined in this architecture is 192 ($24 \times 4 \times 2$).

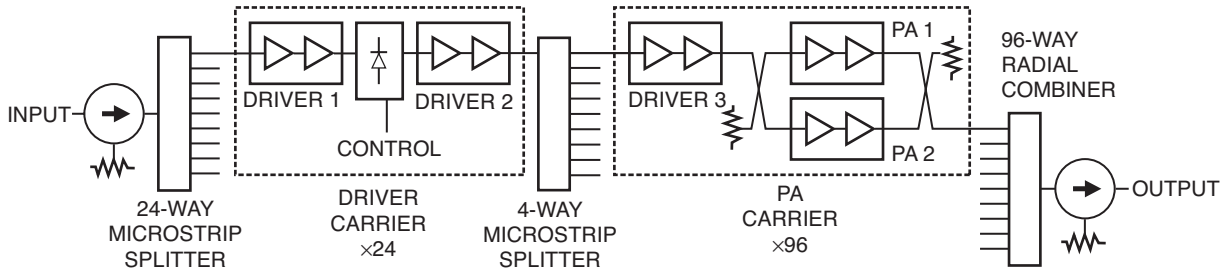


Fig 9. The 96-way radial-combiner-based SSPA architecture.

2. Radial Combiners. There are a number of radial combiners that can be used with the above architecture. However, JPL has chosen to focus primarily on a modified version of the 19-way combiner presented by Chen [13] (Fig. 10). The combiner employs a Marie transducer to convert the circular TE_{01} mode to the rectangular TE_{10} mode output. The circular mode is excited at the center of the base where 19 rectangular waveguides converge. Unlike some radial combiners that have rectangular waveguides in the base oriented such that the guides' E-plane is parallel to the cylindrical base axis [14], the Chen design has the waveguides oriented such that the guides' E-plane is normal to the base axis. This feature allows the possibility of greatly increasing the number of inputs by simply reducing the height (b-dimension) of the rectangular guides. However, since the circular-waveguide diameter cannot be arbitrarily increased, the number of inputs in practice is limited by the finite thickness of the rectangular guide walls and by the increasing loss with reduction in waveguide height (Fig. 6).

It is expected that the Chen combiner can be extended to 24 input ports. Each input port then could be fed by additional combiners. For example, a 4-to-1 combiner similar in concept to the septum divider described by Takeda [15] (Fig. 11) could be used for additonal combining.

Since the rectangular TE_{10} mode has no field variation in the b-dimension, the septum combiner has a broadband response. The 4-way septum divider in series with the 24-way version of the Chen combiner will constitute the 96-way radial combiner.

In addition to the above combiner, a modified version of the 110-way radial combiner proposed by Sanders [12] also will be investigated for use in the architecture in Fig. 9.

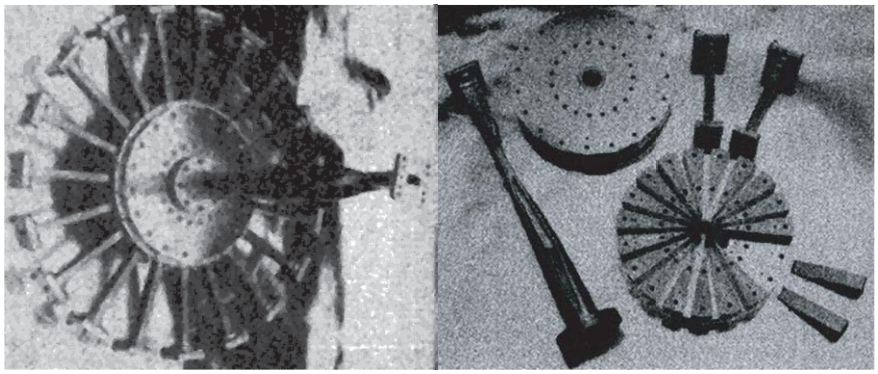


Fig. 10. Chen 19-way radial combiner (18 to 23 GHz, 0.72-dB insertion loss, 20- to 30-dB isolation). From [13].

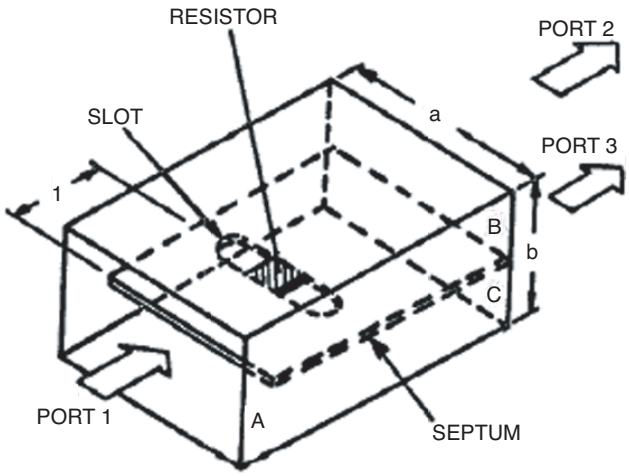


Fig. 11. Takeda septum divider with resistive slot (f = 6.15 GHz, <1.12 VSWR, 0.15-dB insertion loss, 27-dB isolation).

3. Microstrip-to-Waveguide Transitions. A key challenge in implementing the radial combiner design will be the transition from the microstrip output of the PA carrier to the waveguide input of the radial combiner. Two transitions that may be suitable for this application are indicated in Fig. 12. These and other transitions should be investigated in follow-on work until a suitable transition is identified.

4. Expected Performance. A conceptual drawing of the SSPA and estimates of some performance parameters are provided in Fig. 13.

B. Architecture 2: Binary Waveguide Combiner

1. SSPA Architecture. A block diagram of the second architecture is shown in Fig. 14.

Standard corporate binary waveguide structures are used both as the input divider and as the output combiner. Eliminating the microstrip divider at the input reduced the number of driver MMICs required as compared with the radial combiner architecture. Should additional gain be needed, a second driver MMIC can be added to the driver carrier. Similarly, a second power MMIC can be added to the PA carrier in a balanced configuration.

2. Binary Combining Element. As mentioned in Section III.B, a low-loss binary combining element is required for the corporate combining approach to be feasible. A waveguide combining element based on a resistive septum was designed and analyzed to assess if reasonable performance can be achieved. The design is illustrated in Fig. 15.

Unlike more common waveguide combiners with H-plane bends, the proposed combiner has bends in the E-plane. Since the orientation of the waveguide is the same as in the radial design, the microstrip-to-waveguide transitions discussed in Section IV.A.3 also can be used with this structure.

Finite-element analysis indicates that the structure has excellent broadband characteristics (Fig. 16). The insertion loss is better than 0.06 dB; the match is better than 27 dB; and the isolation is better than 33 dB across the full 31- to 36-GHz band. The conductor loss of gold was included in the model since it is envisioned that, to minimize mass, gold-plated aluminum will be used to implement the structure.

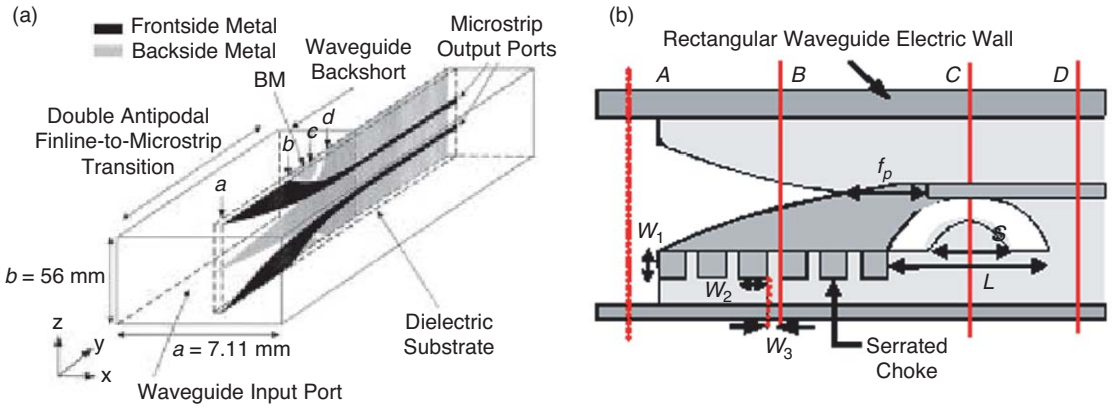


Fig. 12. Microstrip-to-rectangular waveguide E-plane launchers: (a) 26 to 40 GHz, 0.3-dB insertion loss, Jeong [16] and (b) 75 to 90 GHz, 0.74-dB insertion loss, Kim [17].

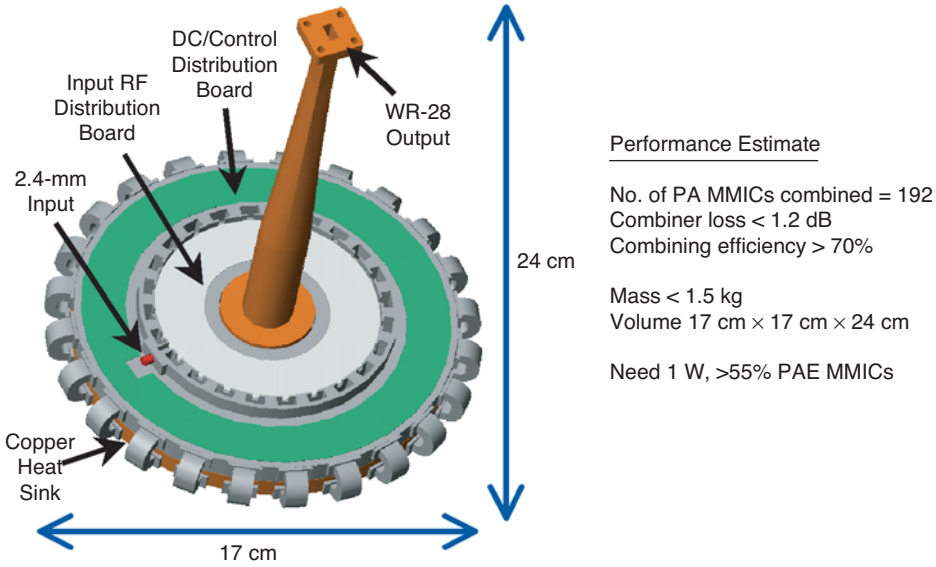


Fig. 13. Proposed radial-combiner-based SSPA.

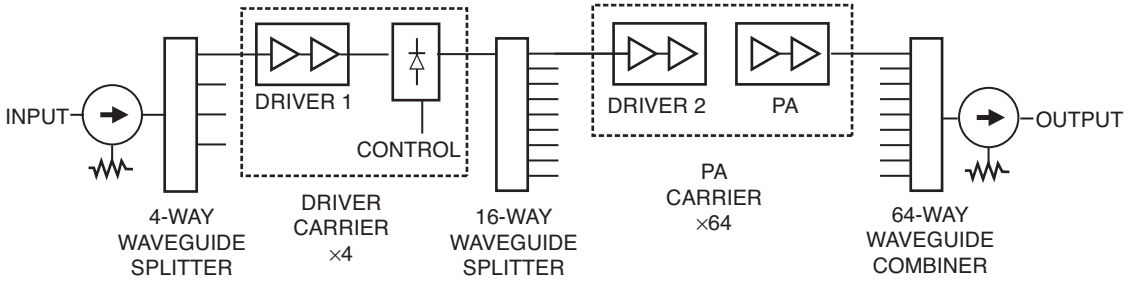


Fig 14. Binary-waveguide-based SSPA architecture.

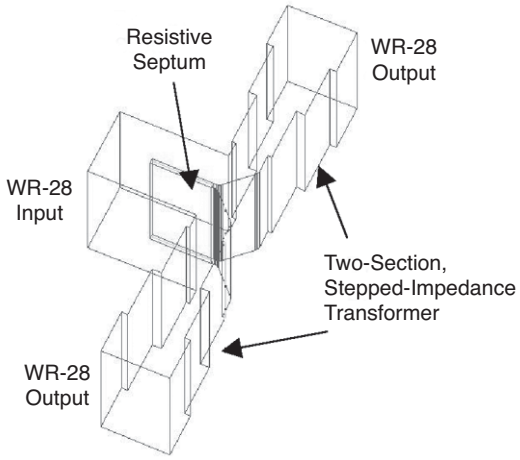


Fig 15. Resistive septum waveguide combiner (31- to 36-GHz design, 0.06-dB insertion loss).

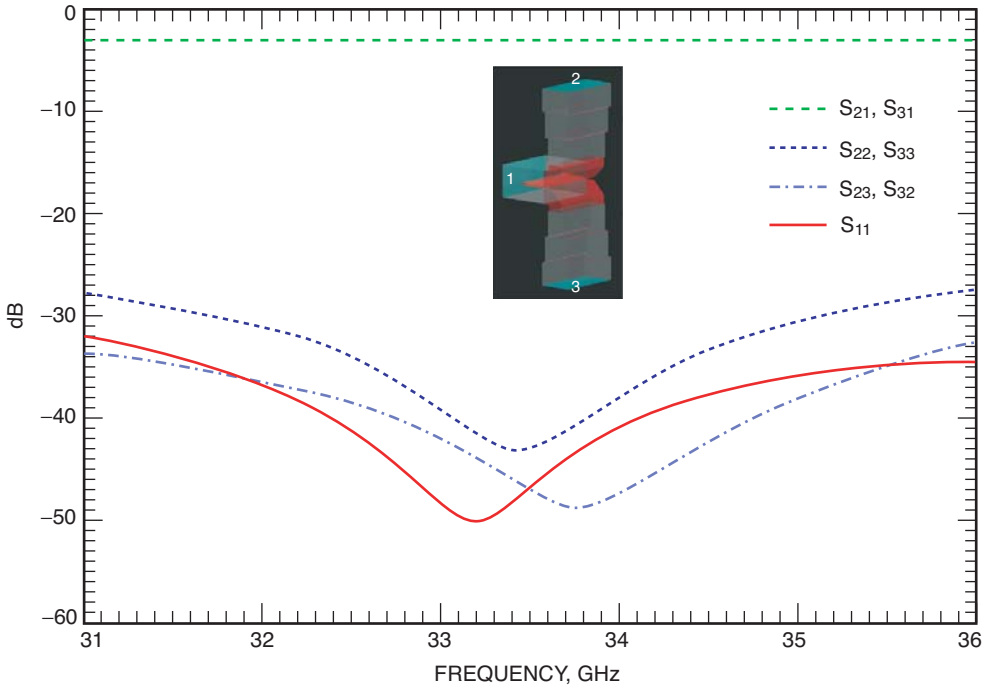


Fig. 16 Simulated performance of the waveguide combiner in Fig. 15.

3. Expected Performance. Figure 17 provides an illustration of the proposed SSPA and estimated performance parameters.

C. Architecture 3: Oversized Coaxial Spatial Combiner

The oversized coaxial SSPA architecture is illustrated in Fig. 18.

Four-way microstrip combining is used on the input side both to boost drive power and to prevent single-point failure at the driver stage. The combiner is expected to be a modified version of the design discussed in Section III.C [Fig. 8(b)] [11]. In particular, the design in [11] has a coaxial connector on the

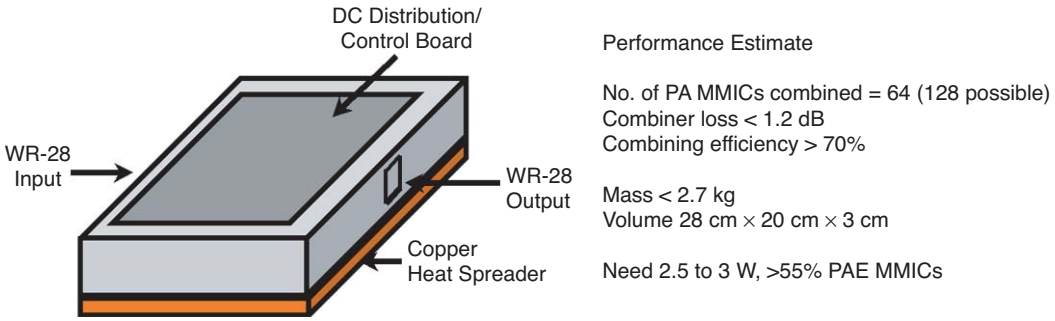


Fig 17. Proposed binary-waveguide-combiner-based SSPA.

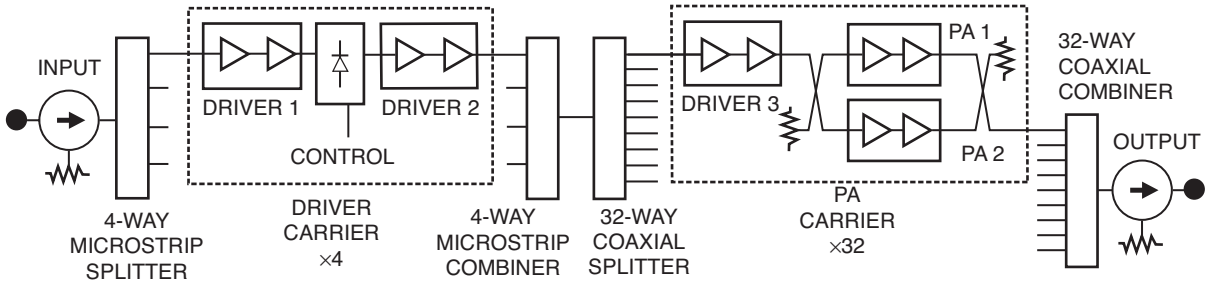


Fig 18. Oversized coaxial-combiner-based SSPA.

output, which may limit the output power at Ka-band. Modifications to be explored include waveguide input/output to improve power handling and alternate MMIC coupling structures to improve isolation and lower loss.

V. Conclusion

In summary, three SSPA architectures were identified based on an extensive literature survey. These architectures were chosen with the final application requirements and the strengths and weaknesses of the underlying gallium nitride technology in mind. An effort was made to make the architectures flexible to the requirement for MMIC power. The overriding factor in choosing the architectures, however, was to minimize the combining loss. Given the high efficiency goal of the program, losses were minimized where possible in order to reduce the MMIC efficiency requirement. Even so, a challenging MMIC PAE of >55 percent likely will be required if the amplifier efficiency goal is to be achieved.

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