Ka-Band Wideband-Gap Solid-State Power Amplifier: General Architecture Considerations

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Motivated by recent advances in wideband-gap (WBG) gallium nitride (GaN) semiconductor technology, there is considerable interest in developing efficient solid-state power amplifiers (SSPAs) as an alternative to the traveling-wave tube amplifier (TWTA) for space applications. This article documents the general architecture considerations pertinent to developing SSPA architectures that can enable a 120-W, 40 percent power-added efficiency (PAE) SSPA at 31 to 36 GHz. This article develops an estimated loss budget for the common elements of these SSPA architectures. It then considers the bandwidth effects of the monolithic microwave integrated circuits (MMICs) and various combiners/dividers used that influence the performance of the SSPA architecture. Finally consideration is given to possible MMIC power levels, efficiencies, and gain. Using these factors, this article develops MMIC and power-combiner requirements for an SSPA architecture to reach the goal of 120 W with a 40 percent PAE.

I. Introduction

A. Wideband-Gap Solid-State Power Amplifier Architecture Study Background

A key component of microwave telecommunication systems is the power amplifier. It is typically the amplifier's linearity, output power, and efficiency that drive the communication system's link performance, power budget, and thermal design. Microwave amplifiers based on vacuum-tube technology are widely used in space telecommunication applications due to their high power capability, good efficiency, and established flight history. However, motivated by benefits such as low supply voltage, graceful degradation, low development cost, and a wide commercial technology base, there is considerable interest in developing efficient, solid-state power amplifiers (SSPAs) as an alternative to vacuum tube technology.

A fundamental hurdle to achieving this objective, however, is the fact that solid-state devices, generally in the form of monolithic microwave integrated circuits (MMICs), produce less power and operate at lower efficiency as compared with individual tube devices. At 32 GHz (Ka-band), for example, commercially

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available gallium arsenide (GaAs) MMIC chips have output power capability that is over an order of magnitude less than that of a traveling-wave tube amplifier (TWTA), and the efficiency is approximately half. Recent advances in wideband-gap (WBG) semiconductors such as gallium nitride (GaN), however, have raised expectations that a new class of high-power, high-efficiency SSPAs can be developed as a suitable alternative to TWTAs.

This article is the first in a series of *Interplanetary Network Progress Report* articles that presents results of a study to evaluate several SSPA architectures and surveys the underlying WBG MMIC technology. The goal is to assess whether expected advances in WBG technology can make a solid-state replacement of a TWTA feasible. This article begins by developing the requirements of an SSPA architecture whose goal is to replace a TWTA.

B. Technical Goals

Key performance targets for the WBG SSPA are listed in Table 1. Compared to state-of-the-art SSPAs at Ka-band (using GaAs technology), the target output power is approximately 10×, and the power-added efficiency is approximately 2× higher. The bandwidth of the SSPA is determined by the frequency response of the MMIC, the input power divider, and the output power-combiner circuits. The MMIC bandwidth is not expected to be a limiting factor. Currently available GaAs MMICs generally have bandwidths in the 10 to 25 percent range without specifically pursuing a wideband design. This is an inherent advantage of pursuing solid-state systems. Moreover, the higher output impedance of GaN devices is expected to further increase the bandwidth capability of WBG MMICs. The required 10 percent SSPA bandwidth, however, does constrain the power-dividing/-combining approaches, as discussed below. The noise figure, amplitude modulation (AM)/phase modulation (PM) conversion, and bias voltage are primarily functions of specific-device geometry and MMIC design. As such, they were not specifically addressed in this study. Instead, this study focused on the SSPA architecture with particular emphasis on broadband, efficient power-combining technology. Total output power, efficiency, bandwidth, and reliability were considered to be the key metrics of the target SSPA. MMIC requirements driven by candidate architectures also were defined and are proposed as targets for further WBG MMIC technology development.

Table 1. SSPA end-of-life performance goals.

Parameter	Value	Note
Power output	120 to 150 W	—
Power-added efficiency	40 percent	At $P_{1\mathrm{dB}}$
Band of operation	31 to 36 GHz	—
Bandwidth	10 percent	—
Gain	50 dB	—
Noise figure	<20 dB	—
AM/PM	<2 deg/dB	—
Phase ripple	<3 deg peak to peak	—
Input bus voltage	50 V ± 5 V	DC
Mass	<4 kg	Including EPC
Environment	Geosynchronous Earth orbit (GEO) or deep space	—

II. General Architecture Considerations

A. The Basic SSPA Architecture

A simplified block diagram of a typical SSPA is shown in Fig. 1. The electronic power conditioner (EPC) provides the interface to the spacecraft bus. It provides regulated bias voltage to each section of the RF block and provides adequate filtering/isolation between the spacecraft bus and the SSPA.

The driver section of the RF block generally contains relatively low-power, high-gain stages that drive the high-power section. Sufficient gain is required to enable the exciter output, typically on the order of 0 dBm, to drive the SSPA into compression. The driver chain also contains control circuitry for overdrive protection and automatic gain control.

The heart of the SSPA, however, is the high-power section of the RF block. This is where the outputs of a number of high-power MMICs are efficiently combined to produce the required SSPA output power. Filters and isolators typically are included at the output of the high-power section to aid transmitter subsystem integration and meet adjacent channel power requirements. For high-power amplifiers, these components generally are added external to the SSPA. Since these components are required for tube-based as well as solid-state amplifiers, the effects of the filters and isolators were not included in the SSPA performance numbers for the purpose of this study. This study focused primarily on the power divider/combiner architecture of the high-power section to determine if expected advances in WBG technology can be successfully leveraged to achieve SSPA performance that is competitive with the TWTA.

GaAs devices can provide high gain at Ka-band and therefore potentially can be used in the driver section of the target SSPA. However, this would require the EPC to deliver ∼6-V bias for GaAs devices in addition to the 30-V bias for WBG devices. Hence, a fully WBG solution may be desirable to simplify the EPC and system design. The overall gain requirements of the driver section are estimated to guide future development of high-gain WBG driver MMICs in addition to high-power/high-efficiency WBG power MMICs.

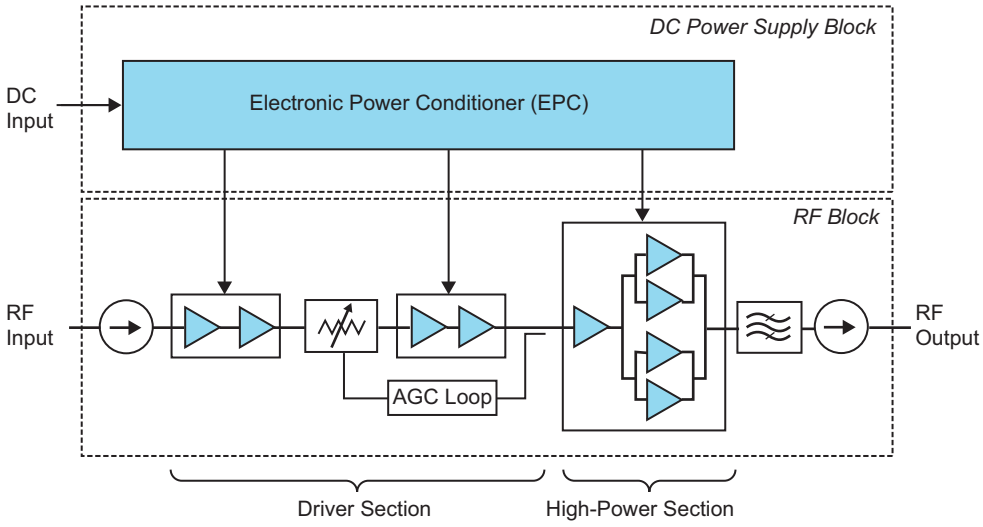

Fig. 1. Simplified block diagram of a solid-state power amplifier. The high-power section contains an input divider that feeds a number of MMIC amplifiers and a power combiner that collects the MMIC amplifiers' output power.

B. Power-Combiner Loss

As noted above, the essential drawbacks of the SSPA with respect to the TWTA are output power and efficiency. The performance of the SSPA with respect to total output power and SSPA efficiency is determined by the performance of the MMICs in the output stage, the number of MMICs power combined, and the combining efficiency. Although WBG semiconductor technology is expected to significantly improve power and efficiency at the MMIC level, to achieve peak SSPA performance, it is imperative that potential SSPA architectures minimize the power-combining loss while preserving the inherent MMIC bandwidth and reliability.

There are two general categories of losses that affect the efficiency of a combining circuit. The first category of loss is the total insertion loss of the microwave circuit between the MMIC output and the SSPA output. This loss includes reflection, conductor, and dielectric losses of the circuit. As indicated in Fig. 2, the major contributors to this category of loss are the MMIC package, the transition between the package and the combining circuit, and the combining circuit itself.

The second category of loss results from power and phase imbalance in each leg of the combiner due to variations in the input dividing circuit, the MMICs, and the output combining circuit. Losses due to the MMIC package, package-to-combiner transition, signal transmission line, and signal imbalance are estimated next.

1. MMIC Package Loss. As illustrated in Fig. 2, the first loss contributor at the output of the MMIC is the MMIC package. Although the high power capability of WBG semiconductors can significantly reduce the number of MMICs that must be combined, the high power density of WBG MMICs also poses a challenge for MMIC packaging. Not only must the package provide adequate heat sinking, it must provide a good hermetic seal and a low-loss microwave interface, and it must have sufficient bandwidth.

Standard drop-in packages, such as the Stratedge SE-40 shown in Fig. 3, employ a packaging architecture that addresses the above requirements. In such a package, the MMIC is die-attached to a copper tungsten or copper molybdenum base via a high-temperature soldering process. The copper alloy provides a good compromise between a good coefficient of thermal expansion (CTE) match with the MMIC and the high thermal conductivity required for adequate heat removal. A lid can be attached to a ceramic guard ring around the MMIC to form a hermetic seal. The DC and RF signals generally are routed

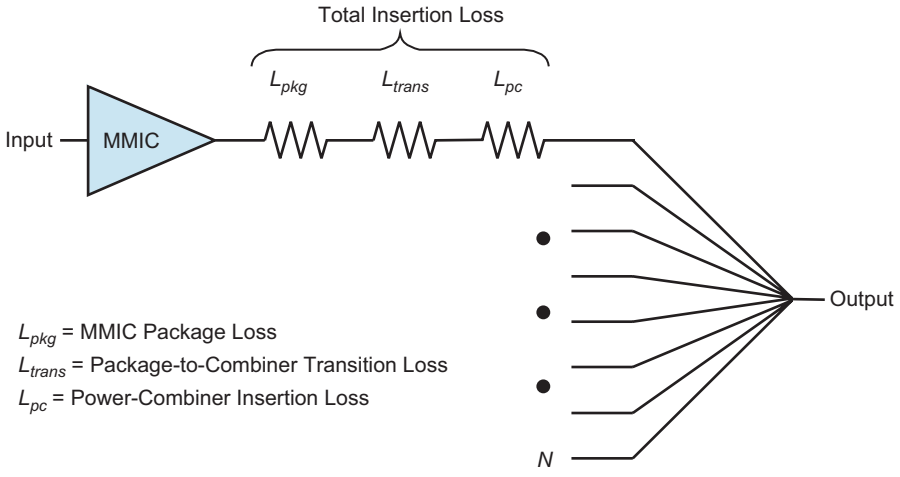

Fig. 2. Components of total insertion loss between the MMIC and SSPA output.

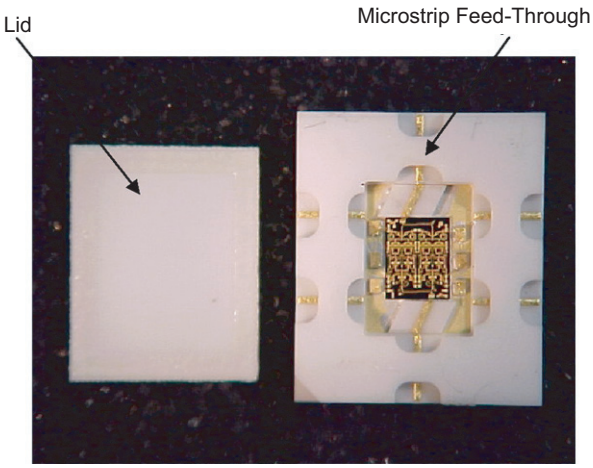

Fig. 3. Triquint GaAs Ka-band power amplifier MMIC in a Stratedge SE-40 package at JPL. The package lid is shown to the left.

through the cavity walls using feed-throughs formed by microstrip-to-microstrip transitions. Measured performance of a single feed-through in the SE-40 package is shown in Fig. 4. The measured insertion loss includes the loss of a 4.8-mm microstrip feed line that has an estimated loss of 0.2 dB. Although the SE-40 is a broadband part, it is not optimized for the 31- to 36-GHz frequency band under study. With a custom design, it is estimated that this packaging approach should yield <0.35-dB insertion loss over the required 10 percent bandwidth. The thermal constraint of such a package will need to be evaluated versus the yet-to-be-determined WBG MMIC thermal limits. The SE-40 package can accommodate MMICs as large as 4.9 mm × 3.4 mm.

2. MMIC Package-to-Power Combiner Transition Loss (Microstrip to Waveguide). Efficient, large-scale power combiners generally employ low-loss waveguide transmission lines. As described below in more detail, waveguides have significantly lower insertion loss as compared with planar transmission lines at millimeter-wave frequencies. Since the MMIC package has microstrip RF ports, a suitable transition therefore is required to efficiently couple energy from microstrip to waveguide structures. Previously [1] two transitions [2,3] were identified as possible candidates. Both employ tapered slot structures that potentially can enable wide-bandwidth operation. With further investigation, however, it was determined that a simple probe-type transition can provide sufficient bandwidth while lowering insertion loss as compared with the tapered slot transitions.

The second contributor to the combining loss indicated in Fig. 2 is the MMIC package-to-power combiner transition loss. To estimate this loss, the probe transition shown in Fig. 5 was designed and analyzed using an Ansoft high-frequency structure simulator (HFSS). As in conventional designs, the microstrip signal line is extended into the waveguide volume through the broad wall to form an E-field probe. To minimize radiation loss, the probe enters the waveguide volume through a narrow channel that is cut off at the operating frequency. The probe is shaped in the form of a radial stub to increase bandwidth. A 0.38-mm (15-mil) alumina substrate was chosen to minimize substrate discontinuity with the MMIC package discussed previously.

The response of the transition structure based on HFSS finite-element analysis also is shown in Fig. 5. The match is better than 25 dB, and the insertion loss is less than 0.08 dB over the design band of 31 to 36 GHz. Both dielectric and conductor losses are included. The conductivity of electro-deposited gold (3.3×10^7 S/m) was used for all conductors. This conductivity value was determined experimentally during hardware validation activities in this study and is approximately 20 percent lower as compared with the default gold conductivity definition in HFSS.

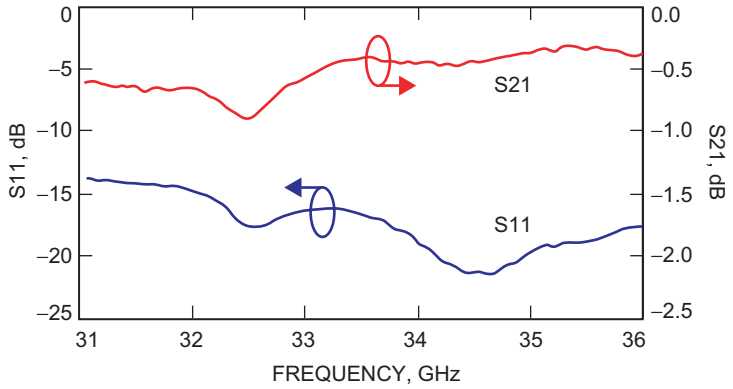

Fig. 4. Stratedge SE-40 package performance over the frequency band under study.

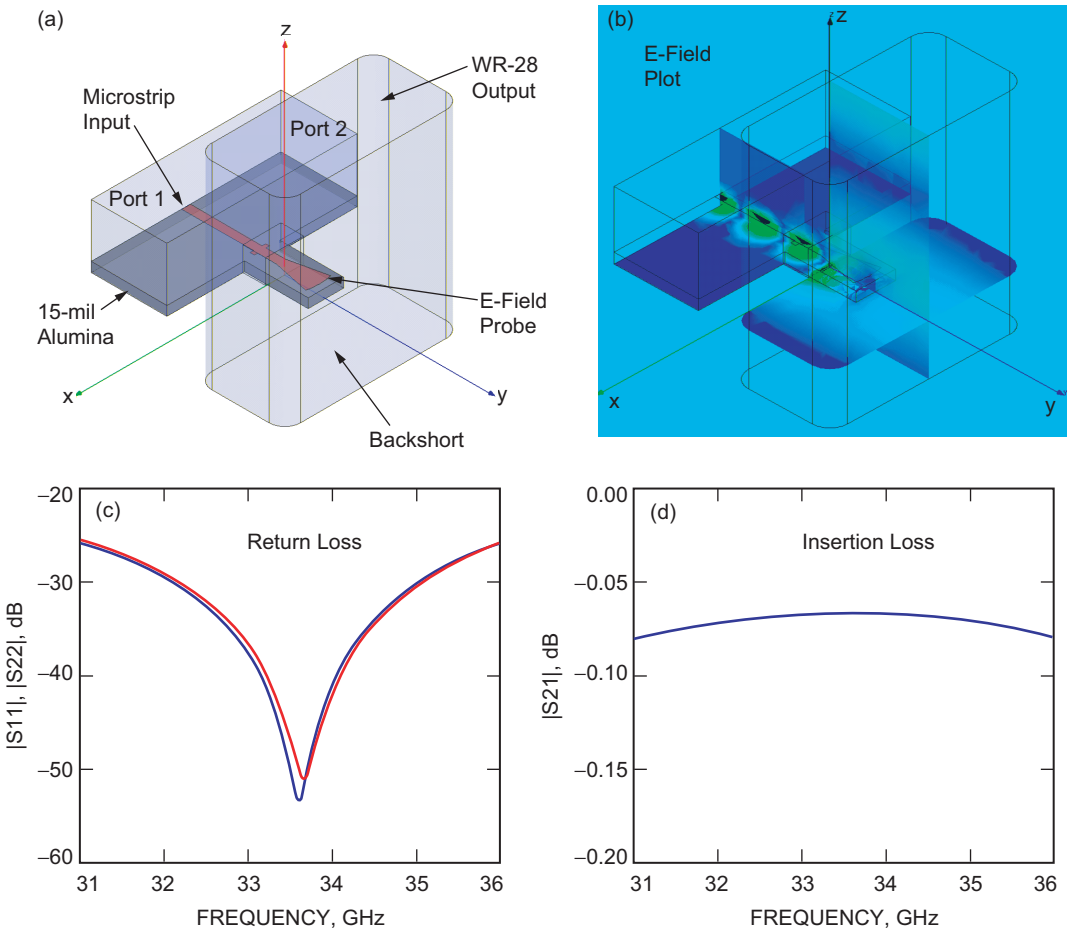

Fig. 5. HFSS model and analysis results of microstrip-to-rectangular-waveguide transition: (a) model geometry, (b) E-field plot, (c) return loss, and (d) insertion loss.

3. Transmission-Line Loss at Ka-Band. To minimize insertion loss in the power combiner, it is essential that a low-loss transmission line be chosen as the guiding structure. Reflection loss due to mismatches can be reduced to a large extent by proper design. Dielectric and conductor losses, however, are fixed for transmission lines of a given type and geometry. When combining a large number of MMICs, the combining circuit generally is many wavelengths long. Therefore, seemingly small differences in transmission-line loss can add up to a significant difference in the efficiency of the combining circuit.

The calculated insertion losses, at 32 GHz, of common transmission lines are listed in Table 2. Only dielectric and conductor losses are included. Measured data for microstrip on GaAs [4] agree well with the calculations. For rectangular and circular waveguides, a measured metal conductivity (electro-deposited gold, 3.3×10^7 S/m) was used.

The first three columns of Table 2 specify the geometry of the transmission line. The nominal dimensions for 50-ohm planar transmission line and for full-height waveguide are used for comparison. For coplanar waveguide, G is the gap between the signal conductor and the ground plane. Two gaps plus the signal conductor width are considered here to be the total width of the line. The loss per guide

Table 2. Insertion loss of various transmission lines at 32 GHz: (a) microstrip on GaAs, (b) coplanar waveguide on GaAs, (c) microstrip on alumina, (d) rectangular waveguide, and (e) circular waveguide.

(a) Microstrip on 0.10-mm (4-mil) GaAs

		W, μm	Zo, ohms	λg, mm	Loss, dB/mm	Loss, dB/λg
		70	50	3.24	0.068	0.22

(b) Coplanar waveguide on 0.10-mm (4-mil) GaAs

W, μm	G, μm	Total width, μm	Zo, ohms	λg, mm	Loss, dB/mm	Loss, dB/λg
26	23	72	50	3.68	0.153	0.56
65	110	285	50	3.40	0.064	0.22

(c) Microstrip on 0.38-mm (15-mil) alumina

		W, mm	Zo, ohms	λg, mm	Loss, dB/mm	Loss, dB/λg
		0.41	50	3.43	0.015	0.051

(d) Rectangular waveguide (WR-28)

	A, mil	b, mil	Zo, ohms	λg, mm	Loss, dB/mm	Loss, dB/λg
	280	140	—	12.45	0.000772	0.0096

(e) Circular waveguide

		R, mm	Zo, ohms	λg, mm	Loss, dB/mm	Loss, dB/λg
		8.2	—	13.2	0.000136	0.0018

wavelength is listed in the final column. Since the lengths of microwave circuits generally scale with the guide wavelength, it is useful to compare this value for the various transmission lines under consideration.

The relative loss per guide wavelength, normalized to that of rectangular waveguide, is as summarized in Table 3.

It is clear from these data that waveguides have significantly lower loss as compared with planar transmission line technology. Moreover, coplanar waveguide (CPW) generally has higher loss as compared with microstrip. Since the CPW impedance depends on the ratio of W to G, it is possible to choose a different combination of parameter values to reduce loss while maintaining the line impedance. However, as indicated in Table 3, to achieve CPW loss comparable to that of microstrip, the total CPW line width increases by approximately a factor of four as compared with the width of microstrip. For comparable widths, the CPW line has more than twice the loss of microstrip.

Since 0.1-mm GaAs is representative of the expected line loss in GaN MMIC technology, it is clear that GaN MMICs designed for high-efficiency applications should minimize on-chip combining to the extent possible. As a comparison of off-chip combining to on-chip combining, consider the waveguide septum designed specifically for the off-chip combining requirements of this effort [1, Section IV.B.2, Fig. 15]. It requires approximately 25 mm of line length ($\sim$2 λ_g). Thus, any on-chip combining requiring microstrip line length more than $2/23 \approx 0.1\lambda_g$, or $\sim$300 μm, will be less efficient than if the combining were performed off-chip using waveguide.

The great benefit of WBG technology for high-power, high-efficiency SSPA application is the potential for sufficient MMIC power to be generated by a single, multi-fingered device cell. Thus, the need for power combining of multiple device cells on-chip to achieve a given power level is reduced. However, to minimize the number of MMICs power combined, and thereby to reduce the system complexity, it may be necessary to implement a limited amount of on-chip combining at the precious expense of efficiency.

4. Signal Imbalance Loss. To evaluate the magnitude of loss due to input amplitude and phase imbalance, it is instructive to consider an ideal two-way combiner, illustrated in Fig. 6. An example of such a combiner is the equal ratio, two-way Wilkinson. For normal operation, the balanced component of the input power is delivered to the load resistor. Any unbalanced component of input power is delivered to the isolation resistor. This absorption of the unbalanced power component is the desired response for increasing the isolation between input ports. However, the power that is dissipated in the isolation resistor is not delivered to the output port. This represents an additional loss above the insertion loss of the microwave circuit. This additional loss theoretically is zero if the combiner is driven with a balanced

Table 3. Transmission-line loss relative to that of rectangular waveguide.

Transmission line	Relative loss
Microstrip (0.1-mm GaAs)	23
Coplanar waveguide (0.1-mm GaAs; $W = 26$ μm)	58
Microstrip (0.38-mm alumina)	5
Rectangular waveguide (WR-28)	1
Circular waveguide ($R = 8.2$ mm)	0.2

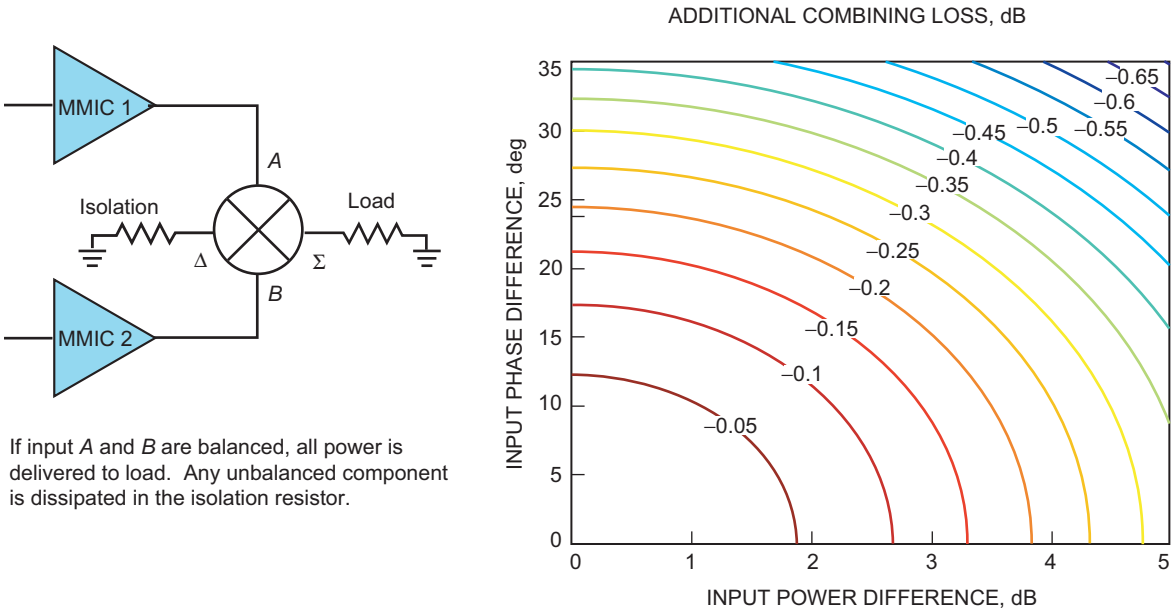

Fig. 6. Additional combining loss in an ideal two-way combiner due to input imbalance.

signal. It can be shown [5] that the additional combining loss resulting from an unbalanced signal is given by the following:

$$\text{imbalance loss} = 10 \cdot \log\left(0.5 + \frac{\sqrt{\text{Pr}}\cos\theta}{1+\text{Pr}}\right) \tag{1}$$

where

$Pr = P_B/P_A$ is the ratio of the input powers

$\theta = \theta_B - \theta_A$ is the input phase difference

A contour plot of this additional loss versus power and phase difference is given in Fig. 6. The plot assumes perfect isolation between input ports. Actual loss therefore will be higher since finite input isolation cannot prevent pulling of the active impedance seen by each MMIC. This plot clearly illustrates that the input phase balance is more critical than the power balance. The 0.2-dB addition loss contour, for example, crosses the power difference axis at a very generous 3.8 dB. On the other hand, the same contour crosses the phase difference axis at approximately 24 deg.

Given the fabrication tolerance issues at Ka-band, achieving the required phase balance could require care. If required, solutions such as MMIC binning, input phase trimming, and individual MMIC bias adjustment can be employed to minimize the additional combining loss due to phase imbalance.

5. Estimated Loss Budget. Based on the simplified analyses presented above, we can estimate the loss budget for the target SSPA as given in Table 4.

It is clear that a significant fraction of the total combining loss is determined by the MMIC package, the transition between the package and the combiner, and the phase uniformity of the MMICs. It is important to note that these losses are largely independent of the power-combining circuit. This suggests that, if the power combining is performed in a low-loss medium (e.g., waveguide), the total combining loss will not be a strong function of the number of MMICs power combined.

Table 4. Estimated loss budget for the target SSPA.

Element	Loss
MMIC package	0.35 dB
Package-to-waveguide transition	0.10 dB
Input phase imbalance (<15 deg)	0.10 dB
Transmission line (WR-28)	0.77 dB/m

C. Bandwidth Limitations

The bandwidth of the SSPA is limited by the bandwidth of each component in the RF path. These components include the driver and power MMICs, the input power divider, and the output power combiner. Bandwidth considerations for each are discussed in general in the following sections. In Section II.C.3, the specific bandwidth limitations of hard-horn-based spatial power combining also is discussed.

1. MMIC Bandwidth. The required 10 percent bandwidth is not expected to be an issue at the MMIC level. Figure 7 illustrates the bandwidth-versus-output power of numerous Ka-band GaAs power amplifier MMICs currently available from Triquint Semiconductor. It can be seen that nearly all MMICs meet at least the required 10 percent bandwidth. Furthermore, it is expected that GaN technology will enable greater bandwidth performance as compared with GaAs technology, due to the higher output impedance of GaN devices as compared with GaAs devices.

2. Power Combiner and Divider Bandwidth. Three waveguide-based power combiners with broadband, low-loss characteristics were analyzed in this study. The results, discussed in [1], suggest that the required bandwidth can be achieved by these combiners. It also is possible to use these power combiners as the power divider in the high-power section of the SSPA. However, assuming >10-dB output-stage gain, it can be shown that the losses in the power divider are not as critical as those in the power combiner. It may be desirable, therefore, to reduce the mass and volume of the SSPA by implementing the input divider in planar technology (e.g., microstrip). To assess the bandwidth limitations of such an approach, four planar power dividers were analyzed over the frequency band under study.

Figure 8 illustrates the ideal response of four common microstrip couplers: the single- and double-element branchline, the rat-race, and the Wilkinson. The data are based on simple circuit theory and

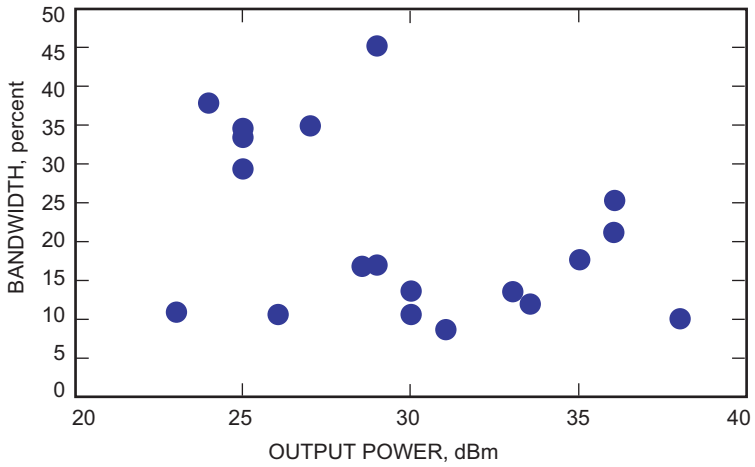

Fig. 7. Bandwidth versus output power of currently available GaAs Ka-band power MMICs.

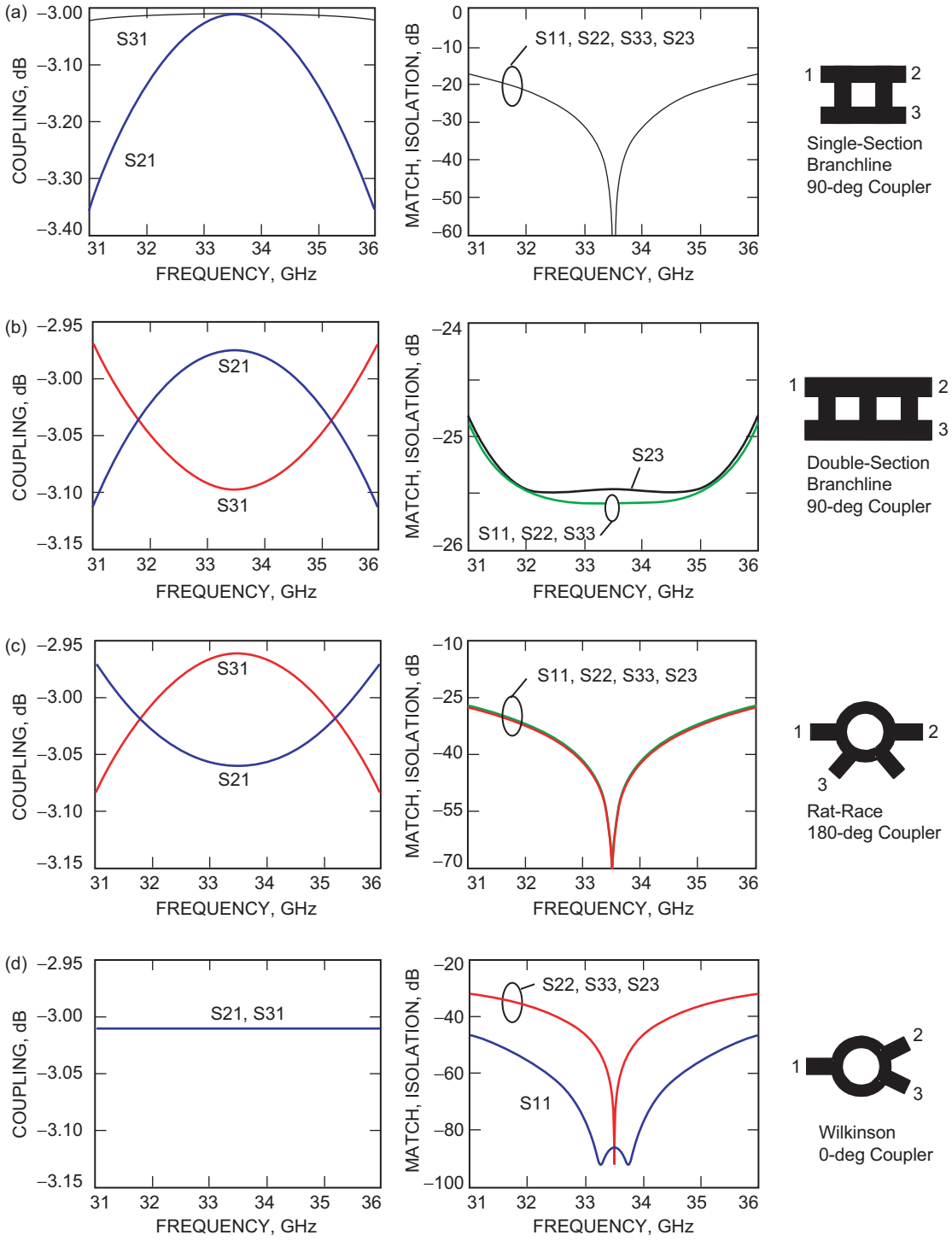

Fig. 8. Ideal circuit response of four microstrip couplers that are commonly used as power dividers: (a) single-section branchline coupler, (b) double-section branchline coupler, (c) rat-race coupler, and (d) Wilkinson coupler.

do not account for the losses that can be expected from real circuits. However, the data do allow one to compare the bandwidth performance of simple microstrip-based power dividers. To divide power equally between more than two ports, multiple couplers typically are cascaded in a binary fashion. Since input power loss is not critical, it also is possible to obtain a number of output ports that is not a power of 2 by simply terminating the output branches that are not required.

Although the insertion loss of the input divider is not critical, the amplitude and phase imbalance is. One contributor to these imbalances is the finite bandwidth of the couplers. The amplitude and phase differences between coupled ports become an increasingly limiting factor as the number of stages increases. The theoretical amplitude and phase balances for each coupler type versus the number of dividing stages are tabulated in Tables 5 and 6. All data are considered over the 31- to 36-GHz band.

It is clear from Fig. 8 and Tables 5 and 6 that the Wilkinson divider has the widest bandwidth. With an ideal symmetry between the circuit ports, the theoretical amplitude and phase balances of the Wilkinson divider are perfect. The need to consider other couplers is primarily driven by the power divider's output phase requirements. Although the Wilkinson divider provides in-phase power division, the branchline and rat-race couplers provide 90 deg and 180 deg, respectively, of output phase difference. To maximize the overall amplitude and phase balances of the power divider, it may be possible to use a combination of coupler types. In such an approach, the Wilkinson divider would provide the power division for most stages, and a branchline and/or rat-race coupler would provide the correct phasing at the final stage. The overall transfer characteristic of such a mixed divider circuit would have to be studied in detail to determine the effects on and implications for higher-order modulation schemes.

Table 5. Theoretical amplitude balance of common microstrip couplers.

Coupler	Theoretical amplitude balance, dB					
	N, number of stages (no. of outputs = 2^N)					
	1	2	3	4	5	6
Branchline-1 section	0.33	0.66	0.99	1.32	1.65	1.98
Branchline-2 section	0.15	0.30	0.45	0.60	0.75	0.90
Rat-race	0.12	0.24	0.36	0.48	0.60	0.72
Wilkinson	0.00	0.00	0.00	0.00	0.00	0.00

Table 6. Theoretical phase balance of common microstrip couplers.

Coupler	Theoretical phase balance, deg					
	N, number of stages (no. of outputs = 2^N)					
	1	2	3	4	5	6
Branchline-1 section	0.52	1.04	1.56	2.08	2.60	3.12
Branchline-2 section	0.36	0.72	1.08	1.44	1.80	2.16
Rat-Race	4.70	9.40	14.10	18.80	23.50	28.20
Wilkinson	0.00	0.00	0.00	0.00	0.00	0.00

3. Bandwidth Effects on Spatial Power Combining with a Hard Horn. Spatial combining architectures were discussed in [1]. While there are many different types of spatial architectures, and arguably an overuse of this term to include architectures that are truly waveguide combining, for TWTA replacement the spatial architecture would have a waveguide input and output. This eliminates systems with large and/or cumbersome "quasi-optical" approaches based on mirrors and lenses; see Fig. 9(a) [6]. The remaining forms of spatial combining, where the active antenna array is placed in a "hard" horn or over-moded guide, are shown in Figs. 9(b) and 9(c).

These latter two architectures are restricted in their bandwidth of operation. The bandwidth of a square hard horn was first estimated by Kildal [7] in 1988. From Eq. (21) of [7], the bandwidth of a hard horn can be related to the size of the aperture of the horn in wavelengths, $\lambda/2a$, where the aperture size is $2a$:

$$BW = \frac{1}{4}\frac{1}{\sqrt{\varepsilon - 1}}\frac{\lambda}{2a} \tag{2}$$

This has tended to hold in practice. For example, a more exact simulation of a hard horn based on the use of the generalized scattering matrix approach and longitudinal-section electric (LSE)/longitudinal-section magnetic (LSM) modes was done by Ali et al. [8]. The LSE/LSM modes form a complete set of orthogonal modes in the area of the dielectric loading. Using this approach [8], they design a hard horn for 31 GHz and compute the bandwidth as a function of the relative permittivity of the dielectric loading. A comparison of this approach and Kildal's estimated bandwidth is shown in Fig. 10.

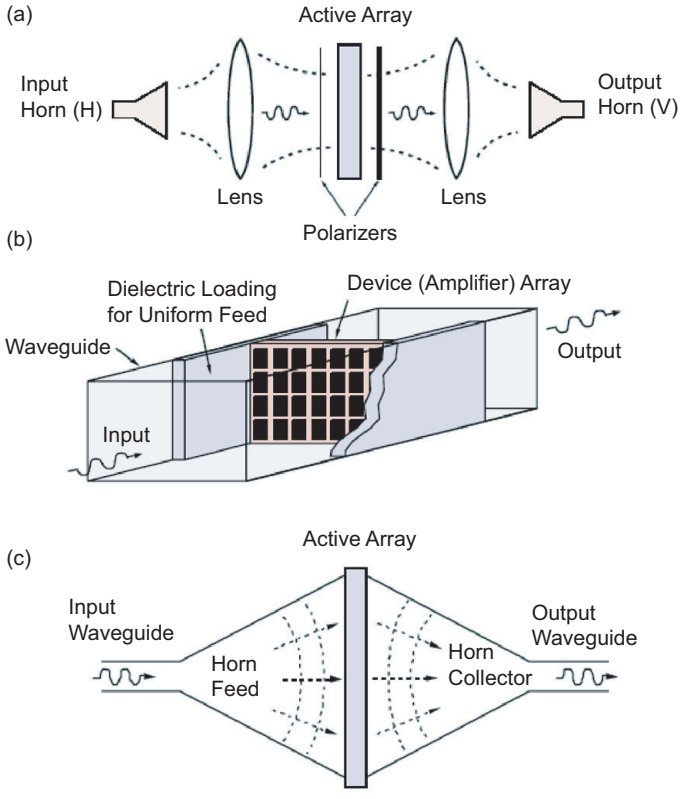

Fig. 9. The three basic forms of spatial power combining from [6]: (a) quasi-optical, (b) spatial amplifier in uniform ("hard") guide, and (c) spatial amplifier in over-moded waveguide.

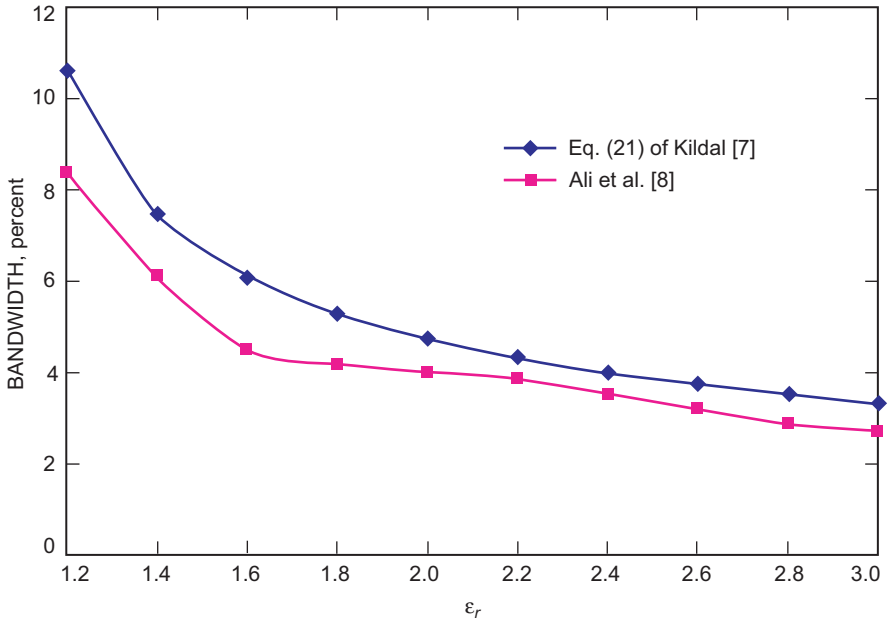

Fig. 10. Bandwidth of a hard horn as a function of the dielectric loading. It shows a comparison of the approximate equation of Kildal [7] to Ali et al. [8].

Figure 10 covers the typical values that are used for the dielectric loading. What can be concluded is that the bandwidth of a hard horn is less than 10 percent for this range of dielectric loading with the more exact generalized scattering matrix computations. Outside this typical range of dielectric loading, such as when the relative permittivity decreases below $\varepsilon_r = 1.2$, the grooves become significantly deeper, such that for the limiting case of $\varepsilon_r = 1.0$ only infinitely deep grooves satisfy the hard boundary condition as given by Kildal [7]. The designer then is faced with the increasing groove depth, causing a corresponding increase in the amount of power in the grooves, instead of the waveguide region where the spatial combining is occurring. To counter this effect, the designer can increase the size of the horn to proportionally increase the ratio of the area air inside the horn to the area in the dielectric loading. Unfortunately, as shown in [8], increasing the size of the horn decreases the bandwidth.

Fewer data exist for the spatial amplifier over-moded waveguide approach, but recent results show a bandwidth of 5 percent [9]. A more useful commercial data point on spatial power combiners would be the work of Wavestream Corporation, which is a venture-capital-funded spin-off of the California Institute of Technology spatial power-combining efforts. Currently, Wavestream is advertising commercial products with a nominal operating bandwidth of 30 to 31 GHz [10].

D. General MMIC and Power-Combiner Requirements

1. MMIC Power and Efficiency. The plots in Fig. 11 illustrate the relationship between the SSPA, the MMIC, and the power-combiner parameters. The SSPA power is primarily a function of the individual MMIC power and the number of MMICs combined. The MMIC power is limited by the device technology while the number of combining ports is limited by increasing complexity of the amplifier system. If we assume a total combining loss of 1 dB and limit the number of combining ports to 32, Fig. 11(a) indicates that a minimum of 6 W per MMIC will be required to achieve the target 150-W SSPA. If a 12-W MMIC is successfully developed, only 16 such MMICs will need to be power combined.

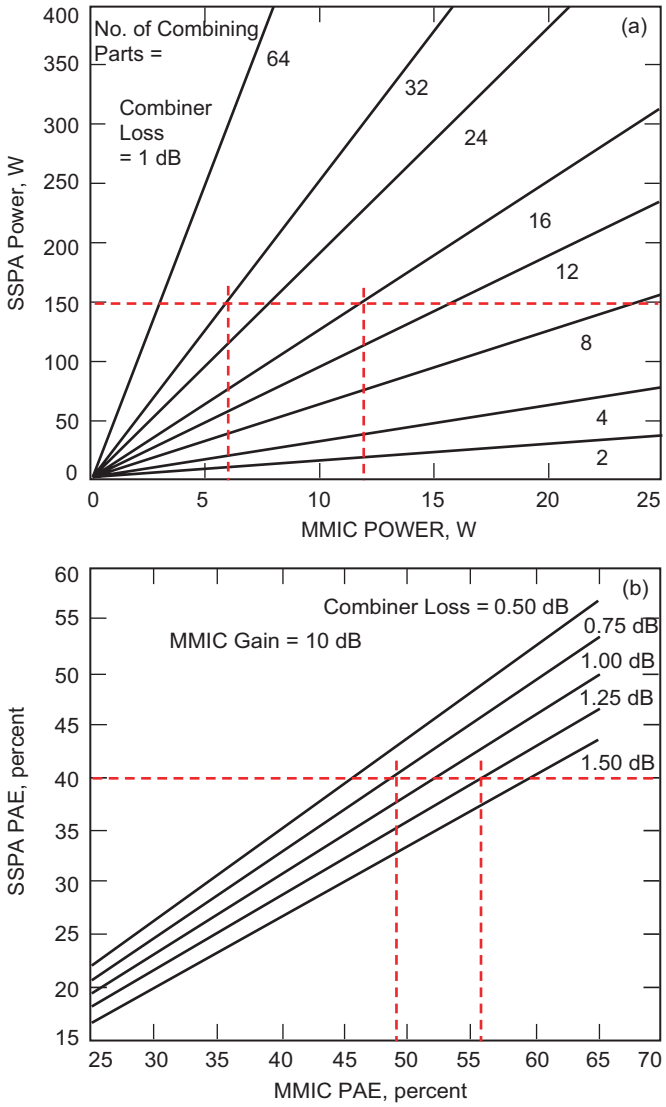

Fig. 11. The SSPA power and efficiency are related to the power and efficiency of the combined MMICs and the combiner loss: (a) SSPA versus MMIC power and (b) SSPA versus MMIC efficiency for a varying number of combining ports and combiner loss.

The SSPA efficiency is a function of the MMIC efficiency and the total combining loss. If we assume that a combining loss in the range of 0.75 to 1.25 dB can be achieved, Fig. 11(b) indicates that the required MMIC efficiency is in the range of 49 to 56 percent. This calculation assumes that the MMIC gain is at least 10 dB. The required MMIC power and efficiency represents >2× improvement over commercially available MMICs based on gallium arsenide technology.

2. MMIC Gain. It is important that the MMICs in the high-power section of the SSPA have sufficient gain. For finite gain, the power-added efficiency, defined as

$$\eta_{PAE} = \frac{(P_{out} - P_{avail})}{P_{dc}} \tag{3}$$

is always less than the drain efficiency, defined as

$$\eta_d = \frac{P_{out}}{P_{dc}} \tag{4}$$

With decreasing MMIC gain, greater input power must drive the MMIC to yield a given output power, and, thus, the PAE is reduced. It is easy to show that the ratio of PAE to drain efficiency is given by

$$\frac{\eta_{PAE}}{\eta_d} = 1 - \frac{1}{G} \tag{5}$$

where G is MMIC gain. A plot of this ratio as a function of MMIC gain is shown in Fig. 12. It is clear that at least a 10-dB MMIC gain is required to ensure a high PAE MMIC. For a 13-dB gain, the PAE-to-drain efficiency ratio is 0.95.

The gain of the power MMIC also is important in a multi-stage SSPA design, where a number of high-gain stages may be utilized to achieve the required SSPA gain. Adequate gain in the power MMIC is required to reduce the dependence of overall SSPA efficiency on the driver MMIC efficiency. The simplified case of a two-stage SSPA is shown in Fig. 13, where the first amplifier block represents a driver MMIC (or a multi-MMIC drive chain) and the second amplifier block represents that power MMIC. It can be shown that the overall SSPA efficiency for such a case is given by

$$\eta_{sspa} = \frac{\eta_1 \eta_2 \left(G_1 G_2 - 1\right)}{\eta_2 \left(G_1 - 1\right) + \eta_1 G_1 \left(G_2 - 1\right)} \tag{6}$$

Since the SSPA gain requirement is 50 dB, we expect that G_1 will be on the order of 40 dB. Thus, assuming $G_1 \gg 1$, we can reduce Eq. (6) to the following:

$$\eta_{sspa} = \frac{\eta_1 \eta_2 G_2}{\eta_2 + \eta_1 \left(G_2 - 1\right)} \tag{7}$$

We can plot the ratio $m = \eta_{sspa}/\eta 2$ as shown in Fig. 13. The ratio is plotted as a function of G_2 with $n = \eta_1/\eta_2$ as a parameter. For $n = 1$ (e.g., $\eta_1 = \eta_2 = \eta$), we see that G_2 is not a factor and the

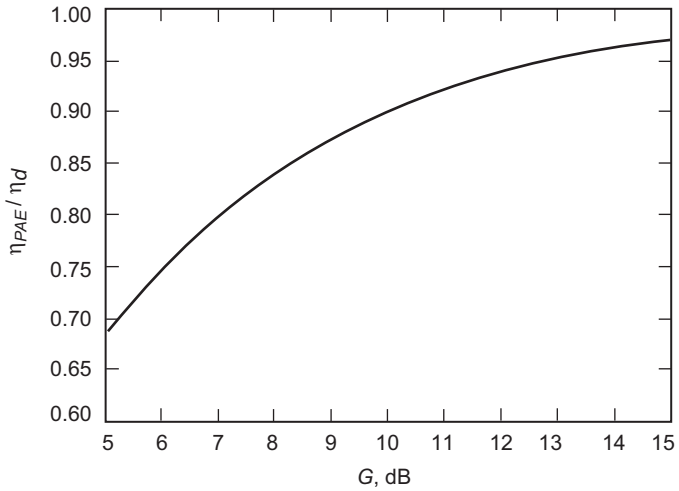

Fig. 12. Ratio of power-added efficiency to drain efficiency versus amplifier gain.

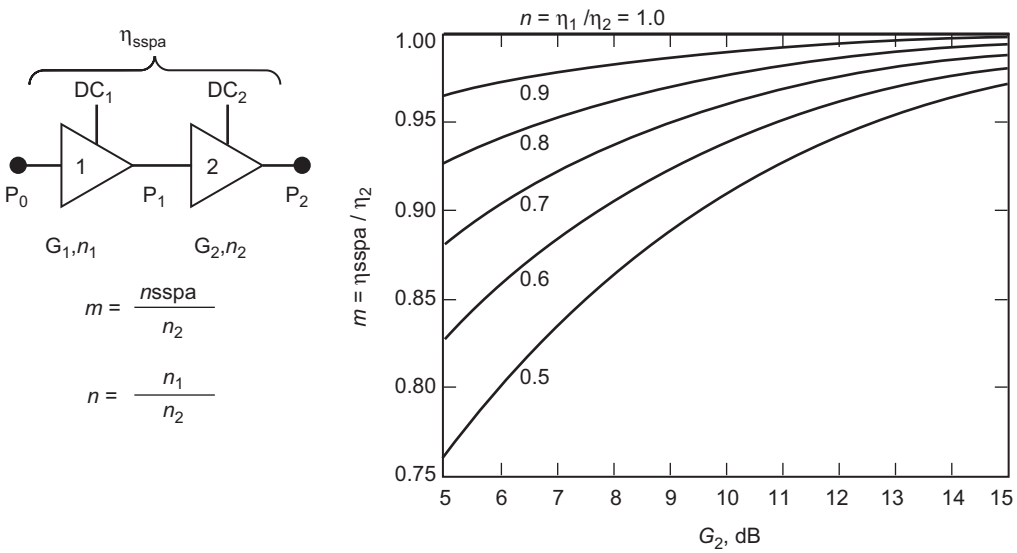

Fig. 13. Effect of power MMIC gain and driver MMIC PAE on overall SSPA PAE. The plot is parameterized by $n = \eta_1 / \eta_2$, the ratio of driver MMIC PAE to power MMIC PAE.

SSPA efficiency is simply η. For $n < 1$, however, the output stage gain has a significant effect on the SSPA efficiency.

Ideally, GaN MMICs specifically optimized for both gain and efficiency would be used as drivers in the SSPA. However, if lower-efficiency GaAs MMICs are used instead, the ratio of the power MMIC efficiency to the driver MMIC efficiency will be on the order of $n = 0.5$. It is evident from Fig. 13 that power MMICs with gain greater than ∼13 dB are required to ensure that the SSPA efficiency is largely independent of the driver MMIC efficiency.

3. MMIC and Combiner Match. Good match in the RF path (including the MMICs) is required not only to minimize return loss, but also to ensure that the phase ripple specification is met. The energy trapped between two reflection planes in the RF path can beat against each other and cause amplitude and phase ripple versus frequency. The magnitude of these ripples can be shown to be a function of the mean reflection coefficient of the two reflection planes.

A plot of the phase ripple versus average impedance match at the reflection planes is shown in Fig. 14. As can be seen, a minimum average match of 16 dB must be maintained in the RF path to ensure that the phase ripple due to mismatch is less than the required 3 deg.

4. Requirements Summary. Based on the SSPA requirements listed in Table 1 and the previous discussion, the MMIC and power combiner requirements can be summarized as given in Tables 7 and 8.

III. Conclusion

In summary, this article developed MMIC and power-combiner requirements required for an SSPA architecture to reach the goal of 120 W with a 40 percent PAE over the 31- to 36-GHz band. The analysis results of three power-combiner designs that meet the above requirements will be presented in an article in the next issue of *The Interplanetary Network Progress Report*.

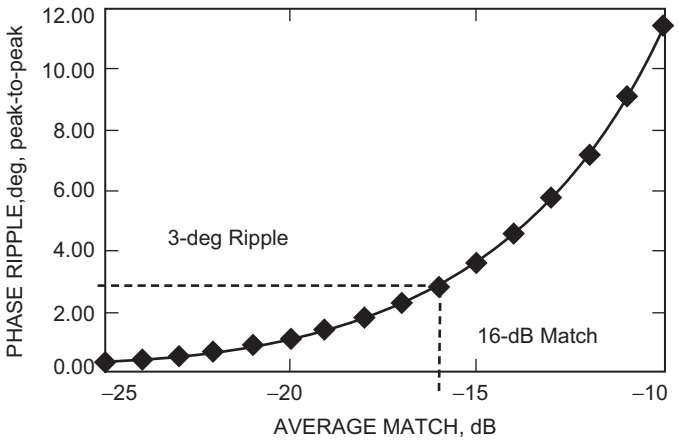

Fig. 14. Magnitude of phase ripple resulting from energy trapped between two reflective interfaces, plotted versus the average impedance match at these interfaces.

Table 7. Initial power MMIC requirements.

Parameter	Value
Output power	6–12 W minimum
Bandwidth	>10 percent
Gain	13 dB minimum
Gain variation	1.5 dB maximum (unit-to-unit variation)
Phase variation	10 deg maximum (unit-to-unit variation)
PAE	49–56 percent minimum
Port match	7 dB minimum (assuming a combiner port match >25 dB)

Table 8. Initial power-combiner requirements.

Parameter	Value
No. of combining ports	16–32
Bandwidth	>10 percent
Total insertion loss	1.0 dB maximum, including MMIC package and transition (<0.55 dB, excluding MMIC package and transition)
Port match	25 dB minimum
Amplitude balance	0.5 dB maximum
Phase balance	5 deg maximum
Isolation	10 dB minimum port–port isolation generally desired for increased tolerance to MMIC variations and failure

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