Frequency-Agile Multi-Channel X-Band Coherent Receiver/Transmitter for the Advanced Deep Space Transponder

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Uplink and downlink Advanced Deep Space Transponder breadboards have been constructed using voltage-controlled oscillator (VCO) phase-locked loop (PLL) frequency synthesizers. Results indicate wideband frequency tuning, demonstrating a 40 percent improvement over prior dielectric resonator oscillator (DRO) components and covering the entire deep-space and near-Earth X-band allocations (7145–7235 MHz for uplink and 8400–8500 MHz for downlink). Phase noise performance is well within current transponder specifications. Coherent turnaround has been demonstrated in the Deep Space Network X-band channel allocation. Particular emphasis has been devoted to loop filter design. Results show excellent agreement between expected and observed performance and clearly indicate excellent promise for the use of VCO PLL technology in spacecraft transponder applications.

I. Introduction

As outlined in the JPL *Strategic Technology Plan, 2005*,[3] future flight projects will require efficient use of Deep Space Network (DSN) resources. High data rate and frequency-agile telecommunications designs will be necessary to accommodate the high volume of data from an increased number of spacecraft assets. Many of these assets will be working in proximity to each other and must be capable of crosslink, or spacecraft-to-spacecraft, communications. NASA technologists envision that spacecraft will continue to build a network of nodes and relay stations throughout our solar system.

With this destination in mind, it becomes clear that telecommunications will become significantly more complicated. With a finite allotted spectrum for X-band (7145–7235 MHz uplink, 8400–8500 MHz downlink) and Ka-band (34,200–34,700 MHz uplink, 31,800–32,300 MHz downlink) operations and an increasing number of users, bandwidth will become a very valued resource. As with any complicated network, the ability to adjust operations to changing demands and unanticipated circumstances will be critical.

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[1] Flight Communications Systems Section.

[2] Autonomy and Control Section.

[3] *Strategic Technology Plan, 2005*, internal document, Jet Propulsion Laboratory, Pasadena, California, December 7, 2004.

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Current deep-space missions utilize the Small Deep Space Transponder (SDST) for direct-to-Earth (DTE) communications. The SDST has been used successfully on a number of missions, but the original design is over 12 years old and it will not be able to meet all the requirements for future missions. Upgrades have been made to the original SDST for changing project needs over the years; however, these upgrades and increased functionality are limited by original architectures that would be extremely expensive and time consuming to change. Research and development to prepare for future needs are critical to success. Current radio frequency integrated circuit (RFIC) technology and lessons learned from the successful JPL SDST program enable the development of an enhanced transponder design to meet the projected future needs of NASA. Improved performance and flexibility can be obtained while reducing mass, power consumption, and size. This rationale has led to funding for technology development of the Advanced Deep Space Transponder (ADST) over the last 3 years.

II. Design Rationale

Primary design drivers for the ADST have been enhanced capability, increased flexibility, and reduced cost. A primary improvement to transponder flexibility focuses on frequency agility. The frequency allocation for deep-space communications at X-band is 7145–7190 MHz for uplink (Earth to space) and 8400–8450 MHz for downlink (space to Earth). These frequency bands have been divided into 35 channels to enable multiple missions to simultaneously utilize the allocated spectrum. Currently, the SDST is pretuned to an assigned communications channel, and all communications throughout the life of the mission take place at the assigned frequency. The SDST does not have the capability to change its operating frequency after it has initially been set, and this additional flexibility is a key improvement provided by the ADST. As more missions are active simultaneously, many of them interacting with each other—such as Mars Exploration Rover (MER), Mars Reconnaissance Orbiter (MRO), and Mars Science Laboratory (MSL)—the ability to adjust communications frequencies easily and at any point during the lifetime of a mission becomes critical. Frequency-agile transponders will enable mission operations to adjust DSN usage in what will become an extremely complicated network.

A frequency-agile transponder also will result in reduced manufacturing costs. A larger quantity of identical transponders could be purchased at one time because they would not consist of mission-specific parts. This would allow a significant reduction in necessary project documentation as well as hands-on labor costs. Due to advances in RFIC and monolithic microwave integrated circuit (MMIC) technologies, the ADST architecture is simpler than previous transponders and requires fewer parts. ADST parts that are required are smaller and of lower mass.

As part of the ADST development, dielectric resonator oscillators (DROs) were designed for transponder uplink (receiver) and downlink (transmitter) frequency synthesis. DRO technology has been used extensively in previous transponders, but past designs did not require the broad tuning range that a frequency-agile transponder does. Broad tuning is very difficult with DRO architectures, and it is well-known that it degrades DRO phase noise performance. These complications have been observed in ADST DRO prototypes, motivating investigations into alternate technologies.

One of these alternate technologies was the voltage-controlled oscillator (VCO). VCO technology boasts broader tuning range capability, and recent technological advances have made it a viable alternative to the DRO for many oscillator applications. Phase noise issues that in the past have dissuaded many engineers from its use have been eliminated. This article will present results obtained from VCO breadboard synthesizers, ultimately justifying the use of VCO technology in the ADST and demonstrating coherent transponder operation.

III. Theory

The transponder front end will detect, track, and downconvert an uplink signal so it can be digitally processed. A coherent receiver signal must be synthesized in order to downconvert the uplink signal while maintaining coherent turnaround. This receiver synthesizer must have sufficient frequency range to match any frequency in the DSN X-band uplink frequency range for frequency-agile operation. The front end also must have low phase noise in order to accurately detect and lock on to weak signals. This is especially important for coherent operation, which allows for mission operators to perform spacecraft ranging and Doppler measurements. The basic architecture for the ADST is shown in Fig. 1, where the front end is the top half of the figure.

An important part of this front-end architecture is the uplink stage necessary to extract command data from the 7.2-GHz carrier. Downconversion must be designed with an uplink frequency synthesizer capable of following the uplink phase so a coherent signal can be transmitted back to Earth. A broad synthesizer tuning range is essential in order to cover the entire X-band uplink DSN frequency spectrum. This is the first location in the transponder architecture where VCO technology will replace prior DRO designs. The second location is on the transmitter side of the transponder, where an 8.4-GHz signal

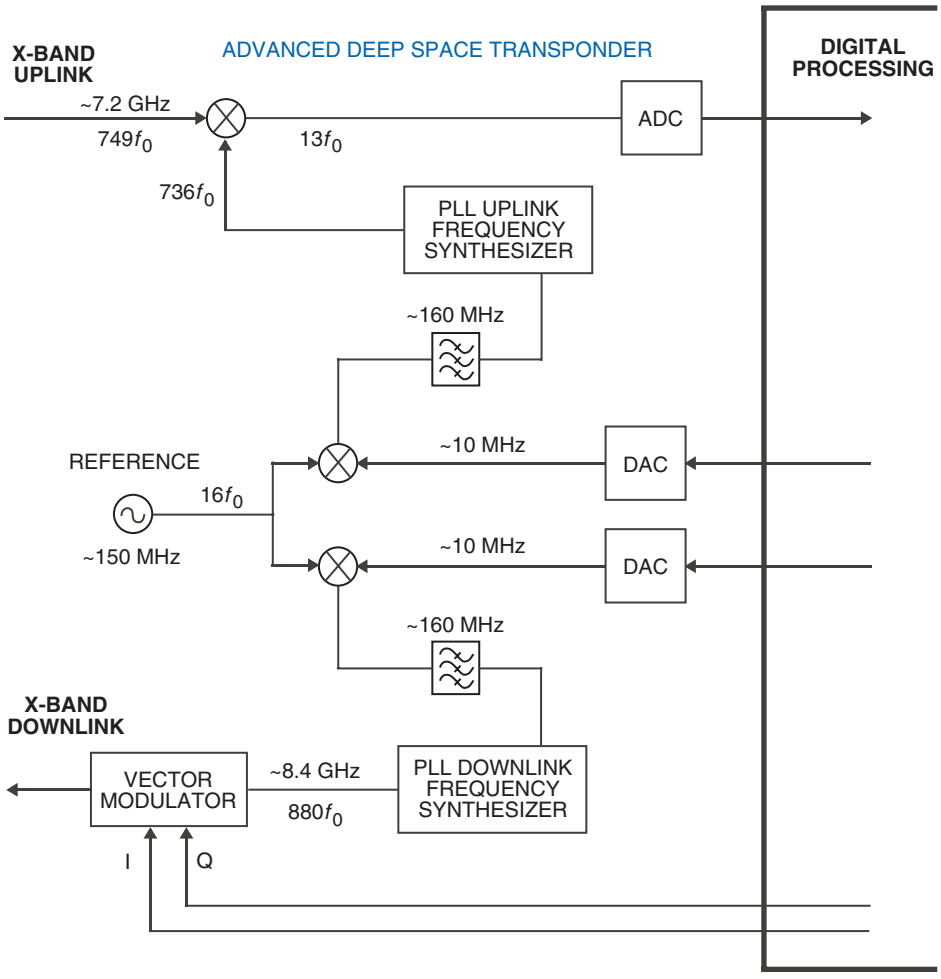

Fig. 1. Basic ADST architecture. (ADC = analog-to-digital converter; DAC = digital-to-analog converter.)

must be generated for downlink transmission. This signal will be modulated with a vector modulator capable of a variety of advanced modulation techniques. To be useful in the ADST architecture, these VCO synthesizers must have broad tuning range and low phase noise. In addition, they should be highly integrated, utilizing modern technology to minimize size, weight, and costs.

Two of these VCO phase-locked loop (PLL) synthesizers are necessary in the architecture of Fig. 1. These synthesizers also could be constructed as vastly smaller MMICs. For this reason, Hittite Microwave Corp. was contracted to design two VCO PLL MMIC dies. It is projected that these MMIC chips will be roughly 8 mm^2, weighing less than 2 grams fully packaged. They will be developed over the next several years, funding permitting. The standard PLL synthesizer architecture consists of several components and is shown in Fig. 2.

The loop filter serves to reduce system noise and block undesirable spurs that may disrupt VCO PLL performance. System noise depends heavily on the characteristics of this component. System bandwidth is also set by the filter and must be carefully selected based on reference phase noise, free-running VCO phase noise, and the probability of the loop locking on undesired spurs. For our design, the PLL filter consisted of an active, differential-input, low-pass filter. A standard architecture for this type of filter is shown in Fig. 3.

Filter impedance and both open- and closed-loop gain equations are easily calculated and have been provided in Eqs. (1) through (3), respectively. These equations have a key role in PLL phase noise and depend on values chosen for R_1, R_2, and C_f, shown in Fig. 3. Full derivations of these formulas have been provided by Banerjee [2]:

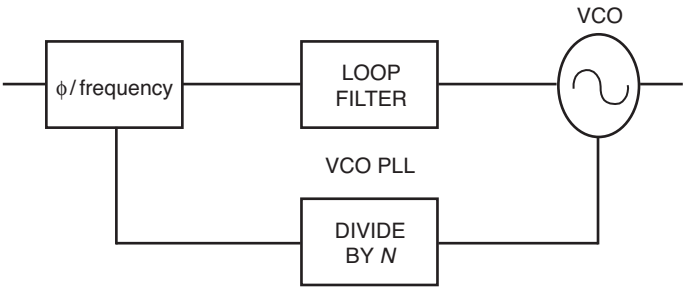

Fig. 2. Basic PLL configuration.

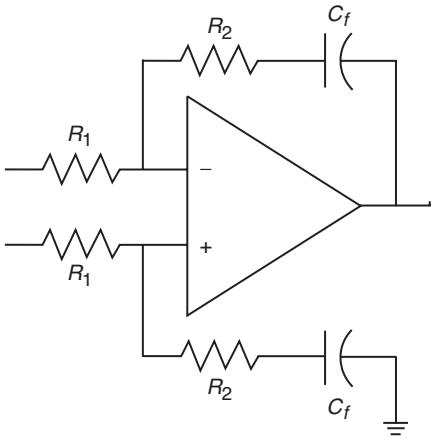

Fig. 3. Loop filter configuration.

$$Z(s) = \frac{1 + C_f R_2 s}{C_f R_1 s} \tag{1}$$

$$G(s) = \frac{K_{pfd} K_{vco} Z(s)}{s} \tag{2}$$

$$CL(s) = \frac{G(s)}{1 + \frac{G(s)}{N}} \tag{3}$$

where K_{pfd} is the proportionality constant for the phase/frequency detector (PFD) in volts/radian, K_{vco} is the proportionality constant for the VCO in radians/second-volt, N is the value of the divider from Fig. 2, and s is the Laplace transform complex variable.

Typically, the single-sideband (SSB) phase noise of the PLL synthesizer will remain at the noise level of the reference source for frequencies below loop filter bandwidth. Phase noise for frequencies higher than the loop filter bandwidth is set by the free-running phase noise of the VCO. Once the loop is locked, the VCO will closely follow low-frequency characteristics of the input signal that are passed through the loop filter. Higher-frequency reference noise is blocked by the filter, and the VCO noise characteristics dominate for these higher frequencies. Loop filter bandwidth is set not only to minimize noise but also to avoid locking on incorrect signals. A sample SSB phase noise plot has been provided in Fig. 4. The PLL bandwidth has been set to minimize synthesizer phase noise. This corresponds to the case in which the bandwidth is set at the frequency intersection of the phase noise plots of the reference source and the free-running VCO.

IV. Breadboard Design

Current specifications for the Advanced Deep Space Transponder synthesizer development are listed in Table 1. The most important specifications are for tuning range and phase noise. It is essential that the VCO PLL synthesizers cover the entire DSN X-band frequency allocation while not adding substantial phase noise to the system.

A picture of the 7-GHz receiver DRO prototype is shown in Fig. 5. This oscillator is constructed on a 20-mil alumina substrate, and tuning is controlled by coarse- and fine-tuning voltages. Although the

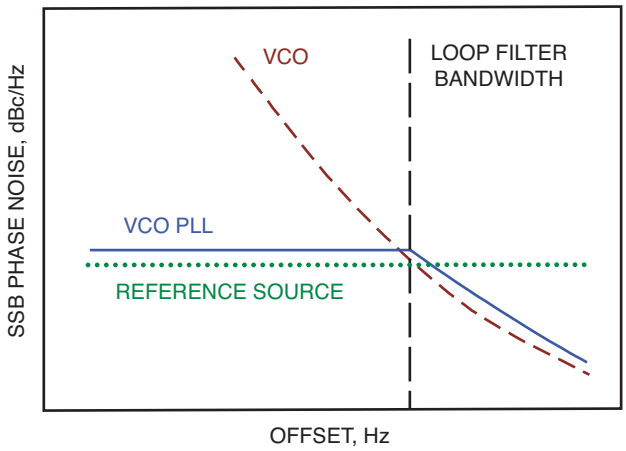

Fig. 4. Expected SSB phase noise characteristics.

Table 1. Receiver/transmitter specifications.

Synthesizer parameter	Specification
X-band RF frequency range:	
X-band receive frequency range	∼7019 MHz to 7069 MHz
X-band transmit frequency range	∼8400 MHz to 8450 MHz
Tuning range	>100 MHz
Output power level	+10 dBm ± 1.0 dB
SSB phase noise	< −50 dBc/Hz at 1 kHz from carrier
Frequency stability versus temperature	±2 ppm/deg C maximum
DC supply frequency pushing (±5% Vdc)	100 kHz maximum
Load frequency pulling [2:1 voltage standing wave ratio (VSWR)]	100 kHz maximum
Harmonics	< −33 dBc
Spurious signals	< −80 dBc
Operating temperature range	−55 deg C to +75 deg C
Output impedance	50 ± 5 ohms, nominal
DC bias current at +5 Vdc	30 mA
Coarse electronic tuning control voltage	+3 V ± 2 V maximum
Fine-tuning control voltage	+3 V ± 2 V maximum

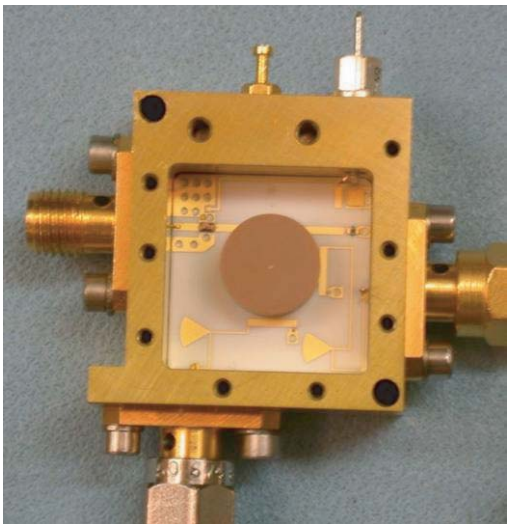

Fig. 5. Prototype receiver DRO.

uplink and downlink DRO prototypes exhibited some tuning range, neither was able to cover the entire DSN X-band uplink or downlink tuning ranges.

Both VCO PLL synthesizers have the same basic architecture, shown in Fig. 6. A photograph of one of the synthesizer breadboards is shown in Fig. 7. Although the VCO PLL breadboard is larger than the DRO prototype, future synthesizers easily can be reduced in size and will weigh significantly less than the DRO. The receiver and transmitter synthesizers utilize different VCOs, and the divide-by-N integer is set to 6 on the uplink synthesizer and to 7 for the downlink synthesizer. Outputs from a Nallatech Xilinx field programmable gate array (FPGA) board are mixed with a 143-MHz clock signal and used as

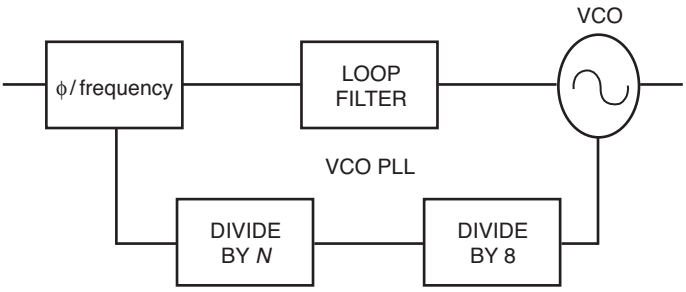

Fig. 6. VCO PLL block diagram.

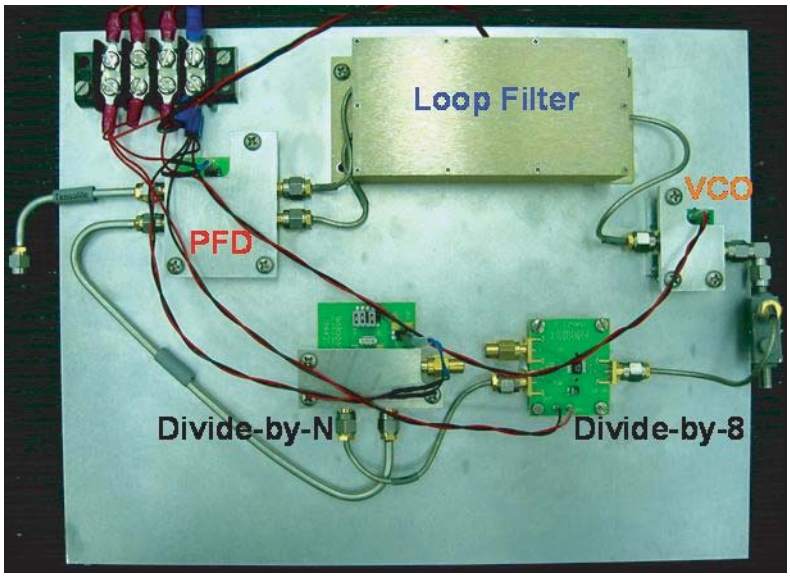

Fig. 7. VCO PLL synthesizer.

reference sources for the VCO PLL frequency synthesizers. Xilinx digital programming and synthesizer divide-by ratios combine to meet the necessary DSN X-band channel assignments.

An active, differential-input loop filter was constructed using a Texas Instruments high-speed low-noise operational amplifier. The architecture of this type of filter has been shown in Fig. 3. A MATLAB program has been written that fully characterizes the loop filter and relates component values to a 3-dB loop bandwidth. This program has been used to design and construct a variety of loop filters corresponding to different desired loop bandwidths. A list of constructed loop filters is given in Table 2. The loop filter plays an important role in the overall phase noise of the PLL system and should be chosen carefully. This will be discussed in more detail in the results section of this article, when phase noise data are presented.

A phase noise test set was used for phase noise measurements in accordance with standard procedures. This test set utilizes a dual-downconversion architecture and was used in conjunction with a spectrum analyzer and a signal generator. A signal generator was used to provide a simulated radio frequency (RF) uplink signal to the ADST breadboard.

Table 2. Loop filters built for the VCO PLL breadboard.

Filter	Expected bandwidth, kHz	Observed bandwidth, kHz
A	N/A	∼200
B	N/A	∼480
1	50.73	∼60
2	28.26	∼30
3	28.26	∼30

V. Results

The ADST breadboard is shown in Fig. 8. The uplink synthesizer that is used to downconvert the uplink signal is the plate on the left, and the downlink synthesizer is on the far right. The center plate consists of the mixers, amplifiers, and filters necessary to provide coherent references to the VCO PLL synthesizers in the designated frequency ranges. The Xilinx FPGA board is in the blue case on the far left of the photograph. This board was controlled using Nallatech FPGA software.

The VCO PLL synthesizers were much easier to design and test than their DRO counterparts. Many aspects of DRO implementation are vague and unpredictable, even for a very experienced DRO engineer, and achieving desired operation typically is a painstaking process. The VCO synthesizers were far more stable and easier to use.

Both of the VCO synthesizers significantly exceed tuning-range design requirements. Uplink and downlink X-band DSN frequency ranges are completely covered for both deep-space and near-Earth bands. Frequency output is close to a linear function of tuning voltage and is continuous throughout the tuning range. Deep-space uplink and downlink synthesizer tuning comparisons between DRO and VCO synthesizers are shown in Fig. 9. Clearly, the DROs do not meet transponder full-band tuning requirements. The VCO synthesizers not only cover 100 percent of the deep-space DSN X-band spectrum, but they also cover the near-Earth spectrum. In addition, it is very difficult and time consuming to adjust DRO frequency operation, and this is not necessary with the VCO synthesizers. The synthesizers continuously track the reference signal throughout the entire tuning range of the VCO.

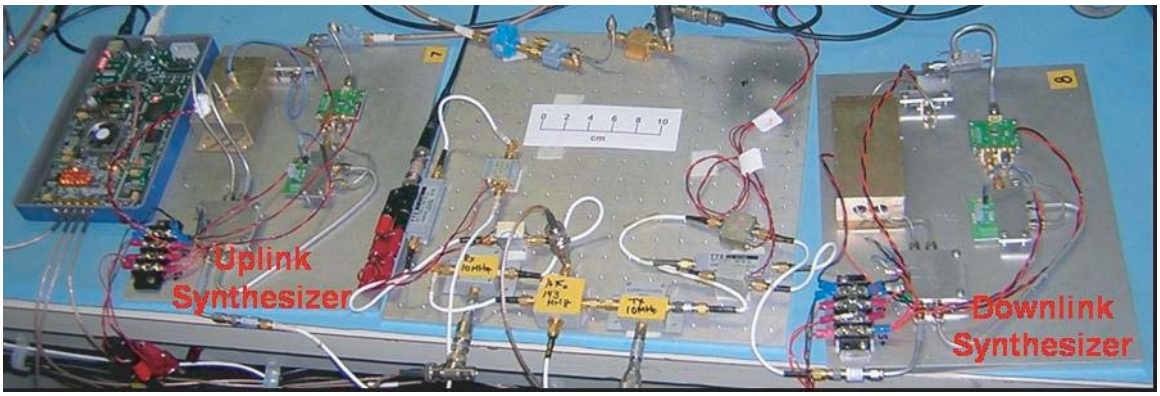

Fig. 8. Advanced transponder with uplink and downlink VCO PLL synthesizers.

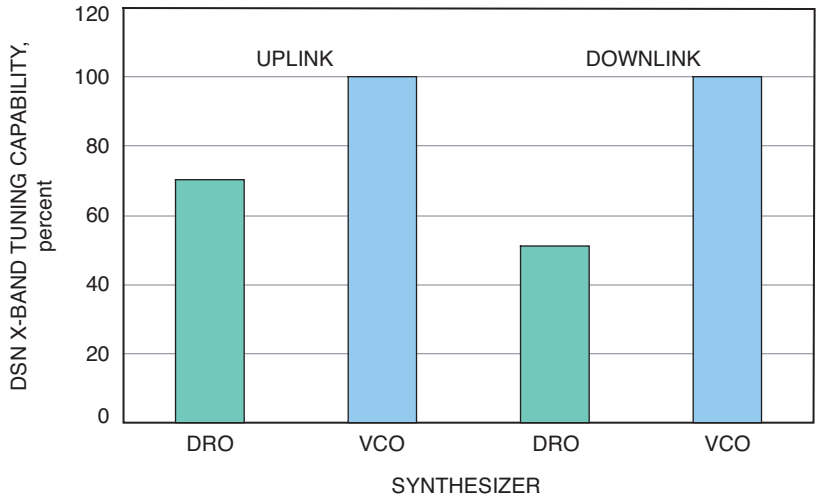

Fig. 9. Tuning comparisons for the DRO and VCO synthesizers.

An important performance specification for transponder operation is system phase noise. Synthesizer phase noise is a key component to total transponder phase noise and, therefore, is carefully tracked. Since VCO technology allows for a much larger tuning range, initial concerns were that the phase noise might be higher. Although breadboard phase noise indeed is slightly greater than the DRO prototypes, VCO specifications from the vendor, Hittite Microwave Corp., demonstrated phase noise performance comparable to the DROs [1,3]. Observed phase noise performance and vendor phase noise specifications are given in Fig. 10.

Results indicate that phase noise is better than current transponder specifications. Phase noise functional specifications for the Mars Reconnaissance Orbiter SDST receiver and exciter are ≤ -20 dBc/Hz at 1 Hz, ≤ -60 dBc/Hz at 100–1000 Hz, and ≤ -70 dBc/Hz at 1–100 kHz. Note that the synthesizer would follow the reference for frequencies below $\sim$100 kHz. Phase noise performance closer to vendor specifications is expected in smaller, future designs. Discrepancy between manufacturer-specified and laboratory-tested phase noise for the VCO synthesizers most likely is due to various additional system components such as loads, power dividers, power supplies, and cables. The tuning and power supply ports of the VCO, for example, are especially sensitive to noise.

In order to fully characterize synthesizer performance, the VCO synthesizers were locked to a signal generator reference source. This was done to verify phase noise performance with theoretical operation, as well as to adjust loop filter parameters. Both uplink and downlink synthesizers exhibited nearly identical performance; this is shown in Fig. 11.

According to PLL theory, the system phase noise should follow the reference source for frequencies lower than the loop bandwidth, beyond which it will follow the free-running VCO noise. Phase noise plots for the signal generator and the free-running VCO have been included in Fig. 11. The loop filter bandwidth has been chosen such that the loop bandwidth is approximately 200 kHz. This was selected because it is the frequency intersection of the reference source and free-running VCO phase noise curves. This choice results in minimal system phase noise. It is clearly seen from the plots that the phase noise for both the receiver and transmitter synthesizers closely follow expected performance. Note that there is a 1.34-dB difference between the reference curves for the receive and transmit synthesizers. This is due to the different division ratios of the phase-locked loops (48 and 56).

Coherent turnaround was demonstrated with the VCO receive and transmit synthesizers. A signal generator was used to simulate an uplink signal that was downconverted with the output from

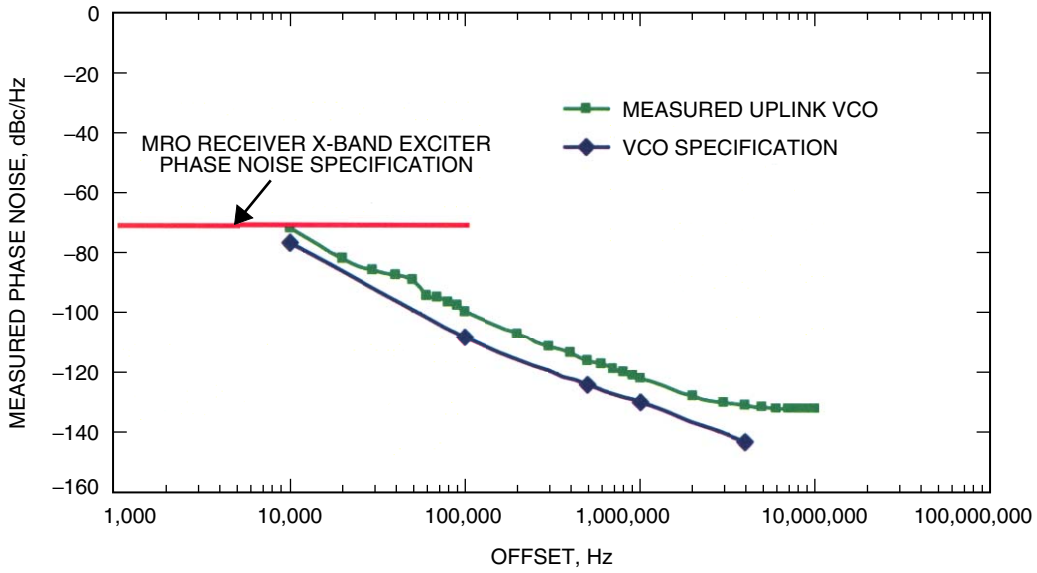

Fig. 10. Part specification and measured VCO free-running phase noise.

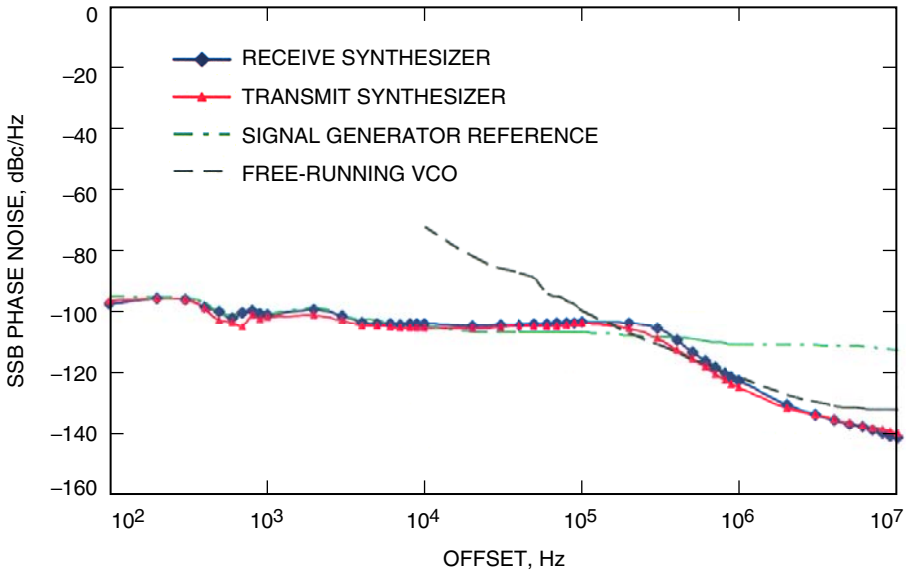

Fig. 11. Receive and transmit VCO synthesizer phase noise characteristics.

the receive VCO synthesizer breadboard. This intermediate frequency (IF) signal then was passed to the Xilinx FPGA, which output the two coherent reference signals that were mixed with the system 143-MHz clock and passed as the reference inputs to both VCO PLL synthesizers. Xilinx programming was adjusted for transponder operation in the DSN X-band allocation.

Phase noise measurements for coherent operation have been provided in Fig. 12. Generating the coherent input to the VCO synthesizers involved the Xilinx FPGAs and added nearly 10 dB of system phase noise. This most likely is due to the mixers, filters, and amplifiers necessary for this architecture that were not needed for the previous measurements of Fig. 11. This also could be due to numerically controlled oscillator (NCO) noise from the Xilinx FPGA.

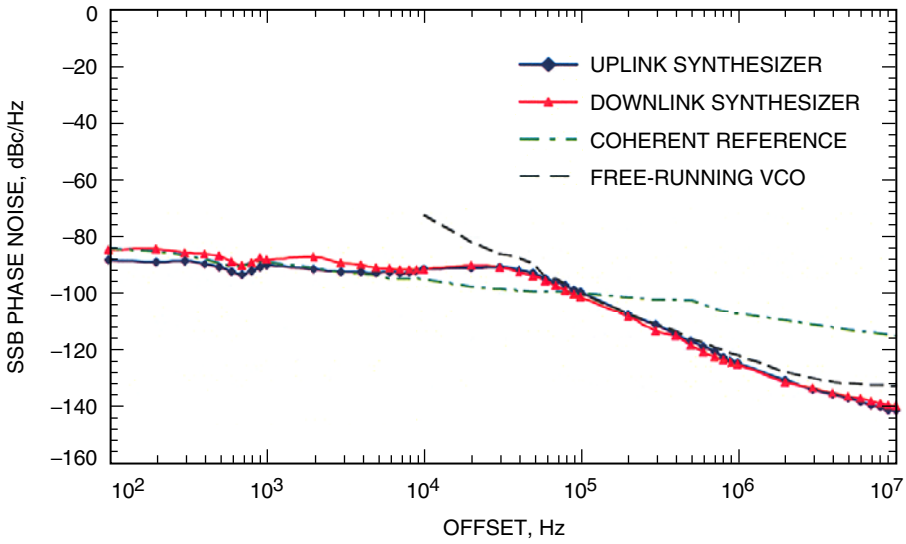

Fig. 12. Coherent receive and transmit synthesizer characteristics.

The importance of loop bandwidth selection has been discussed previously. The selection of loop bandwidth has a significant impact on system noise and overall performance. The loop filter is an easy component to replace and adjust, and for these reasons significant time was spent in engineering the loop filter. The plots shown in Fig. 13 clearly show the effect of loop filter bandwidth. This figure is very similar to Fig. 11; however, an alternative loop bandwidth curve (filter 3) corresponding to 30 kHz has been included. A 15-dB difference can be seen between the two phase noise measurements at 30 kHz.

Recall that minimum phase noise is achieved when the loop bandwidth is set at the frequency intersection between the reference source and free-running VCO phase noise curves. In Fig. 13, this is the intersection between the black and green curves and is at 220 kHz. From Table 2, it can be seen that the loop bandwidth using filter A (200 kHz) is much closer to this value than the bandwidth for filter 3 (30 kHz). The system phase noise begins to follow the free-running VCO phase noise at the loop bandwidth. This means that at 30 kHz the system phase noise rises up to follow the free-running VCO curve. A 15-dB improvement is observed using filter A, representing a wiser selection of loop bandwidth.

Receiver coherent phase noise plots have been collected in Fig. 14 for the loop filters designed and tested on the synthesizer breadboards. This figure shows the loop bandwidths characteristic of each filter, corresponding to Table 2.

VI. Conclusions

The Advanced Deep Space Transponder breadboard performed quite well using the RFIC VCO receive and transmit synthesizers, and ADST development will proceed using this VCO technology. Measured VCO synthesizer performance demonstrated significantly broader tuning capability than the DRO prototypes, covering the entire DSN X-band allocation for both deep-space and near-Earth bands.

Measured VCO synthesizer breadboard phase noise was well within advanced transponder specifications and comparable to that of prior DRO prototypes. In addition, further improved performance is expected in future synthesizer prototypes.

Coherent turnaround was demonstrated in the DSN X-band channel allocation. Advanced transponder performance closely followed expectations, and significant VCO synthesizer design and measurement capability were developed under this effort. Loop filter design and loop bandwidth selection were carefully

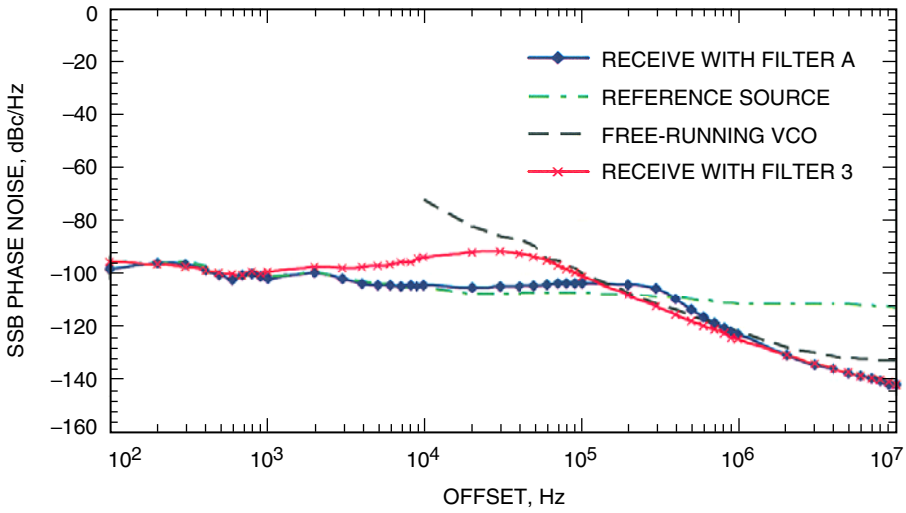

Fig. 13. Receive synthesizer showing the effect of loop filter bandwidth.

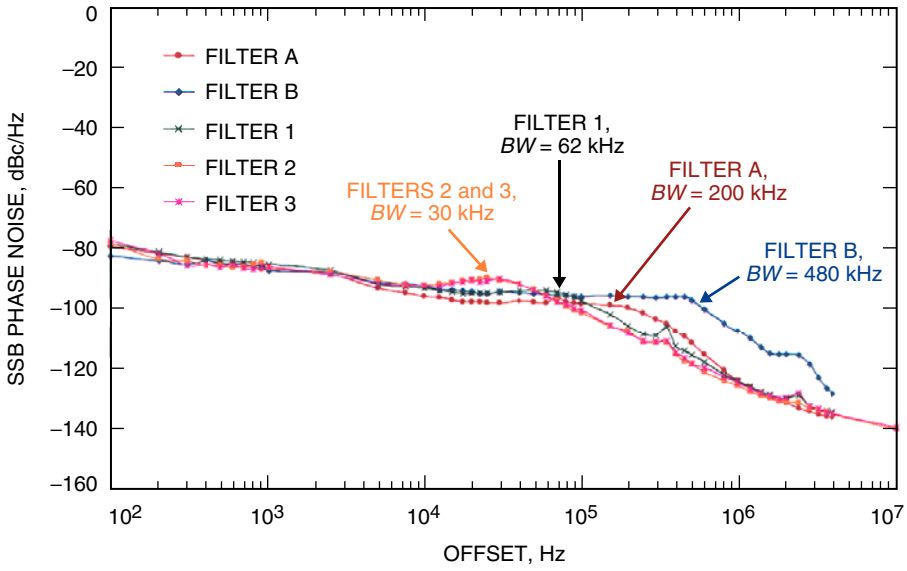

Fig. 14. Receiver phase noise plots showing loop bandwidths for constructed filters.

investigated and fully understood. MATLAB code was written according to phase-locked loop theory to aid in loop filter design, and this code was fully validated in the laboratory. Three synthesizer breadboards were constructed and integrated in the advanced transponder, as well as five loop filters.

VII. Future Work

Future work will focus on miniaturizing the front end and further integrating transponder components. Ultimately, a MMIC die fabricated based on designs finalized in fiscal year 2006 will comprise a miniaturized, fully integrated front end. Digital software will be finalized and integrated into the front end to allow for agile, reprogrammable operation. In addition, downlink vector modulator components and Ka-band architectures will be infused in future breadboards. It also would be highly desirable if there were one VCO that could adequately handle all necessary X-band frequencies for uplink and downlink

in both deep-space and near-Earth frequency bands. Such a VCO would add significant flexibility to the next-generation advanced transponder as well as significantly reducing manufacturing costs. Conclusions reached from this work indicate that development of such a VCO may certainly be feasible and should be investigated.

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