Physical Temperature of the Active Region in Cryogenically Cooled Indium Phosphide High-Electron Mobility Transistors

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This article describes an experiment to measure the physical temperature of the active region of indium phosphide high-electron mobility transistors (HEMTs) while varying the chip temperature from 15 K to 50 K. The Pospieszalski HEMT device noise model predicts that the device noise temperature is dependent on the square root of the device-gate physical temperature. For this experiment the three-terminal HEMT device was separated into 2 two-terminal devices. One device was used as a heating element while the other served as a temperature-sensing element. The results indicate that the active device region is close to the chip ambient temperature.

I. Introduction

In recent years, cryogenically cooled indium phosphide (InP)-based high-electron mobility transistor (HEMT) low-noise amplifiers (LNAs) have demonstrated record low-noise temperatures from microwave to millimeter-wave frequencies (1 GHz to 100 GHz). These HEMT LNAs are employed in the Deep Space Network (DSN) at 8.4 GHz and 32 GHz and are the lowest-noise cryogenically cooled InP devices currently available [1].

This cryogenic InP HEMT technology was developed under contract to Northrop-Grumman Corporation (NGC), formerly TRW. The lowest noise devices were delivered in October 1999. The delivery consisted of three wafers, designated as CRYO3/A-Z1 (wafer numbers 4074-090, 4099-040, and 4099-041), referred to herein as CRYO3. The three wafers used the same mask set, and the devices selected for this experiment were taken from wafer 4099-041. This wafer provided the highest device yield and demonstrated the lowest device noise temperatures at cryogenic temperatures. These InP HEMT devices are composed of multiple semiconductor and metallic-alloy layers ranging in thickness from 1000 nm for the InP and indium aluminum arsenide (InAlAs) buffer layers down to 4 nm for the InAlAs spacer [2]. Figure 1 shows the device layer cross section used for this study.

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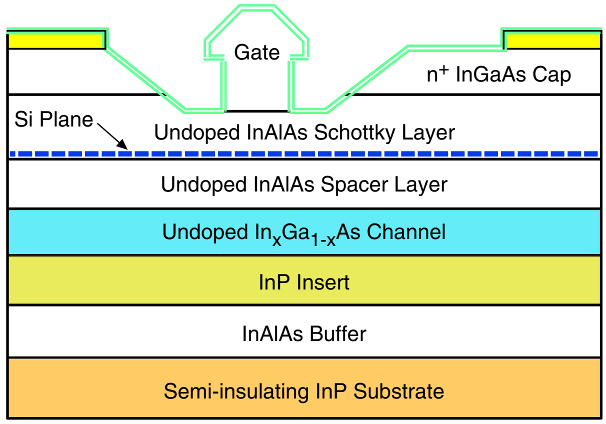

Fig. 1. Cross-sectional view of molecular beam epitaxy-grown NGC InGaAs/InAlAs/InP HEMT.

These devices show better than an order of magnitude reduction in noise temperature when cooled from 300 K to 15 K, with most of the noise performance improvement realized in cooling from 300 K to 100 K. However, below 100 K the noise performance begins to level off [3]. Figure 2 shows the gain and noise-temperature performance at 32 GHz of three DSN cryogenic LNA modules as a function of physical temperature from 15 K to 50 K. One LNA module is a four-stage NGC InP HEMT microwave integrated circuit (MIC) using CRYO3 discrete devices from wafer 4099-041, while the other two are monolithic microwave integrated circuit (MMIC)-based modules utilizing the same CRYO3 HEMT structure grown by NGC in 2003. One MMIC module (3-stage-MMIC) uses a single three-stage LNA MMIC while the other (2xMMIC) uses two in cascade (essentially a six-stage LNA module).

Although the data in Fig. 2 show noise-temperature improvement on cooling from 50 K to 15 K, earlier gallium arsenide (GaAs)-based HEMTs showed less significant improvement in noise performance when cooled over the same physical-temperature range, shown in Fig. 3 [3].

II. Background

The thermal conductivity, κ (phonon or heat transport), of semiconductors is known to be a power function of physical temperature. In general, for bulk or macroscopic samples at low temperatures (<10 K) κ is proportional to T_n, where T is the physical temperature. The exponent n $(1.5 < n < 3)$ is dependent on sample size and material properties. For crystalline semiconductors, κ reaches a maximum around 10 K to 15 K and varies as T^{-1} at higher temperatures. As devices shrink to micrometer and nanometer dimensions, boundaries, defects, impurities, and charge carriers can severely limit κ. For GaAs samples and aluminum antimonide (AlSb)/InAs super-lattices of nanometer dimensions, κ is observed to drop by 2 to 3 orders of magnitude, and the κ peak (or maximum) increases to a higher temperature by 1 to 2 orders of magnitude in comparison with bulk samples [4]. Thus, poor heat-transport properties of nanometer-sized semiconductor devices can severely limit their performance at cryogenic temperatures.

An understanding of the heat-transport properties of HEMT structures would result in significant performance improvements at cryogenic temperatures as well as a significant increase in their frequency performance bandwidth. For example, achieving the same noise performance at a higher physical temperature, such as 50 K, would enable the use of small, cheap, efficient, and reliable cryo-coolers. Additionally, an accurate HEMT thermal transport model would accelerate the development of cryogenically cooled indium antimonide (InSb) HEMTs, which have the potential for operation up to 1 THz [5]. The objective of this work is to provide an understanding of the electronic versus thermal engineering trade-offs of hetero-structures intended for cryogenic applications by developing a technique to directly measure the physical temperature of the active regions of cryogenic, low-noise InP HEMTs.

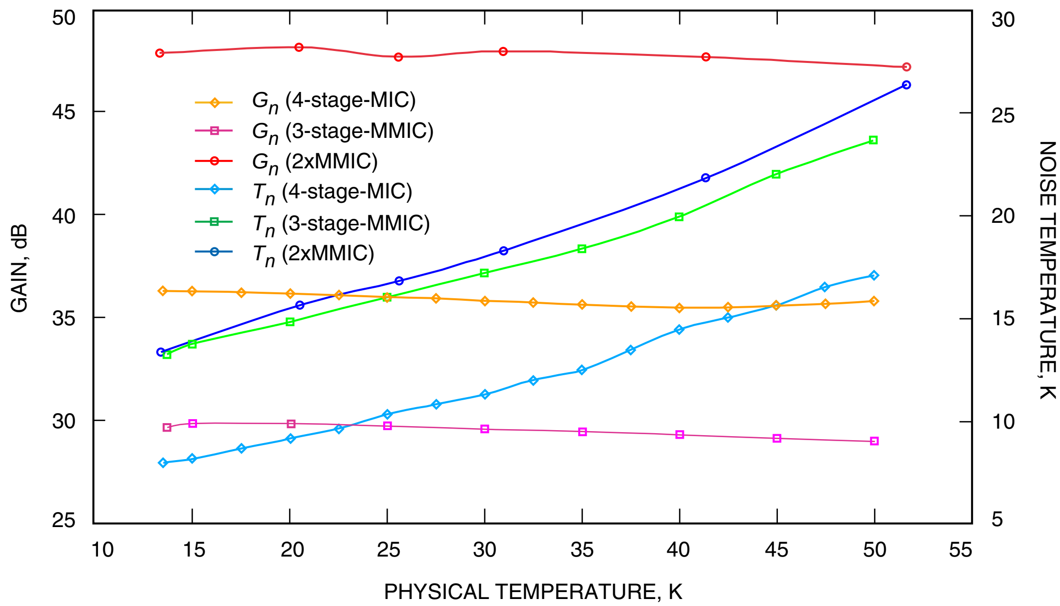

Fig. 2. Noise-temperature and gain performance versus physical temperature at 32 GHz of three LNA modules.

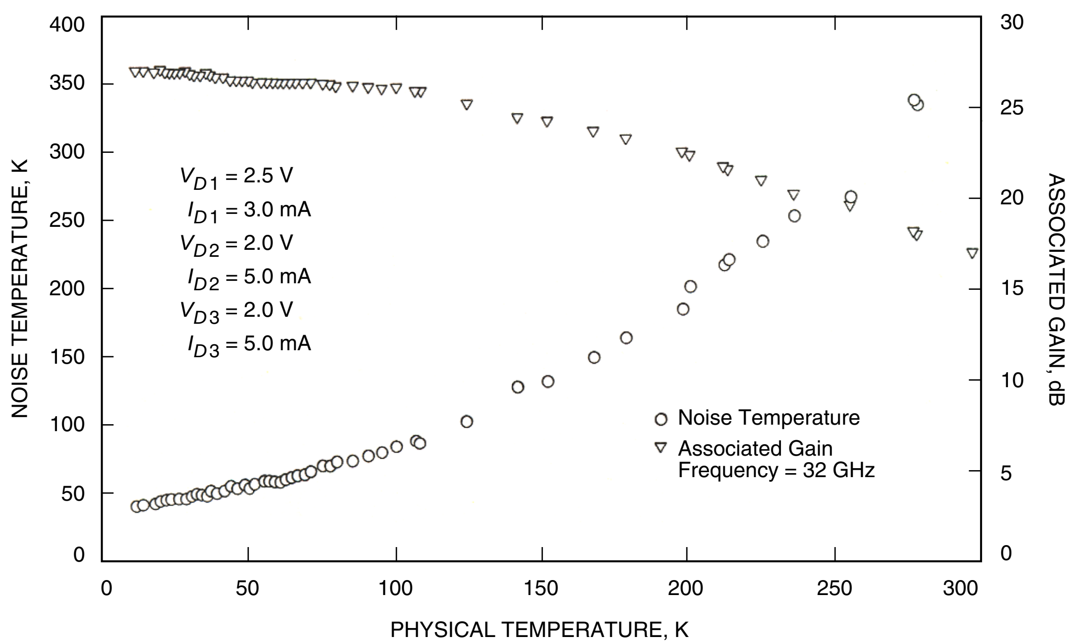

Fig. 3. Noise-temperature performance versus physical temperature of a three-stage MIC LNA utilizing GaAs HEMTs.

III. Experimental Procedure

Although there are efforts directed at measuring κ and understanding heat transport of a variety of semiconductor nano-structures and super-lattices, to our knowledge direct measurement of the physical temperature of the HEMT active region has not been attempted. This article describes an experimental measurement of the physical temperature of the active region in InP CRYO3 HEMTs at cryogenic temperatures under low-noise bias conditions. The results are then compared to measured noise temperatures.

To ensure uniformity in device dimensions and performance, devices were selected from the center of the wafer (CRYO3/A-Z1 wafer 4099-041). Two device types were selected for this study, one set with source air-bridges and the other without. The devices with air-bridges were used for cryogenic noise-temperature measurements, while the ones without air-bridges were used to measure the device physical temperature. The device layout topography is shown in Figs. 4 and 5. The device uses inter-digital four-finger gates and two-finger drains with the source terminals connected by air-bridges.

The air-bridgeless devices were mechanically separated into two separate devices, a gate to the source diode and a drain to the source resistor, using a tungsten scribe. A tempered tungsten scribe controlled by a micro-manipulator was used to remove a portion of the gate metallization, as shown in Fig. 4. Unfortunately, after 24 attempts (of 28 available devices from the wafer), only two devices survived. Of the devices that survived mechanical scribing, low residual currents of 10 percent and 1 percent of the total current between the severed terminals were present at room and cryogenic temperatures, respectively. The low residual current indicates that the two devices were not completely separated or independent.

IV. Measurement Results

Following separation, the gate diode curve (I_{gs} versus V_{gs}) between the terminals labeled Gate 3 and 4/Source 3 (as noted in Figs. 4(a) and 5) was evaluated as shown in Fig. 6. Then I_{gs} was calibrated as a function of physical temperature against a known silicon diode thermometer. Current, I_{ds}, was then driven through the drain resistor with an applied voltage, V_{ds}, between the terminals labeled Source 1/Drain 1, and the drain region physical temperature was determined by the measured value of I_{gs} of the adjacent gate diode.

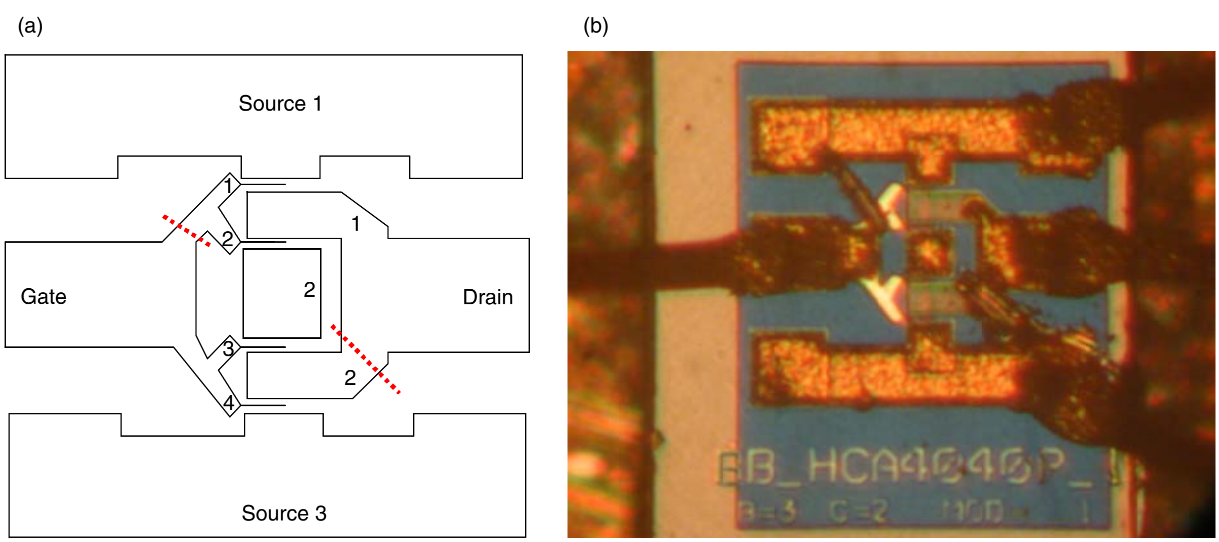

Fig. 4. The device following mechanical separation and mounting in the test fixture: (a) drawing (red dashed lines indicate the location of mechanical scribing) and (b) photograph.

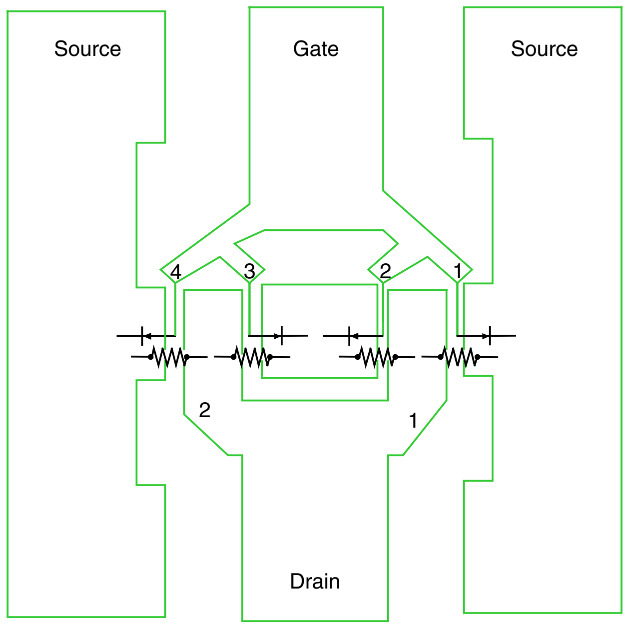

Fig. 5. Schematic representation of the HEMT device without air-bridges, showing the inter-digital, four-finger gate, two-finger drain, and source pads.

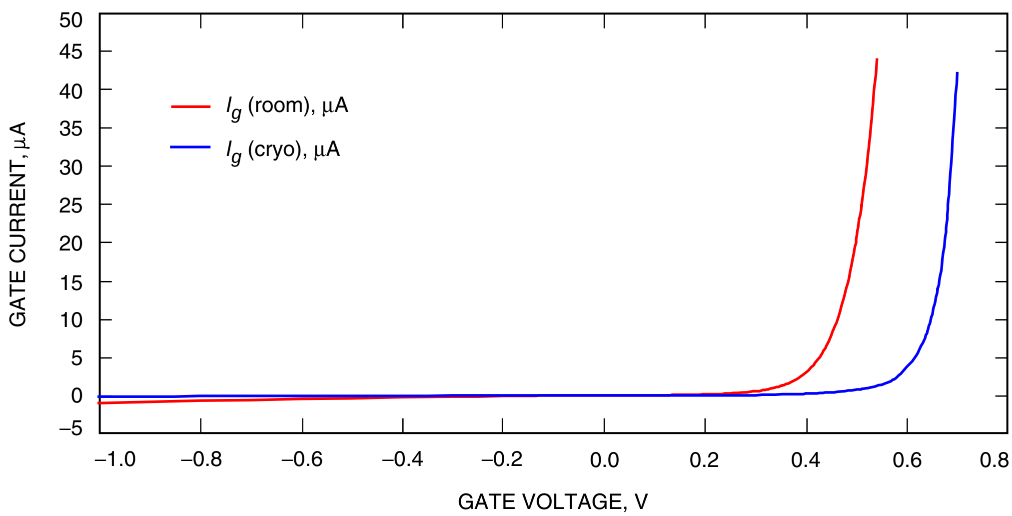

Fig. 6. Diode curve at room (red curve) and cryogenic (blue curve) temperatures.

Figure 7 displays the diode calibration curve obtained as a function of temperature for $V_{gs} = 0.6$ V and V_{ds} values of 0.0 V and 0.5 V along with their sensitivity curve (or derivative with respect to T). At the lowest temperatures of 14 K, the sensitivity curve value of the diode is about 0.003 μA/K with an associated error of ± 0.002 μA. At this temperature, the highest temperature change sensitivities are for a gate voltage of 0.6 V and a drain voltage of 0.0 V to $\sim$0.5 V. Thus, the smallest detectable temperature change is of the order of 10 K. However, at higher physical temperatures, the sensitivity was observed to improve by an order of magnitude. At the physical temperature of 50 K, the sensitivity improves to 1 K.

Figure 8 shows the current-voltage (IV) curves of the separated device at room and cryogenic temperatures. At room temperature the data indicate that the device is not completely isolated, since the IV curves are dependent on V_{gs}. For comparison, Fig. 9 shows the IV curves of the standard

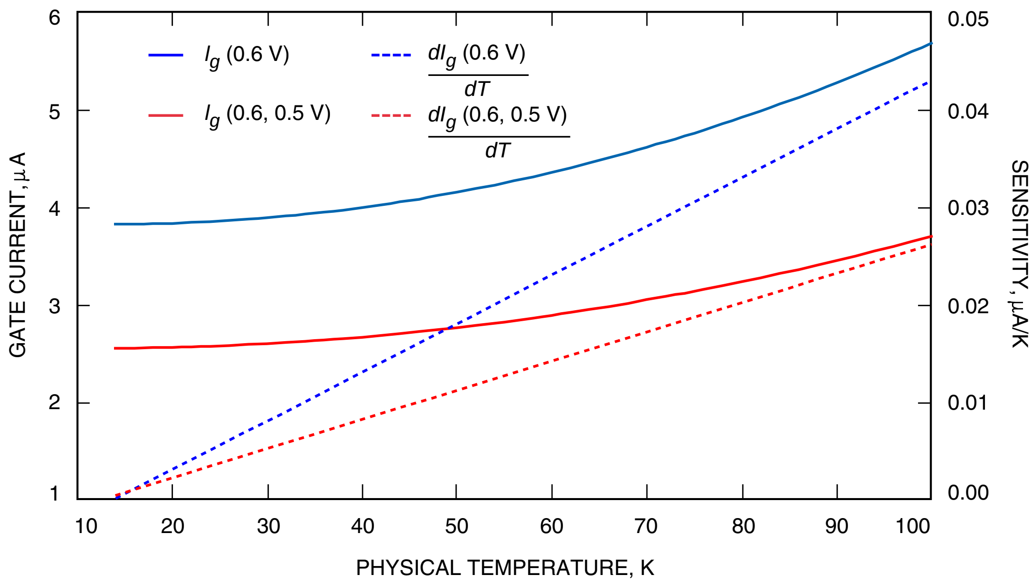

Fig. 7. Diode temperature calibration and sensitivity plots as a function of temperature.

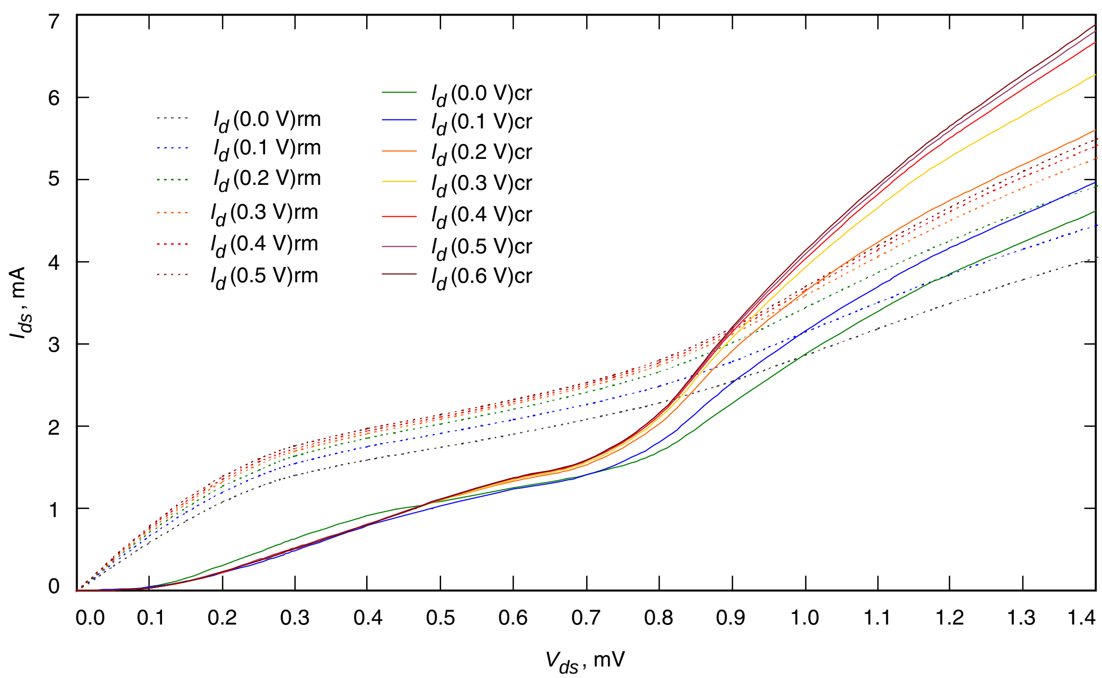

Fig. 8. IV curves of a separated device at room (dashed curves) and cryogenic (solid curves) temperatures.

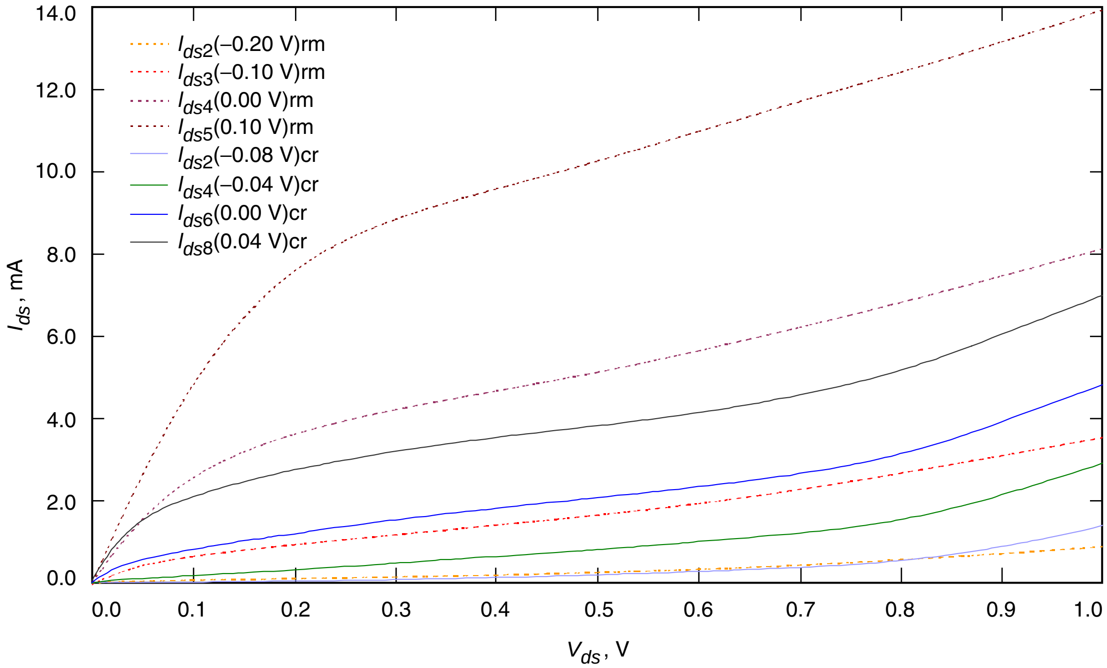

Fig. 9. Standard IV curves of the InP device with source air-bridges at room (dashed curves) and cryogenic (solid curves) temperatures.

CRYO3 device used in DSN LNAs at room and cryogenic temperatures. At cryogenic temperatures for 0.2 V $< V_{gs} <$ 0.6 V and for $V_{ds} <$ 0.8 V, the IV curves are relatively independent of gate voltage. IV curves comparable to the 14-K data were obtained for the physical temperatures of 21 K, 30 K, 40 K, and 51 K. At these higher cryogenic temperatures for $V_{gs} = 0.2$ V to 0.5 V, the gate current was measured to be relatively constant and then to start to drop as the drain voltage (drain current) was increased further, indicating that the gate current can leak into the drain-source region. The gate current leaking into the drain source is not associated with a temperature change and is taken into account.

These dc cryogenic measurements indicate that, at the lowest temperature investigated, 14 K, for a low-noise bias setting of $V_{ds} = 0.5$ V, $V_{gs} = 0.1$ V, and $I_{ds} = 1$ mA, the physical temperature of the device active region remains within 10 K of the chip physical temperature. For the highest physical temperature studied, 51 K, and the same bias settings, the active region is within 1 K of the chip temperature.

It is noted that the Pospieszalski noise model predicts that the minimum noise temperature, $T_{\min}$, is proportional to the geometric mean of the charge carrier temperature, T_d, and the gate ambient temperature, T_g. Figure 10 shows the noise temperature of the LNA models discussed in Fig. 2 along with associated curves, $T_{\text{noise}} = k_i \cdot \sqrt{T_{\text{physical}}}$. For each LNA, this model shows a reasonable fit for temperatures from 14 K to 35 K. However, above 35 K, the "square root" model temperature-dependent curves begin to diverge from the measured results.

V. Conclusion

Today the best cryogenic, HEMT MIC and MMIC LNAs use InP technology. These devices have noise temperatures of 8 K at a physical temperature of 15 K and at 32 GHz, requiring about 3 mW of power per gain stage for operation. All of the device parameters are engineered and optimized for room-temperature operation. Poor thermal heat transport in hetero-structures could limit noise performance at cryogenic temperatures.

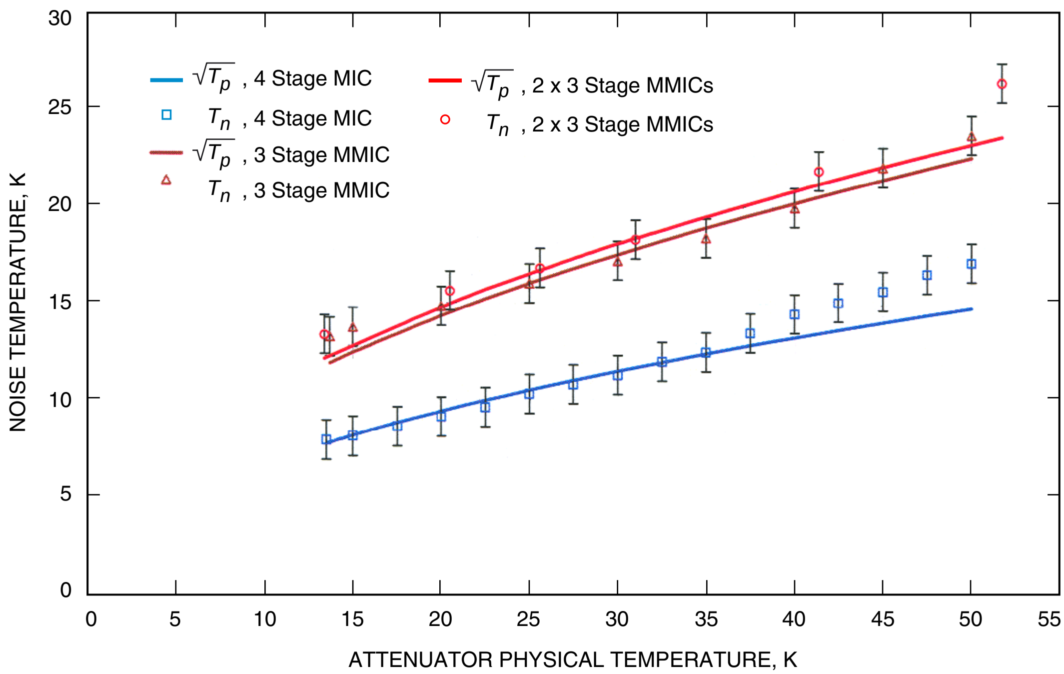

Fig. 10. Comparison of the Pospieszalski noise model to measured noise temperatures of InP HEMT LNA modules as a function of physical temperature.

Subsequent research would focus on optimizing the device thermal conductivity, lowering the bias power, and optimizing its transconductance for low-noise and maximum-gain operation near 50 K or higher. The follow-on investigation would also examine alternate HEMT structures based on promising materials like InAs and InSb that could exceed InP and GaN performance, which has the additional potential of applications to both power and low noise.

The results indicate that for low bias settings the physical temperature of the active device region is within the detectable limit of 10 K at the lowest cryogenic temperature, 14 K, while at the highest cryogenic temperature, 51 K, the active region temperature is within 1 K. Furthermore, this study demonstrated a method to monitor the physical temperature of the active region of HEMT devices at cryogenic temperatures.

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