4800-bps High-Speed Data Error Statistics

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Analysis of GCF 4800-bps high-speed data error statistics information shows error bursts having a median length of 26 bits, though the range of burst lengths is very wide. Approximately 70% of the bits within a typical burst were error-free. An error block usually contains only one burst. Several burst characteristics are directly related to bit error rate. There is a small time correlation between errors experienced in opposite directions of transmission.

During October–December 1972, a series of high-speed data (HSD) tests were conducted between CTA 21 and DSSs 14, 42, 51, 61, and 71. These tests, which were run at 4800 bps on the Ground Communication Facility's (GCF) conventional HSD circuits, were designed to gather data on the distribution of the bit errors generated in the HSD System.

The configuration used for these tests is shown in Fig. 1. Identical 1200-bit high-speed data test blocks were generated by the DOI-5300-SP-A program operating in the Digital Instrumentation Subsystem (DIS). This continual data stream was forwarded through the block multiplexer. The encoder added the usual 33-bit error detection code. The encoded blocks were transmitted via a 203A List 2 data set at 4800 bps. Conventional back-to-back-data-set regeneration was routinely used at the NASA Communications (NASCOM) overseas switch centers (Madrid and Canberra) and at the central NASCOM switch at Goddard Space Flight Center (GSFC). Data were received by a 203A, decoded to detect errors, and forwarded to the receive section (sensor) of the DOI-5300-SP-A program.

The receive section compared the received block with a known good block on a bit-by-bit basis. The resulting error positions, by block number and bit location, were recorded on magnetic tape and reduced by an 1108 analysis program.

No attempt was made during the tests to specify particular circuits, nor to influence the circuit routing used by NASCOM. The goal was to obtain a realistic sample of the service normally supplied by the GCF.

Thirty-one separate tests were conducted, the total circuit time subtending 66 h. The individual tests were assigned to one of three analysis groups according to the measured bit error rate. The green group consists of individual tests having bit error rates better (less) than 1×10^{-5}. The amber group rates fall between 1×10^{-4} and 1×10^{-5}. The red group rates were all worse than 1×10^{-4}. These three groups, green, amber, and red, represent

excellent, normal, and poor GCF error performance. Normally, the GCF would not utilize red condition circuits (since they are out of limits); however, these tests were continued in order to provide an upper bound on error performance.

Most of the tests were run simultaneously in both directions (full-duplex). This permitted comparison of both sides of the circuit under identical conditions.

Table 1 shows various parameters by color group. A comparison of blocks received versus blocks transmitted shows an increasing block loss as line conditions worsen. This loss was composed of two parts: short line outages and sync recognition failures. The relative magnitude of the two parts could not be measured; only the total was observed. (Sync failure occurs when the 24-bit block synchronization code contains more than three errors. When this happens, the DIS comm buffer does not recognize the sync pattern and the faulty block is not inputted to the computer.)

Error blocks also naturally increase (percentage-wise) as line conditions worsen, and block thruput (a function of error and missed blocks) falls. The total thruput for these tests, 99.55%, is very close to the GCF's long-term average of 99.5%.

Median burst length was 26 bits for the total group, and was surprisingly close to this value for both the green and amber groups. In common with wideband data experiences, a relatively few long bursts cause the average burst length (59 bits) to substantially exceed the median (26 bits) case.

Within a burst, there are roughly 2 error-free bits for each in error. This ratio, in common with other burst parameters, is quite dependent on how a burst is defined. In this analysis, a burst was considered to be a string of good and bad bits which always starts and stops with an error and which was separated from an adjacent burst by 40 or more good bits.

A review of the raw data shows three kinds of bursts:

(1) A single-hit type of error, which produced only a few errors separated by many good bits. The data set scrambler establishes the minimum length of this type of burst, which occurs mostly during good line conditions.

(2) A truly random burst condition, wherein 1's were translated to 0's and 0's to 1's with about equal probability. During such bursts, the number of good bits and error bits were about equal.

(3) A carrier-failure condition due either to a long, heavy noise condition or an actual circuit failure. During this condition, the data set clamped its output to the 1 state until more normal conditions prevailed. This all-1's output causes all data 0's to be changed to 1's.

The bit translations entry in Table 1 shows an increasingly greater preference for 0-to-1 translations as line conditions worsen. This appears to be due solely to the third type of burst outlined above.

Block error rates were determined for the 1200-bit blocks now being used in the GCF and also for 2400- and 4800-bit lengths. During good circuit conditions, the block error rate increases linearly with block length, indicating that the bursts are much more than 4800 bits apart. This proportionality does not quite hold during average (amber) conditions. During red conditions, a significant number of the longer blocks apparently contain more than one burst.

As mentioned earlier, most of the tests were conducted simultaneously in both directions. Since the test start times were accurately recorded to the second, it was often possible to determine how many block errors occurred simultaneously in both directions. The results, shown in Table 2, imply that perhaps one error block in ten is mated with an error block in the opposite direction. Most such dual errors could be expected to be caused by the same error-generating source.

Using a model developed by D.C. Card, the circuit and its delivered bits can be considered to always be in one of two states—burst or error-free. During the error-free state, all bits are delivered without errors. During the burst state, some bits are delivered in error and some are error-free, as noted earlier. Each bit may thus be classified as one of three types:

0 An error-free bit occurring during a non-burst state. (This is the "normal" state which we would like all bits to occupy.)

1 An *error* bit occurring within a burst.

2 An *error-free* bit occurring within a burst.

A burst always starts with an error and ends with an error. This permits a firm determination of the beginning and end of each burst and eliminates the spectre of bursts which contain no errors.

Using the above tags, a 0-to-0 transition occurs between 2 bits, both of which are error-free and outside a burst. A 0-to-1 transition marks the beginning of a burst and is

ultimately followed by a 1-to-0 transition at the end of the burst. A 1-to-2 transition would indicate an error bit followed by a good bit, both within a burst. (0-to-2 and 2-to-0 transitions are not permissible since category 2 bits can occur only within a burst, while 0 bits occur only outside a burst.)

From the transition data, it was possible to construct the Card transition probability matrices shown in Table 3. These matrices depict, for each of the groups and the total, the probability of occurrence of each of the transitions. The bit types across the top represent the state of bit n and the types along the left show the state of the $n + 1$ bit. For instance, in the green group, the probability of a 1-to-2 transition is 0.592, whereas the probability of a 1-to-0 transition is 0.088. As discussed earlier, 0-2 and 2-0 transitions are not permitted and are given a zero probability. The matrices readily show many of the characteristics previously pointed out: the burst nature of the errors, good/bad ratio in a burst, etc.

Figure 2 presents information on the distance between bit errors. In the green group, for instance, there were 305 cases where adjacent bits (distance = 1) were in error, 215 cases where there was one good bit between the error bits (distance = 2), etc.

If the errors were random, the slope of the curve would have been $1/2^n$. In all cases, this slope holds through a distance of 6 to 7 bits. Beyond this point, the presence of many good bits mixed with a few error bits causes the slope to decrease.

The peaks in Fig. 2 at a distance of 5 and 18 were caused by the data set scrambler, a shift register device which makes the transmission spectrum essentially independent of the digital bit sequences. Unfortunately, during very short circuit noise pulses (hits), the scrambler acts as a $\times 3$ error multiplier, inserting extra errors at distances of 5 and 18.

Table 1. Error parameters

Parameter	Group			Total
	Green	Amber	Red	
Test duration, min	1095.2	362.7	2486.6	3944.5
Number of tests	9	19	3	31
Bit error rate:				
Average	3.04×10^{-6}	3.08×10^{-5}	2.52×10^{-4}	4.33×10^{-5}
Median test	2.3×10^{-6}	2.48×10^{-5}	2.54×10^{-4}	1.63×10^{-5}
Number of bursts	84	1167	1462	2713
Bursts per hour	4.6	35.3	193.0	41.3
Blocks transmitted:				
Inbound	181279	275062	85587	541928
Outbound	81374	326682	0	408056
Total	262653	601744	85587	949984
Blocks not received	9	1066	1465	2540
Blocks received in error	78	1184	495	1757
Block thruput, %	99.96	99.63	97.71	99.55
Burst length, bits:				
Shortest	0	1	1	0
Longest	417	869	1071	1
Average	38.9	50.2	71.6	59.1
Median	24	26	54	26
Bits within bursts, %:				
Good bits	70.8	69.6	68.9	69.3
Error bits	29.2	30.4	31.1	30.7
Error bit translations, bits:				
1's translated to 0's	345	7558	8318	16221
0's translated to 1's	527	13298	16180	30005
Block error rate:				
1200 bit blocks	0.00030	0.0020	0.0058	0.00185
2400 bit blocks[a]	0.00058	0.0035	0.0084	0.00315
4800 bit blocks[a]	0.00108	0.0067	0.012	0.00564

[a]Derived from tests conducted with 1200 test blocks.

Table 2. Simultaneous block errors in opposite directions

Tests	Block errors inbound	Block errors outbound	Simultaneous block errors
3,4	37	100	3
5,6	11	22	0
31,32	0	11	0
33,34	176	9	0
1,2	0	24	0
7,8	5	24	2
9,10	1	37	0
35,36	2	19	0
37,38	29	53	9
11,12	221	214	14
22,23	96	112	23
	578	625	51

Table 3. Card transition probability matrices

Green

	0	1	2
0	$1 - (2.73 \times 10^{-7})$	0.088	0
1	2.73×10^{-7}	0.320	0.244
2	0	0.592	0.756

Amber

	0	1	2
0	$1 - (2.02 \times 10^{-6})$	0.065	0
1	2.02×10^{-6}	0.341	0.259
2	0	0.594	0.741

Red

	0	1	2
0	$1 - (1.14 \times 10^{-5})$	0.045	0
1	1.14×10^{-5}	0.355	0.270
2	0	0.600	0.730

Total

	0	1	2
0	$1 - (2.40 \times 10^{-6})$	0.055	0
1	2.40×10^{-6}	0.348	0.265
2	0	0.597	0.735

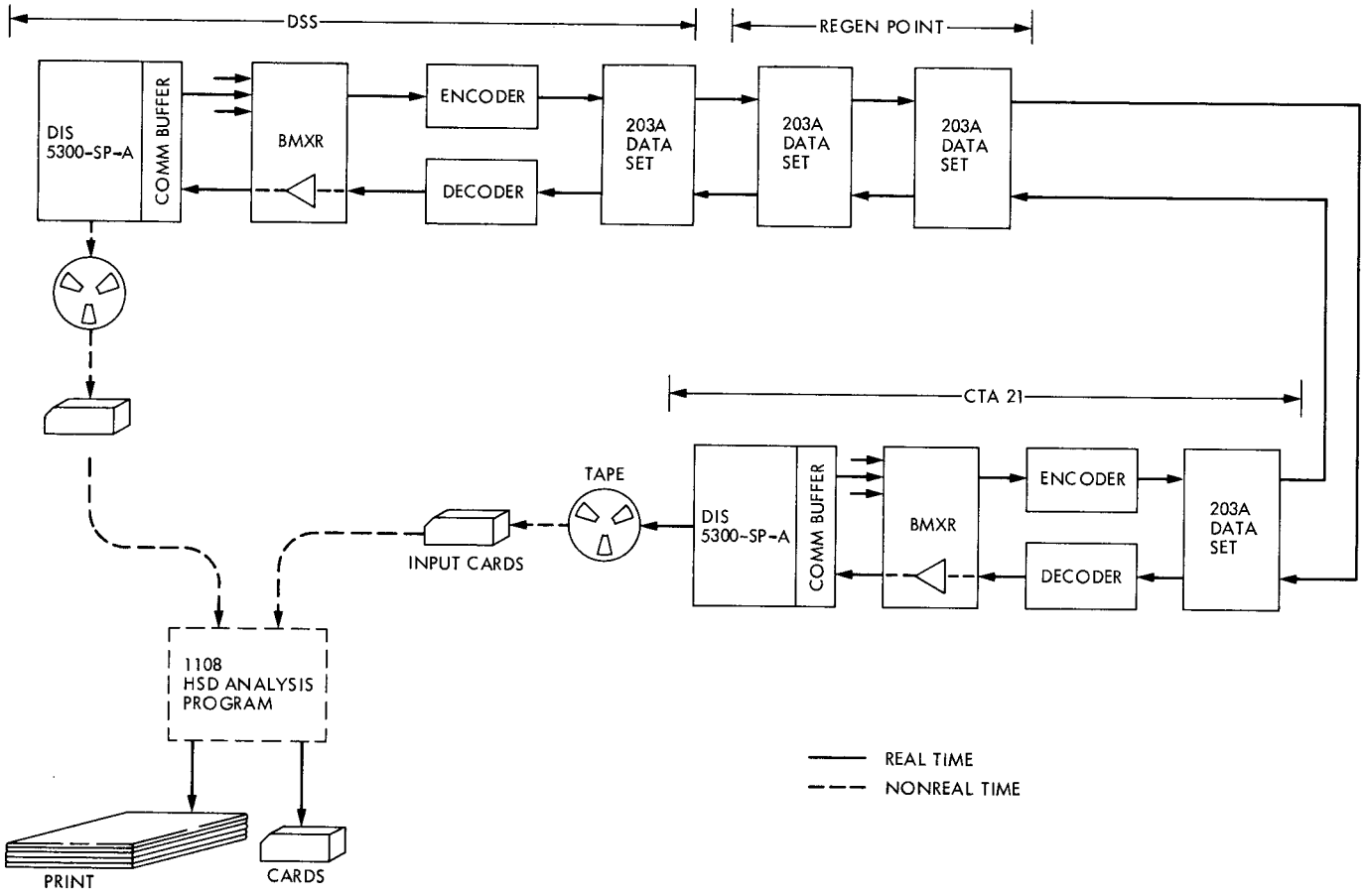

Fig. 1. 4800-bps high-speed data test configuration

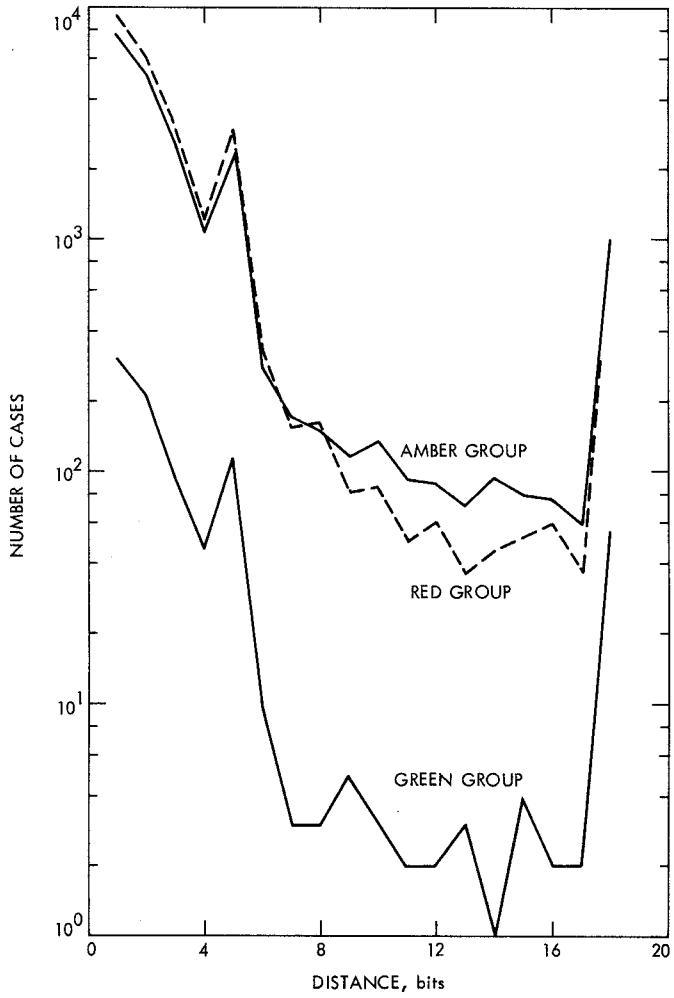

Fig. 2. Distance between bit errors