Hybrid Integrated Circuit Development

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This report describes the development of a single hybrid circuit to replace the control portion of a 15-line computer interface consisting of 25 discrete integrated circuits. The primary requirements of this hybrid development are the standardization of a logical design to implement the requirements of the Deep Space Network standard interface requirement and the reduction of system downtime due to complex troubleshooting.

I. Introduction

The control portion (handshaker) of the standard DSN 15-line interface (Ref. 1) performs all the information transfer protocol and generally relates necessary communication between computer and device before data can be successfully transferred. A handshaker circuit that satisfies these computer and device interface requirements has been designed (Fig. 1) and will function between any desired combination computer and peripheral device. This circuit is both device and computer independent and operates in the half duplex mode using a fully interlocked request and acknowledge control transfer (Ref. 2).

The handshaker circuit contains 25 transistor-transistor logic (TTL) integrated circuit (IC) packages and 25 wirewrap IC sockets (Fig. 2) all mounted on a 120 mm × 115 mm circuit board. This method requires 750 connections, 50 of which are for B+ and ground. Because this circuit is designed such that it feeds signals from one stage to another, dependent on conditions within its feedback and/or external inputs, it is extremely difficult to troubleshoot (i.e., even if every IC was replaced with fully tested units, it would take a minimum of 15 min, and the fault could still be in the sockets or in one of the 750 connections).

A requirement to reduce Deep Space Station downtime resulted in the investigation of hybrid circuits as a means to replace multiple discrete integrated circuits with a single package and to provide a standardization of the logic design.

II. Implementation

The initial hybrid development utilizes the same TTL circuit design as the discrete design. The TTL circuit chips are bonded to a package that is 36 mm × 36 mm, with 24 pins. The TTL interconnect circuitry within the hybrid is similar to a standard printed circuit (PC) board in that the circuit traces are etched. Due to its small size, circuit crossovers can be made with short gold wire jumpers bonded to the traces. This method, because it

eliminates the need for multilayer boards to solve circuit crossovers, greatly reduces design time and cost over the conventional PC board. The completed hybrid circuit package is shown in Fig. 3, and a single chip has been enlarged in Fig. 4 to show the wire bonding.

III. Conclusion

The hybrid handshaker circuit has been successfully evaluated with the coherent reference generator and the PDP-11 minicomputer using the 15-line interface. The hybrid circuit has reduced the system parts inventory by 10 to 1, based on stocking one each of every type of IC. The system assembly has been reduced from 750 connections to 48, thereby improving both reliability and enhancing quality control. By reducing parts by 24 and interconnections by over 700, the system testability has been improved as well as downtime due to testing and repair. Because the TTL chips can be removed with heat, the hybrid can be returned to the factory for repair at a fraction of replacement cost. The completed prototype hybrid handshaker will undergo further testing outside of the development group.

The results of these tests will be used to evaluate this approach and determine if further design effort is required.

References

1. Fry, W. C., *Deep Space Network Standard Interface,* Spec. ES50834A, June 4, 1973 (JPL internal document).
2. Foster, C. F., *Complete Logical Operation and Test Procedure of Handshaker Circuit,* Spec. TP510942A, in preparation (JPL internal document).

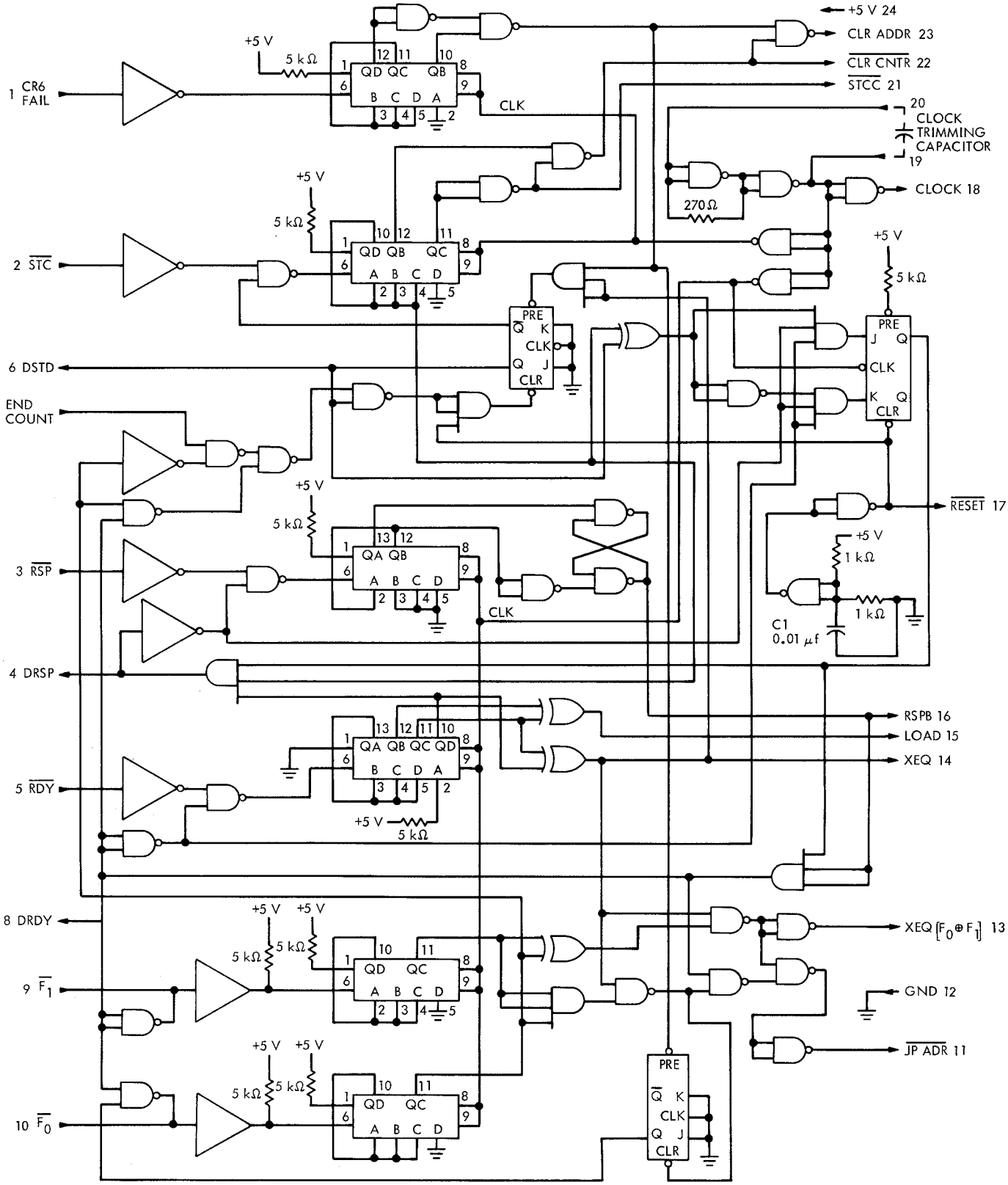

Fig. 1. CRG computer interface handshaker logic diagram

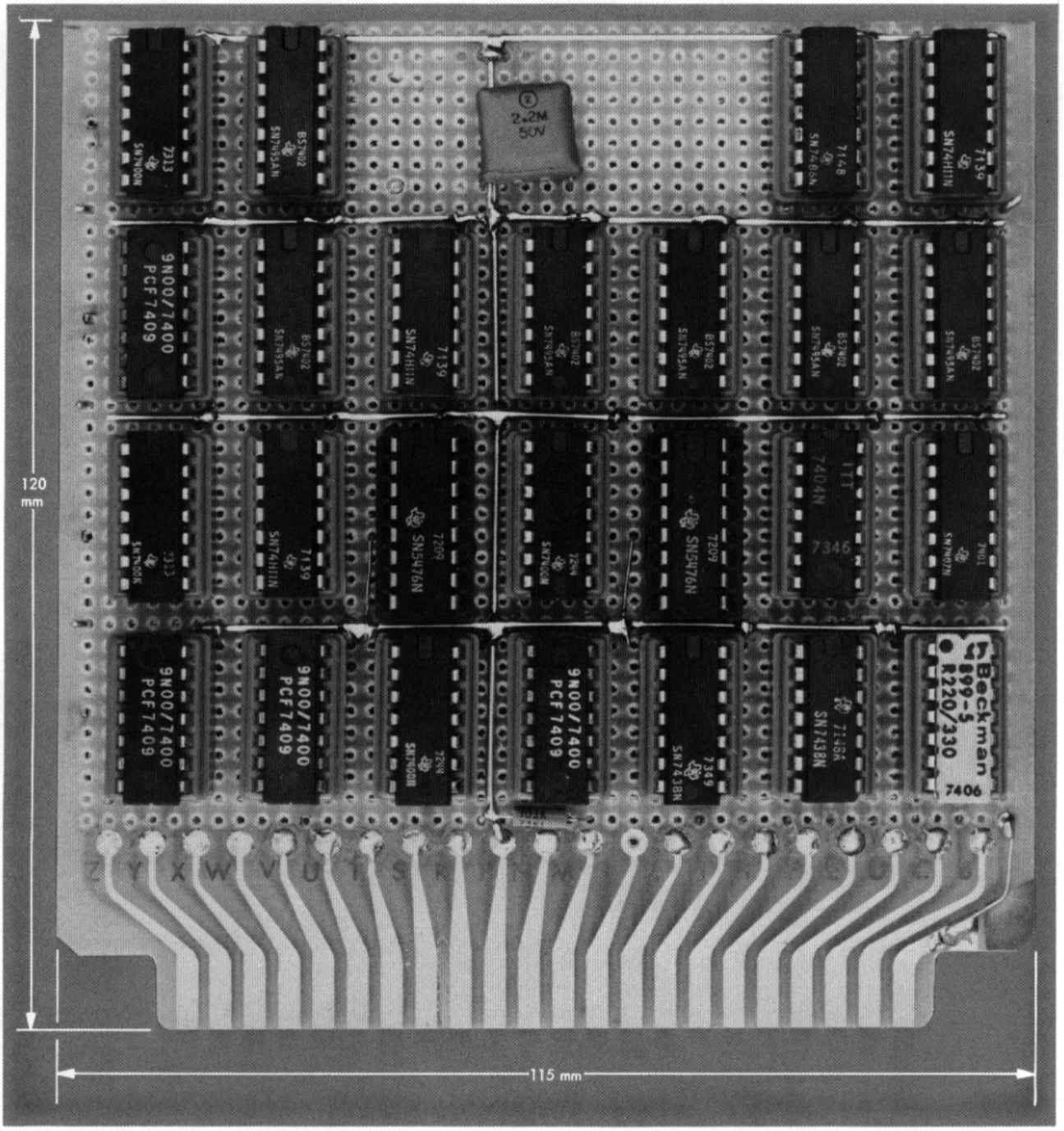

Fig. 2. Computer interface handshaker logic (discrete)

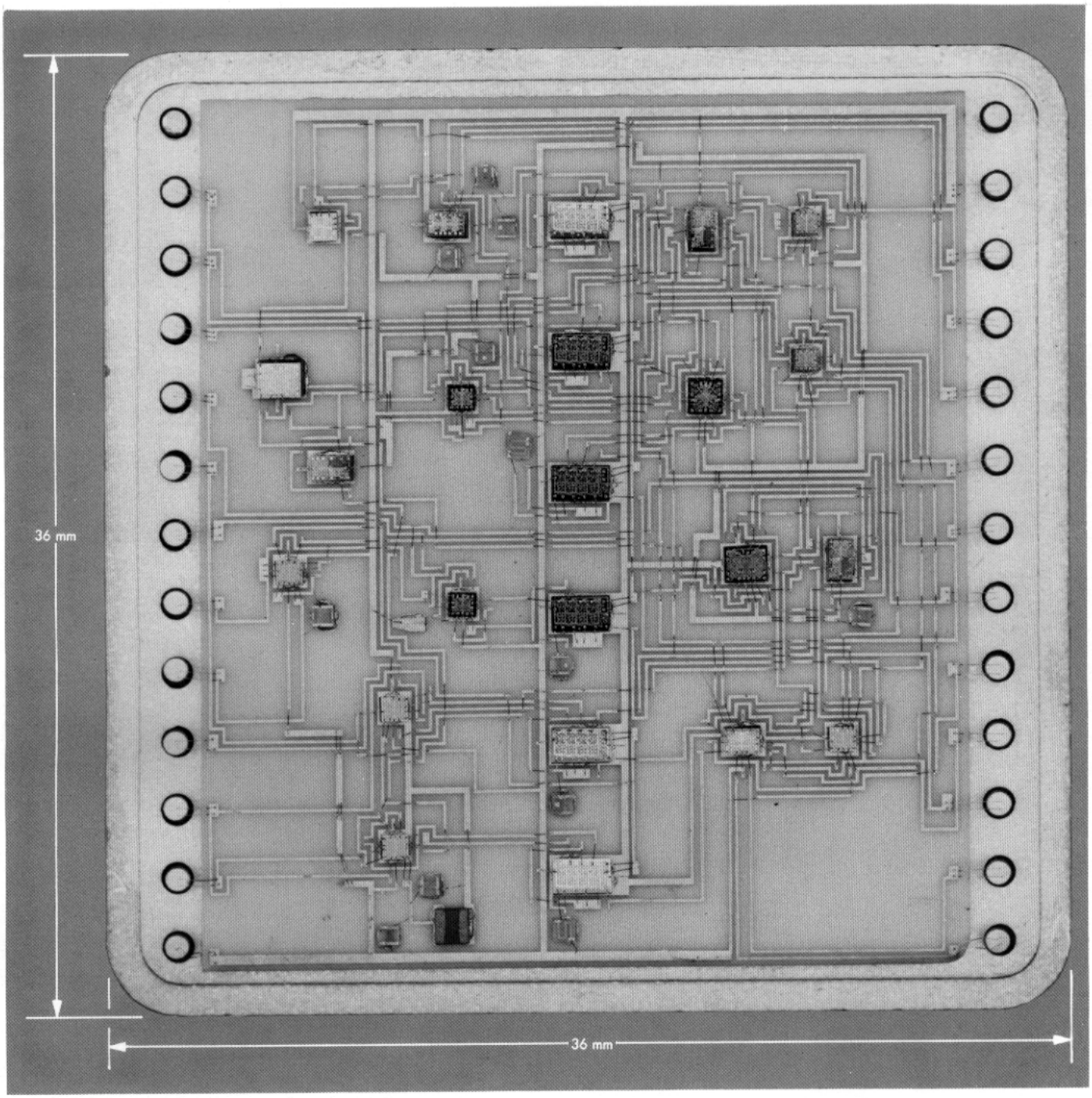

Fig. 3. CRG computer interface handshaker logic (hybrid)

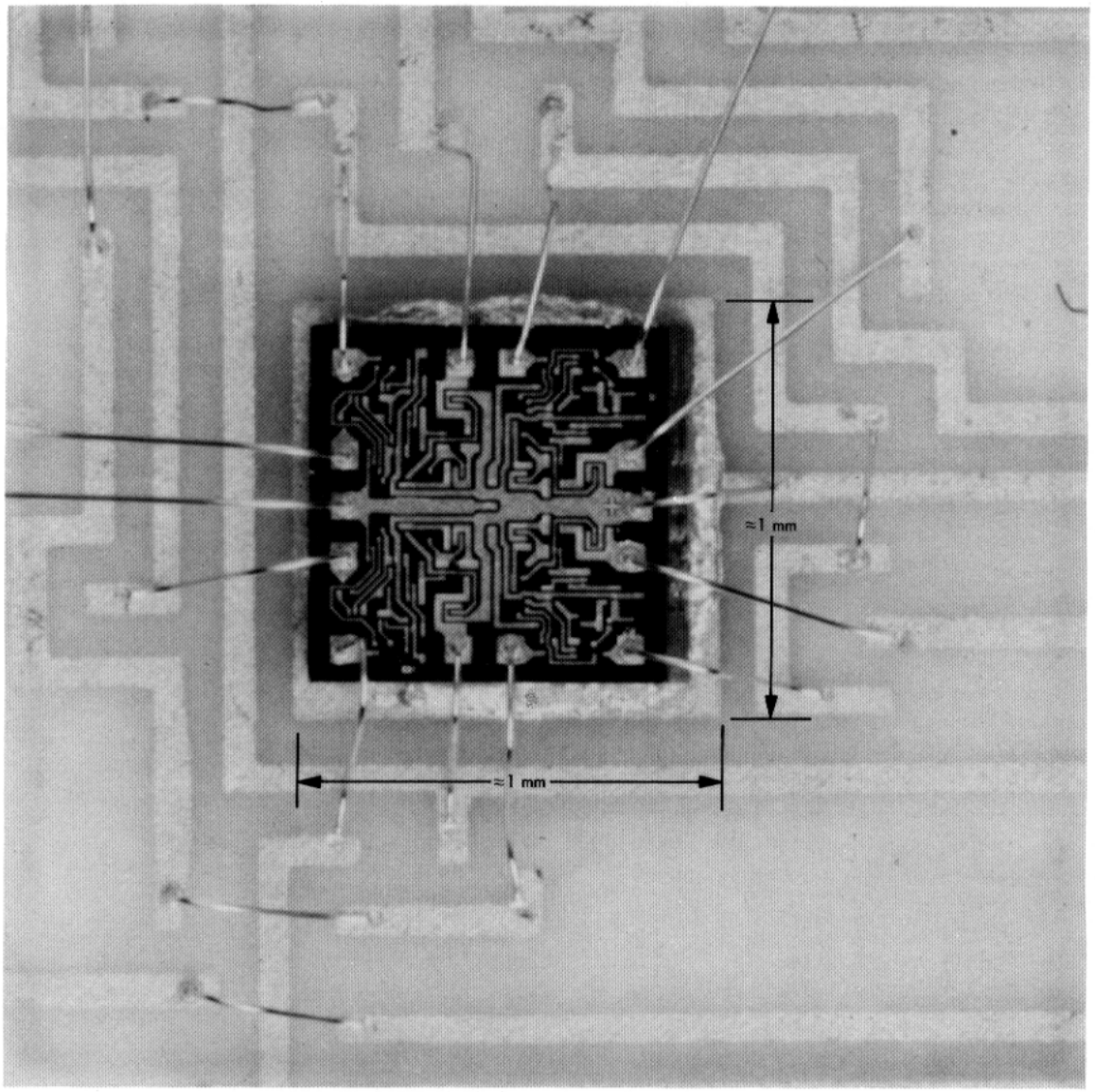

Fig. 4. Hybrid circuit chip mount