Simulation Time Switch Assembly: A New Conjoint Station Time Switching Capability

M. J. Galitzen
DSN Data Systems Development Section

The DSN conjoint stations located in Spain and Australia have been operating with a tracking and telemetry simulation restriction. The Frequency and Timing Subsystem is able to provide either a real-time output or a simulation time output to the 64-m and 26-m station wings of the conjoint stations at any time, but not both simultaneously. During various tracking schedules, it is useful to be able to conduct a simulation run or training exercise with the non-tracking wing. This station utilization is restricted with the present system. The solution to this problem is to provide a separate real-time and simulation time interface to each of the two stations and to the three Telemetry and Command Processor strings. The simulation time switch assembly will provide the switching capability to drive independently the 64-m, 26-m, and processor interfaces with binary coded decimal time, 1 pulse per second, 100 pulse per second, and 1000 pulse per second Greenwich Mean Time (GMT) real time or simulation/tape time sources.

I. Introduction

The 64-m/26-m conjoint stations have one Frequency and Timing Subsystem (FTS) digital clock system which provides Greenwich Mean Time (GMT) real time, and clock pulses to clock the dual control room telemetry systems. The station configuration required that the two stations and the Telemetry and Command Processors (TCPs) be driven together from the single FTS for a simulation or training exercise, or for a spacecraft track. The subsystem to processor interface is shown in Fig. 1. Figure 1 shows that the present subsystem can be switched to either the real-time mode or the simulation mode. The real-time input to the subsystem is amplified and distributed to the TCP 1, 2, and 3 equipment. The simulation input to the real-time switch is derived from a serial to parallel time code translator (TCT) which is a part of the Pre-Post Recording (PPR) Subsystem. The input to the time code translator is a 36-bit serial NASA time code. This code is switched at the Pre-Post Recording Subsystem and is used to drive the time code translator. The inputs to the translator are derived from either the Simulation Conversion Assembly (SCA) time code generator (TCG) or the 64-m/26-m tape recorder time playback channels. The 30-bit binary coded decimal (BCD) time codes and a 1-pulse-per-second (pps) signal are provided by the time code translator for the FTS simulation channel. The binary coded decimal signals are distributed to all complex equipment when the FTS is in the simulation switch mode. The time code translator 1 pps is used to reset the subsystem timing pulse outputs before they are distributed. The subsystem outputs are reset only when in the simulation mode.

The TCP 2 presently has a special time switch assembly. This assembly switches the 30-bit binary coded decimal, 1-pps and a 1-kpps signal from either the time code translator or the FTS. The TCP 2 time switch assembly reamplifies and distributes the 30 binary coded decimal real time or simulation binary coded decimal and the 1-pps, 1-kpps pulse inputs to the TCP 2 computers. The TCP 1 and 3 computers can only be used for simulation if the FTS is in the simulation position. A summary of the configuration and constraints of this system is given in Fig. 2. Line A shows the operational modes when the FTS GMT switch is on GMT. Line B shows the lack of flexibility when the subsystem GMT switch is in the simulation position.

II. New Configuration

The simulation time switch assembly (STSA) was built to replace the time switch assembly and to expand the FTS GMT time distribution. Figure 3 is a functional diagram of the FTS, Pre-Post Recording Subsystem, simulation time switch assembly, and station configuration. The simulation time switch assembly receives inputs from the FTS and the Pre-Post Recording Subsystem time code translator. The FTS input consists of the 30-bit GMT binary coded decimal time bits, 1 pps and 1 kpps. The assembly time code translator also provides the binary coded decimal and pulse outputs for a tape playback mode. The assembly uses the simulation and tape 1 pps and 1 kpps to generate internally a 100-pps signal for the simulation and tape channels. The assembly can then independently switch the real-time and nonreal-time input pulses and binary coded decimal GMT to the 64-m station FTS distribution system, the 26-m station FTS distribution system, and each of the three Telemetry and Command Processors. This capability then allows the 64-m station and the 26-m station to operate independently. The basic capability of the new system can be summarized in the following two statements:

(1) The simulation time switch assembly provides real-time and simulation time buses which allow each telemetry string and station to connect to either bus independently.

(2) The simulation time switch assembly also provides sufficient distribution amplifiers to drive multiple-telemetry processing strings and station loads which are to be switched on to the assembly buses.

A. Tape Time Mode

The real-time/simulation inputs to the simulation time switch assembly originate at the FTS GMT/SIM switch and the assembly time code translator. The GMT/SIM position of the FTS is driven by 30 binary coded decimal bits from the time code translator mounted within the simulation time switch assembly. The input to the time code translator would normally be from 64-m or 26-m station tape recorder time channels. This input provides a means of switching tape playback time on to the FTS simulation time switch assembly real-time bus. In this tape playback mode, the FTS real-time bus then becomes a nonreal-time (tape time) bus. Control switches connected to the assembly will be used to activate the assembly time code translator tape pulse outputs in conjunction with the FTS simulation switch.

B. Dual Time Operation

The Pre-Post Recording Subsystem time code translator would be used to provide the simulation time bus with simulation time. By using the frequency and timing/simulation bus and the simulation time switch assembly simulation bus, the stations can conduct a tape playback verification and a simulation or training exercise simultaneously. The control of both of these buses is from a central control panel mounted in the Station Monitor and Control (SMC) Subsystem. This panel provides the switching point for the simulation time switch assembly. The assembly has an independent single status monitor output. This output will provide digital information to the Monitor Subsystem. This information will be input to the station monitor computers which would record or display the assembly switching status.

III. Simulation Time Switch Assembly System Design

The assembly requires a standard equipment rack. Mounted within this rack are pulse amplifiers, amplifier power supplies, a time code translator, a control and status assembly, coaxial switch assembly, a binary coded decimal relay assembly, and a signal distribution assembly.

The block diagram of the simulation time switch assembly binary coded decimal switching is shown in Fig. 4. The 30 binary coded decimal bits from the FTS simulation bus are distributed to five 51-pole relays. One relay is provided for each of the five outputs. These channels, as stated before, are for the 64-m and 26-m station Frequency and Timing Subsystems, and for the three Telemetry and Command Processors.

A. Failure Isolation

The FTS binary coded decimal signals are amplified and sent to the FTS distribution system. This series amplifier protects the simulation time switch assembly FTS/GMT bus from 64-m station binary coded decimal line failures or feedback. The signals to the 26-m station FTS distribution are re-amplified and isolated within the 26-m station FTS distribution system. The Telemetry and Command Processor outputs are also amplified, isolated, and distributed to the three processors through their respective relays. Each of the five relays has an external independent control and monitor interface. This is represented by the circled capital R on Fig. 4.

B. Timing Pulse Distribution and Switching

The distribution and generation system for the 1 pps, 100 pps, and 1 kpps is shown in Fig. 5. The Frequency and Timing Subsystem provides a 1-pps, 100-pps, and 1-kpps timing pulse input. These signals are amplified, isolated, and distributed to five coaxial relays. The time code translator from simulation and the time code translator within the simulation time switch assembly each provide a 1-pps and a 1-kpps input. These signals are used to generate a synchronized 100 pps for the simulation and tape channels. The simulation tape 1 pps, 100 pps and 1 kpps are switched within five sets of three coaxial relays. The relays have three inputs, one each for FTS, simulation, and tape pulses. The output of the coaxial relays is controlled by the external monitor and control panel within the Station Monitor and Control Subsystem. Status lines are sensed and are part of the remote monitor interface. This interface is combined with the binary coded decimal status lines to form an interface which can be sensed by the station monitor computers.

IV. Conclusions

The simulation time switch assembly will support the Viking multiprobe mission. This system will allow tracking, training, and simulation in a dual station simultaneously. This will increase the utilization of the dual station configuration. In future years the tape playback channel will be used for tape verification as well as for simulation from prepared test tapes.

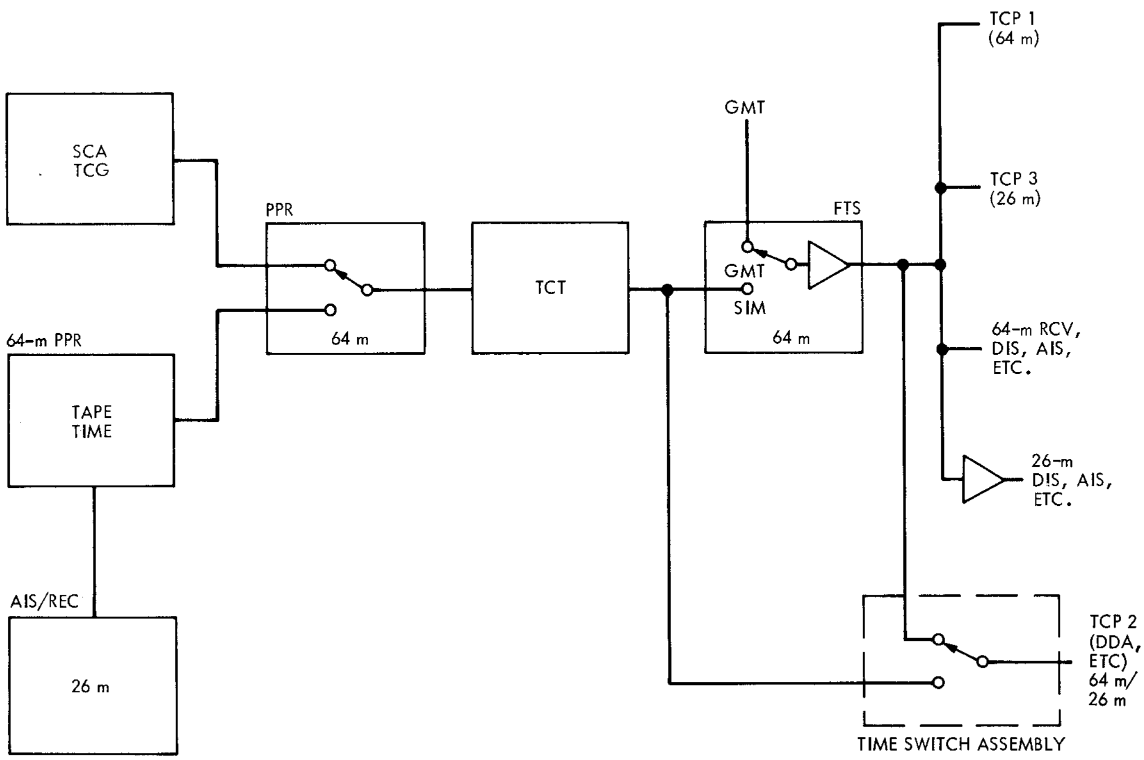

Fig. 1. Present configuration for DSSs 43/42, 63/61

64 m: $\underbrace{\text{TLM STRING 1, TLM STRING 2}}$

26 m: $\underbrace{\text{TLM STRING 2, TLM STRING 3}}$

LINE	TLM STRING 1	TLM STRING 2	TLM STRING 3	STATION EQUIPMENT	
				64 m	26 m
A	GMT	GMT OR SIM	GMT	GMT	GMT
B	SIM	SIM	SIM	SIM	SIM

Fig. 2. Present capabilities of dual station time switching

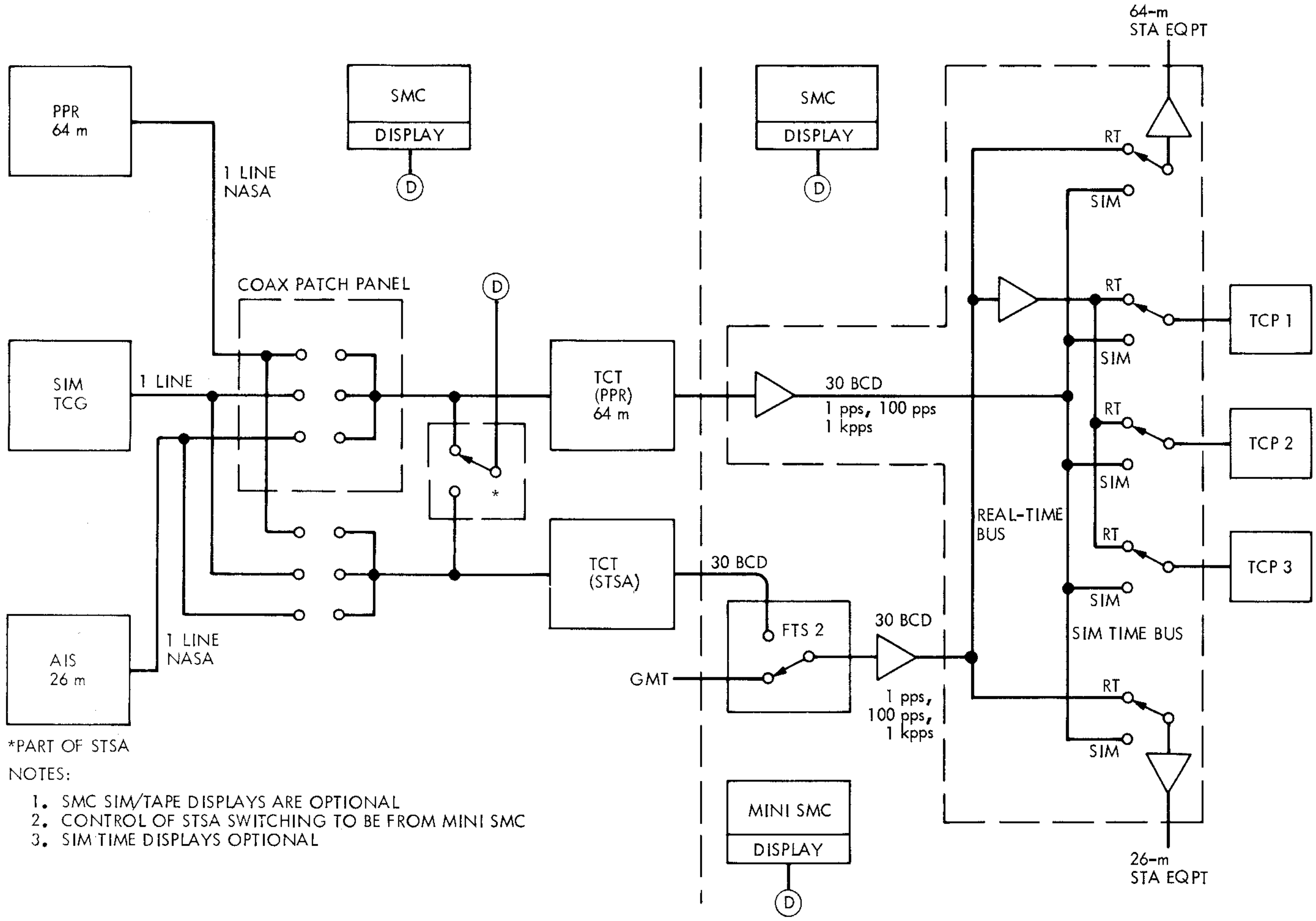

Fig. 3. Simulation time switch assembly configuration

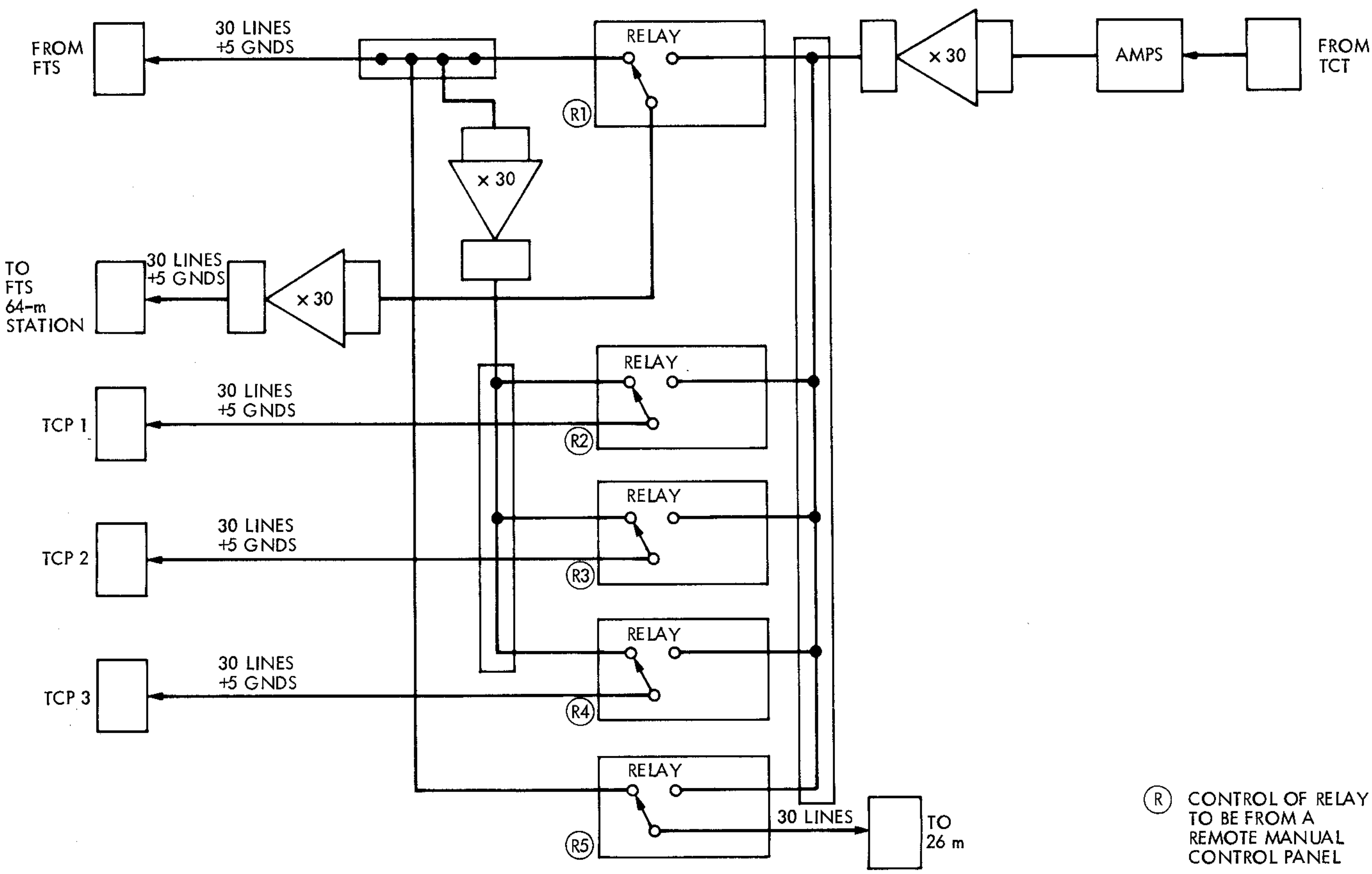

Fig. 4. Block diagram of simulation time switch assembly BCD switching

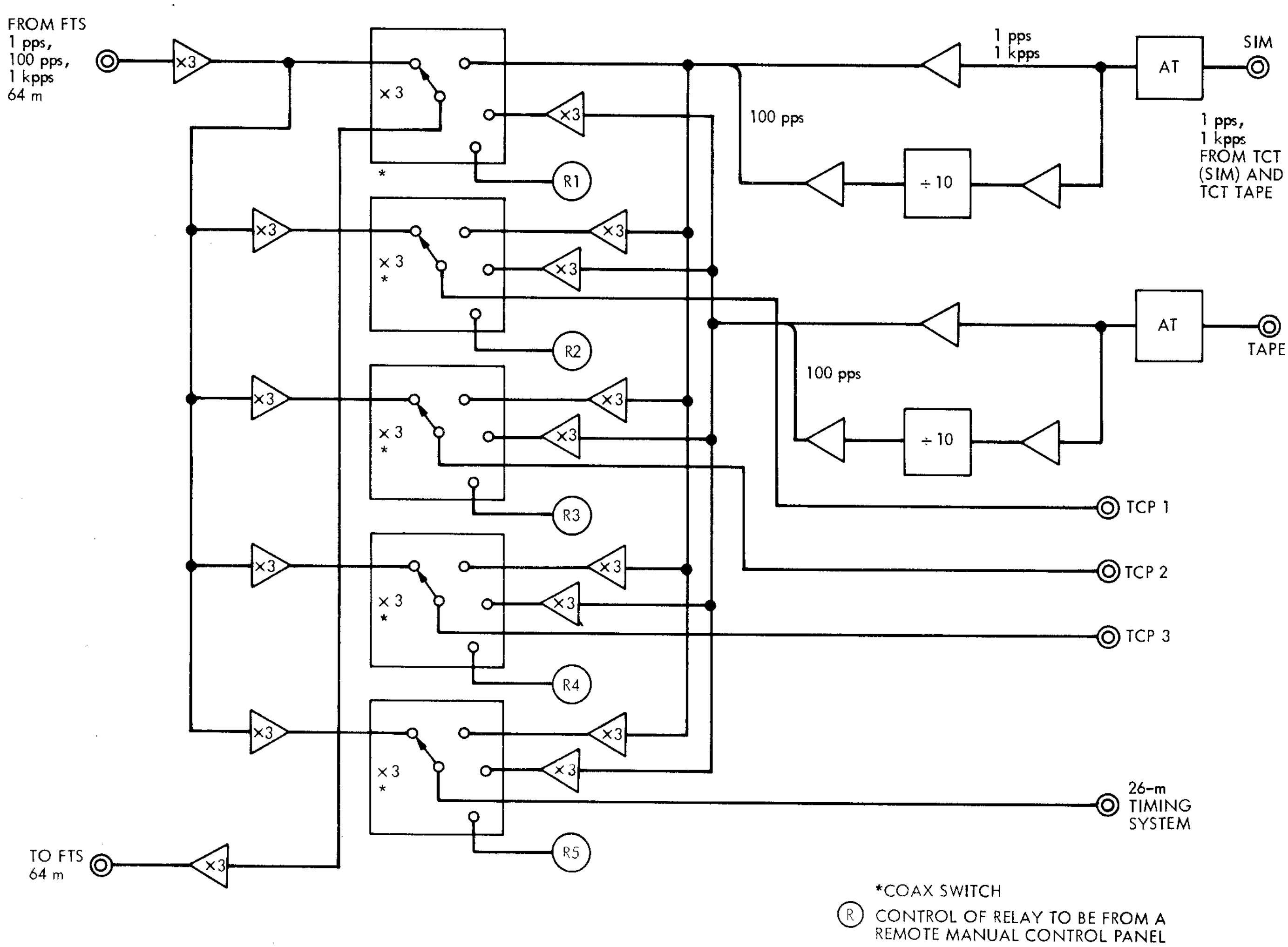

Fig. 5. Block diagram of simulation time switch assembly for 1 pps, 100 pps, and 1 kpps