DSN Standard Interface Adapter and Buffer Assembly Used in the Mark III Data System

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This article describes the DSN Standard Interface Adapter and Buffer Assembly (referred to as the "900/SIA") used to effect interface compatibility between the Xerox Data Systems 920 computer (XDS 920) and the Mark III Data System (MDS) processors. It sets forth the requirements based on the differences between the two systems. Described are the operational characteristics and general design strategy as well as certain efficient implementation techniques used. From a software standpoint, the transfer protocol is discussed to a level of detail sufficient for its operation.

I. Mark III Data System Requirements

The Mark III Data System (MDS) retains the Digital Instrumentation Subsystem (DIS) 920, which is then required to communicate with the MDS Modular Computer Systems (MODCOMP) processors through the Star Switch Controllers (SSCs). Because of the gross incompatibilities between the 920 and the DSN Standard Interface, an interface adapter and buffer is required. The incompatibilities exist in the areas of:

(1) Speed of operation.

(2) Data format.

(3) Interface protocol.

(4) Electrical signals.

The 920 cycle time is 8 μs, requiring an average of 5 to 6 cycle times per word transfer (i.e., 40 to 48 μs), while the Standard Interface transfer rate may be as high as 500 kHz (i.e., 2 μs per word transfer), depending on cable length. The 920-word format is 24 bits per word, while the word format of the MDS processors is 16 bits per word and the Standard Interface word format is 8 bits per word.

The 920 I/O register mode interface control is based on outbound requests in the form of EOM (energize output medium) code words and inbound single line "interrupt" responses.

The 920 then operates on a pulse technology where the event of a pulse must be stored in the adapter as must

the sequence of succession of events. The Standard Interface consists of an outbound "request to transmit" signal, an inbound "response," i.e., ready to receive signal, and an outbound "data available" or "data ready" signal. The 920 control signals are short-duration pulses (8 V), one for the beginning and one for the end of an operation, while the Standard Interface signals are "levels" (5 V) which prevail during an operation, the beginning of the level signaling the beginning of the operation and the end of the level the end of the operation. Control signal memories for the Standard Interface need then not be furnished in the interface adapter.

The 920 and the Standard Interface parameters of concern to the adapter are described in the following sections.

II. Standard Interface, General Description

The MDS consists of a large number of processors and peripherals, many from different manufacturers and with gross interface incompatibilities. Each device has been made to conform to the Standard Interface. The Standard Interface uses an 8-bit parallel (byte) transfer and the transfer control signals are simple. They consist of a unidirectional "request to transmit" signal, one in each direction, a "response" and a "ready" signal, both bidirectional. Electrically these signals are 5-V signal levels, where +5 V is the idle level and GND is the active level.

III. 900/SIA Adapter Buffer Requirements

Systems analysis has concluded that transmission between the DIS 920 and an MDS processor over a single register would create too large an overhead time for the MDS processor, which would then be inefficiently used. A data memory or buffer is therefore included in the adapter. The capacity of this buffer is equal to a high speed data block, or approximately 1200 bits. The buffer, which is a rate and format buffer, can be functionally visualized as a shift-register with the first data in being the first data out.

Systems analysis considerations further suggest the use of two identical buffers, one in each direction. If an MDS processor were to request to transmit to the adapter buffer while the buffer was being filled by the 920, either the partial block from the 920 would have to be discarded or the processor would have to reconfigure its I/O and be faced with an additional overhead. The amount of hardware required for switching of data and control, for a single buffer to be able to operate in either direction, is considerably larger than an additional buffer without such switching.

The operation of such a buffer is as follows: When transmitting from the DIS 920 to the MDS processor, data are metered out from the 920, through its register I/O POT (parallel output) connections, to the adapter buffer until a full data block has been assembled in the buffer. At that instant, the adapter requests to transmit this data block to the MDS processor at a high rate through the SSC. When the buffer has been fully unloaded it is again available to be loaded and the sequence is repeated.

When transmitting from an MDS processor to the 920, the sequence is essentially reversed. The processor requests to transmit a complete data block at high speed to the adapter buffer.

IV. 900/SIA/Design Parameters, Summary

The design parameters for the 920/SIA are summarized as follows (for reference see Fig. 1):

(1) Two identical channels are provided, one each on directly interchangeable subassemblies.

(2) For each channel, four distinctly identifiable interfaces exist.

(3) Two of the four interfaces, to and from the SSC through the SIA, share one port.

(4) One set of PIN/POT connections is shared between the two channels.

(5) The POT connections are common to both channels.

(6) The PIN connections are collector OR-controlled between the channels.

(7) The adapter operates at maximum speed commensurate with the access times of the buffers.

(8) Because of the timing specifications between Input Data, Address and Load Pulse for the buffers, each 920 EOM involved in buffer control is divided into phases.

(9) The interrupts to the 920 are time buffered to comply with the 920 8-μs requirement.

A. Word Formats

The 920 word format is 24 parallel bits while the MDS processor word format is 16 bits. The Standard Interface

to which the MDS processors conform operates on 8-bit bytes. The assembly and disassembly of half a processor word into a third of the 920 word would be both cumbersome and time consuming, especially in handling parity and check sum. Systems analysis has concluded, based on a tradeoff between idle core capacity and increased speed of operation, to limit the 920 word length to 16 bits, commensurate with the MDS processor word length and with two standard interface 8-bit bytes.

B. Buffer Control

For each channel there are two buffers: Buffer A from the 920 to the SIA and Buffer B from the SIA to the 920. Because of the required word assembly and disassembly between the 920 16-bit word and the SIA 8-bit byte, each buffer is divided into two branches of 8 bits each: A_1, A_2, B_1, B_2. For reference, see Fig. 2. This configuration has been used during checkout and test.

C. Block Length Control

The block length control is implemented by using one additional buffer track for flags or markers. A single flag bit on a unique track indicates the end of a data block. At the time the end flag is inserted the content is available to be read out. End of readout is signaled by the end-of-block flag appearing at the output. The buffers are implemented using a Random Access Memory (RAM), and the beginning of a data block is synonymous with reset of the address register. The end of a data block is a single flag bit inserted at the address of the last byte. For readout, the address register is reset and sequenced in the same manner as during loading, until the flag bit is detected signaling unload complete.

D. Buffer Control Summary

Both the A and the B buffers are configured as 16-bit-wide buffers. Buffer A is 160 words long, Buffer B 80 words. Buffer A loads two identical 16-bit words with data change for every other address change. The address changes for each load pulse. The alternating control is applied to the OE (Output Enable). The end-of-block flag is loaded into the control buffer at the address of the last byte plus one. Buffer A unload is accomplished by resetting its address register and augmenting it by the data strobe pulse until the end-of-block flag is encountered at the control buffer output. Buffer A_1 and A_2 outputs are paralleled, and their OEs are alternately asserted. Since the buffer output circuit is a tristate circuit, the parallel connection and alternating OEs will produce the desired 8-bit-byte data stream to the SIA, with no auxiliary data switching logic required.

Buffer B operates in a similar manner. During the load operation the inbound 8-bit-byte data are connected in parallel to the input of both branches, B_1 and B_2. The address changes for every other load pulse. During the unload operation, both branches B_1 and B_2 are unloaded simultaneously, thus forming the assembled 16-bit words.

V. Control of the Four Interfaces

There are four different major interfaces:

(1) The 920 to Adapter Interface, Buffer A Load.

(2) The Adapter to SIA Interface, Buffer A Unload.

(3) The SIA to Adapter Interface, Buffer B Load.

(4) The Adapter to 920 Interface, Buffer B Unload.

For reference see Fig. 3.

The terminology and timing control in general are the same for all four interfaces listed above. For reasons discussed elsewhere, the interface strategy as well as terminology is influenced by the MDS processor interface rather than by the 920 and is as follows.

A computer (920) or device (adapter) that has data to be transmitted initiates the operation by asserting an outbound request-to-transmit line. To this request the recipient responds by asserting an outbound response line (RSP) indicating a ready-to-receive condition. As the sender receives an inbound RSP it asserts an outbound RDY line, indicating that the data he wishes to send are on the data lines and stable. The recipient can then use this information on the inbound RDY line to generate a data strobe by which to strobe-in the incoming data into a receiving register or buffer. Upon receipt of the data the recipient signals the sender that the data have been successfully received. This is accomplished by releasing his outbound RSP line. As the sender detects the release of the inbound RSP, he releases his outbound RDY line as it is no longer required.

The SIA operates with level control as described above. Its inbound and outbound request lines are unidirectional while the RSP, RDY lines are bidirectional. The 920 operates on pulses in the form of outbound EOM pulses and inbound interrupt pulses. If one were to send a request-to-transmit pulse over an interrupt line to the 920, it may not, however, be prepared to receive unless preceded by an EOM message stating that this condition is also true.

In listing the sequences for each interface, attempts were made to keep them as uniform as possible. Secondly, each sequence is repetitive and requires no single unique directive such as initialization, buffer clear, or reset. Figure 4 shows the timing sequence for data transfer.

Additional stipulations pertain to the recognition of a single transition on a line, to noise filtering and synchronization, and to insertion of delays between the signals for easier recognition. Examples of such stipulations with a bearing on the implementation of the control circuits follow.

In order to combat noise and to synchronize the data transfer interface timing control signals to the internal clock of a recipient device, a signal transition is, in general, recognized only upon the second consecutive sample of the internal clock that the signal remains in its new state, and then only if the signal remained in its previous state for the same length of time. This specification is valid for transitions in either direction. Stated differently, a single noise pulse of either polarity of a duration less than 2 clock periods occurring at any time shall have no effect on the true operation.

VI. 920 EOM/Interrupt Summary

Between the four interfaces listed there are five EOMs and four interrupts used for each channel. They are listed in Table 1. The EOMs are decoded on the channel subassemblies. The interrupts are returned to the 920 through separate coax lines, four for each channel.

For a quick-look summary, Figs. 5 and 6 depict the four interfaces through arrow-and-number-labeled EOMs and interrupts.

VII. 920 I/O Register Interface and Data Transfer Protocol

The interface considered here is the parallel input-output operation through the computer's C-register, which is the method used for general communication. The 920/adapter interface operates in an open-loop configuration, relying on EOM requests and return interrupt responses. Parallel input-output operations, where a data transfer is involved, consist of two instructions, an EOM (energize output medium) instruction followed by either a POT (parallel output) or a PIN (parallel input) instruction.

VIII. Design Verification and Operational Acceptance Testing

A bench tester for the 900/SIA was designed and built at JPL for design verification and for bench checkout of manufactured units. It consists of a 900/SIA chassis with a separate built-in EOM sequencer which is controlled by the adapter interrupts. It serves as a test jig for the IC boards, there being two identical boards for each adapter. This tester could, with nominal effort, be updated to become another adapter.

The operational system test is a software test using a MODCOMP built-in 920 emulator and a special wrap-around test box or a Star Switch Controller from Buffer A channel 1 output to Buffer B channel 2 input. The hardware configuration is shown in Fig. 7.

IX. Design and Development Milestones

The detail design of the 900/SIA was a sole JPL effort during a three-week period. This included completion of detail logic and timing diagrams, as well as descriptive text. A detail design review and transfer of the design to contractor engineering personnel has been concluded. No engineering breadboard or prototype was built. Checkout of the contractor manufacturing prototype (first article) was a sole contractor effort concluded in a two-week period. Cursory system checkout using the Telemetry Processor Assembly (TPA) Mod Comp Emulator at CTA 21 was a combined contractor/JPL effort concluded during one week.

Final system checkout, which included the contractor-produced test software, was successfully concluded during a two-week period in April 1976. This was a combined effort between JPL hardware and contractor software personnel. During the above overall period, a JPL engineering prototype unit was being built and tested at JPL in parallel with the contractor-built unit.

X. Documentation

The original logic design diagrams provided the source information for the automatically produced sectionalized manufacturing drawings and associated wire lists. While the original diagrams are best suited to convey a functional understanding, the sectionalized drawings and associated wire lists are best suited for local troubleshooting.

The following is a list of the documents mentioned above:

(1) 920/adapter interface timing control circuitry.

(2) Buffer A data flow circuits.

(3) Buffer B data flow circuits.

(4) Adapter/SIA interface timing control (hand-shake) circuitry.

(5) Detail timing chart for Buffer A load/unload operation.

(6) Detail timing chart for Buffer B load/unload operation.

(7) Design verification sequencer, logic diagram.

Additional descriptive material relating to system circuitry is currently being prepared.

Table 1. List of 920/SIA adapter EOMs and interrupts

Sequence	EOM/interrupt	Description
1	EOM 1	920 Request to transmit to adapter Buffer A
1	EOM 2	920 to adapter Buffer A data transfer EOM 2/POT loop
1	EOM 3	920 to adapter Buffer A end-of-data block
4	EOM 4	920 ready to accept "request to transmit" from adapter Buffer B
4	EOM 5	Adapter Buffer B to the 920, data transfer EOM 5/PIN loop
1	Interrupt 1	Adapter response to 920, EOM 1, adapter ready to accept data EOM 2 from the 920
2	Interrupt 2	SSA time-out, data block transferred over interface 2 not complete, adapter to the 920, repeat sequence 2
4	Interrupt 3	Adapter Buffer B response to EOM 4 request to transmit
4	Interrupt 4	Adapter Buffer B empty, transmission complete

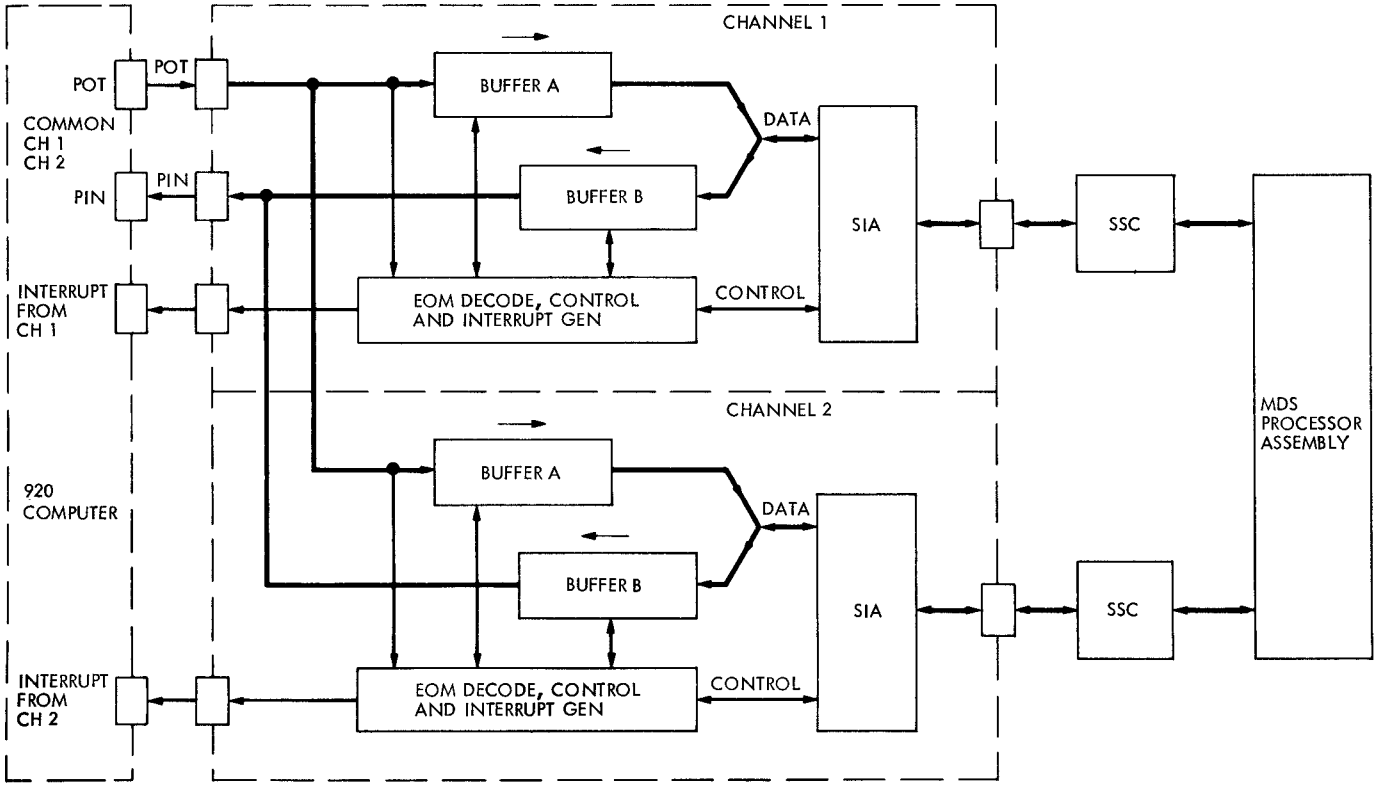

Fig. 1. 920/SIA Adapter and Buffer Assembly block diagram shown in subsystem configuration

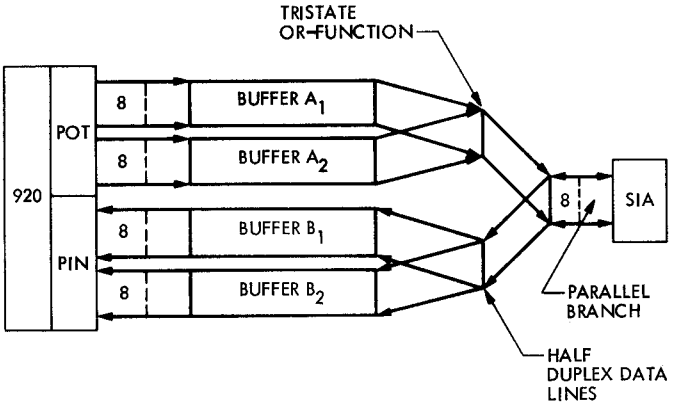

Fig. 2. Block diagram showing data buffer branches A_1, A_2, B_1, B_2 with no external data switching required

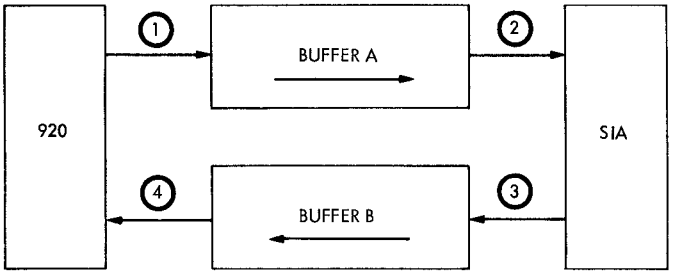

Fig. 3. Four major interfaces

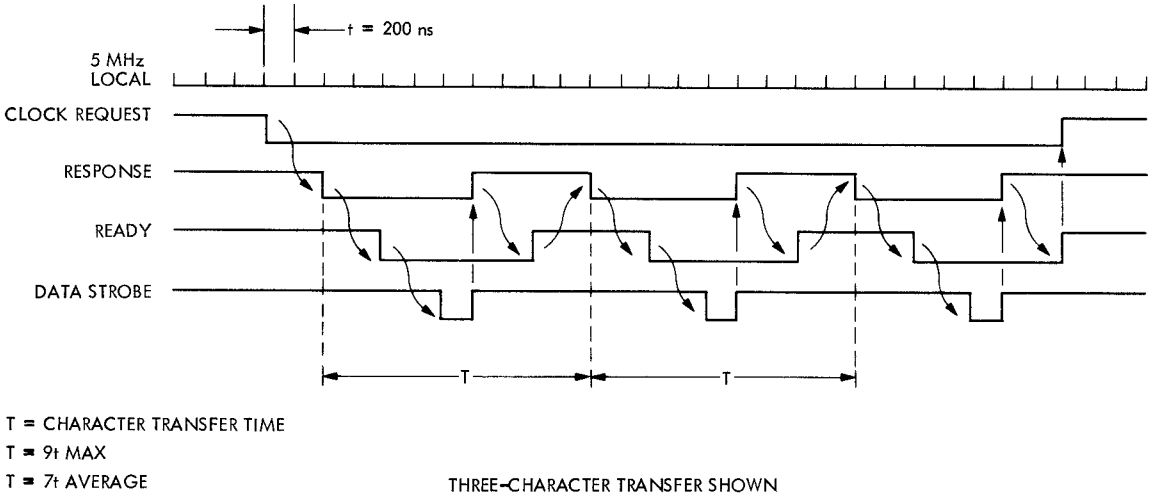

Fig. 4. Timing chart for the standard interface timing control lines

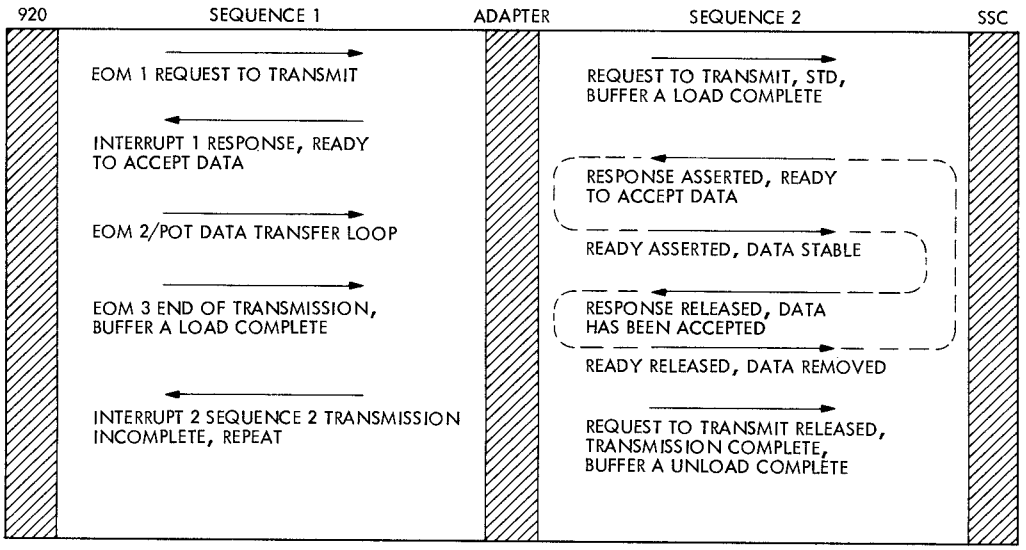

Fig. 5. Summary of interface sequences 1 and 2

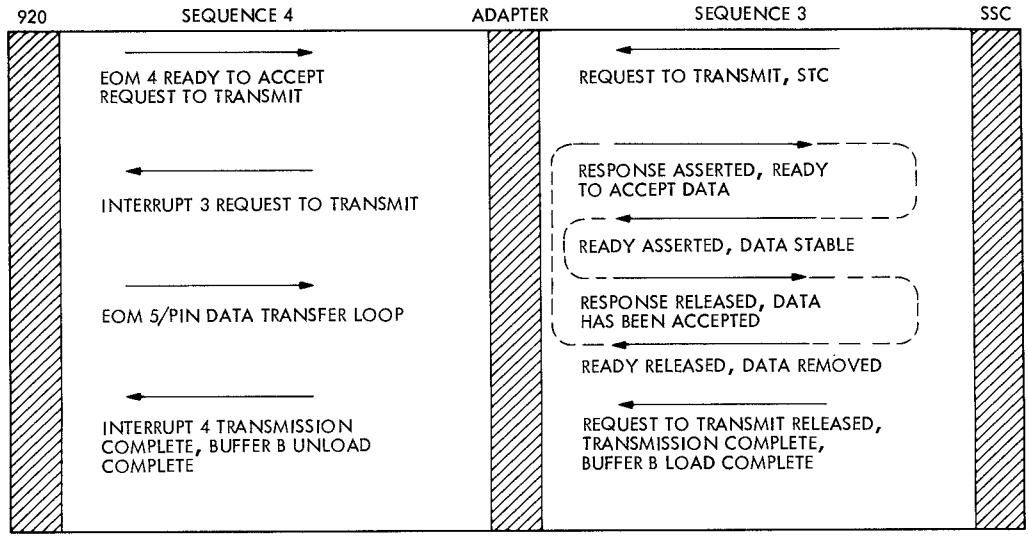

Fig. 6. Summary of interface sequences 3 and 4

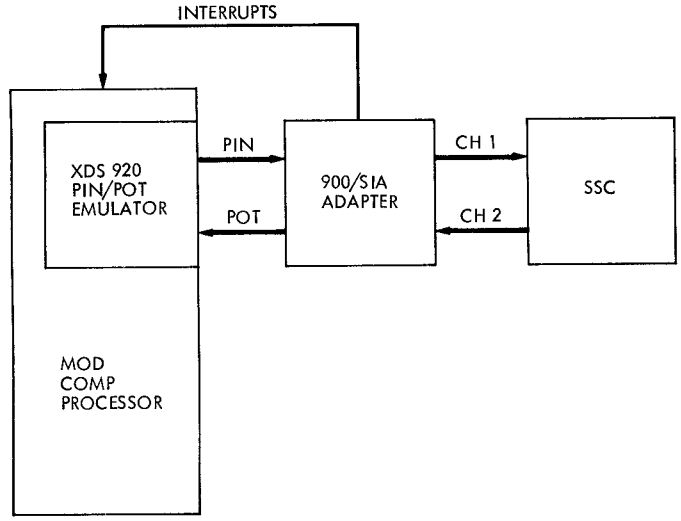

Fig. 7. Hardware configuration for 900/SIA software testing