Three-Level Sampler Having Automated Thresholds

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A three-level sampler is described that has its thresholds controlled automatically so as to track changes in the statistics of the random process being sampled. In particular, the mean value is removed and the ratio of the standard deviation of the random process to the threshold is maintained constant. The system is configured in such a manner that slow drifts in the level comparators and digital-to-analog converters are also removed. The ratio of the standard deviation to threshold level may be chosen within the constraints of the ratios of two integers N and M. These may be chosen to minimize the quantizing noise of the sampled process. Proper ratios have been given by Rodemich for gaussian random processes.

The advantages of computing autocorrelation functions from hard-clipped noise processes were originally formulated by VanVleck (Ref. 1). This procedure results in a degradation of the power spectra by a factor of $\pi/2$ and is usually offset by increasing the observing time by a factor of nearly 2.5. Rodemich demonstrated that considerable improvement could be made by extending the number of quantizing levels (Ref. 2). The new JPL-Haystack autocrosscorrelator system (HAC) can support 2×2 (usual hard-clipped mode), 3×2, and 3×3 level products in the formation of the autocorrelation function. This system has been described by Jurgens (Ref. 3). A one-bit data sampler having automated dc removal has been described by Brokl and Hurd (Ref. 4). Their procedure has been extended to a three-level sampler having automated dc removal and threshold tracking to remove amplifier gain variations in the receiver system and to establish optimum thresholds for minimizing the quantizing noise. The resulting sampler is designed with Motorola emitter-coupled logic (MECL) and operates in excess of 100 MHz. This note describes the operation of the sampler and the dynamics of the feedback loops.

Let $x(t)$ be a stationary zero-mean gaussian random process having variance σ_x^2. This process is assumed to be contaminated by drifts in the receivers and amplifiers such that a new time varying process $y(t)$ is formed, where $y(t) = a(t)x(t)+b(t)$. $a(t)$ and $b(t)$ are slowly varying, and $a(t)$ is always assumed to be greater than zero. The process $y(t)$ is to be sampled; however, the sampling thresholds may be chosen so as to remove the drifts $a(t)$ and $b(t)$ simultaneously. Figure 1 shows a simple three-level sampler which may be extended to operate for any number of levels. The voltages v_+ and v_- control the upper and lower thresholds of the comparators, respectively. The comparator C_1 gives a 1 state output when clocked if $y(t) > v_+$ and zero otherwise. The comparator C_2 gives a 1 state output if $y(t) < v_-$ and zero otherwise, three sample levels result and will be called 1, 0, and -1. The threshold voltages may be determined from certain running averages calculated from the outputs v_{10} and v_{20}. The system then acts simultaneously as an automatic gain control and a dc removal control.

Any number of schemes can be used to establish the feedback signals v_+ and v_-, but perhaps the simplest scheme is to force the average ratio of 1's to (0's plus -1's) to be a fixed ratio while simultaneously forcing the number -1's to (1's plus 0's) to maintain the same ratio as suggested by E. R. Rodemich. Figure 2 shows a simple scheme to accomplish this. The NOR gate, G1, yields a 1 state for 0's of the truth table of Fig. 1, and the 1's and 0's are merged by the OR gate G_2, and likewise the -1's and 0's by the gate G_3. The divide by N and divide by M counters establish a proper balance between the 1's and everything else and the -1's and everything else. If the counts going into the up-down counters UD1 and UD2 are on the average equally up and down the output count remains nearly constant and the voltage at the output of the digital-to-analog converters (DAC) remains constant. If, for example, the rate of 1's relative to the 0's and -1's is too large, UD1 will count upward increasing the output of DAC1 which raises the threshold voltage v_+ and decreases the 1's count rate. DAC2 generates the lower reference voltage which is normally negative.

The dynamics of the system may be modeled by observing that the up–down counters combined with the digital-to-analog converters act as integrators of the average rates of up counts minus the down counts. The equation for the v_+ signal may be written in terms of the rate of 1's, r_1, and the rate of 0's or -1's, r_0.

$$v_+(t) = S \int_0^t [r_1(u) - r_0(u)] du$$

where S is the sensitivity of the DAC, and the counters are assumed to be set to 0 at $t = 0$. $r_1(t)$ is clock rate times the probability of 1's divided by N, while $r_0(t)$ is the clock rate times the probability of 0's or -1's divided by M. Therefore if C_k is the clock rate, then

$$v_+ = s \int_0^t C_k\, P\{y > v_+(u)\}/N - C_k\, P\{y \leq v_+(u)\}/M \, du \qquad (1)$$

If the random process $x(t)$ is gaussian the probabilities in Eq. (1) may be calculated from the probability density functions of either x or y.

$$p(x) = \frac{1}{\sqrt{2\pi}\sigma_x} \exp\left[-1/2(x/\sigma_x)^2\right] \qquad (2)$$

and

$$p(y) = \frac{1}{\sqrt{2\pi}a\sigma_x} \exp\left[-(x-b)^2/2a^2\sigma_x^2\right] \qquad (3)$$

Thus

$$P\{y \leq v_+(t)\} = P\left\{x \leq \frac{v_+(t) - b}{a}\right\} = F_x\left(\frac{v_+ - b}{a}\right) \qquad (4)$$

where

$$F_x\left(\frac{v_+ - b}{a}\right) = \int_{-\infty}^{\frac{v_+ - b}{a}} \frac{1}{\sqrt{2\pi}\,\sigma_x} \exp\left[-1/2(x/\sigma_x)^2\right] dx \qquad (5)$$

and

$$P\{y > v_+(t)\} = 1 - F_x\left(\frac{v_+ - b}{a}\right) \qquad (6)$$

Replacing the probabilities in Eq. (1) with Eqs. (4) and (6) and differentiating both sides yields:

$$\frac{dv_+}{dt} = SC_k\left\{\frac{1}{N} - \left(\frac{1}{N} + \frac{1}{M}\right) F_x\left(\frac{v_+ - b}{a}\right)\right\} \qquad (7)$$

A somewhat more convenient form may be obtained by replacing $F_x(x)$ with

$$\frac{1}{2}\left[1 + \operatorname{erf}\left(\frac{x}{2\,\sigma_x}\right)\right]$$

giving

$$\frac{dv_+}{dt} = -1/2\, SC_k\left\{\left(\frac{1}{N} + \frac{1}{M}\right) \operatorname{erf}\left(\frac{v_+ - b}{\sqrt{2}\, a\sigma_x}\right) - \left(\frac{1}{N} - \frac{1}{M}\right)\right\} \qquad (8)$$

Likewise, the differential equation for $v_-(t)$ may be obtained:

$$\frac{dv_-}{dt} = -1/2\, SC_k \left\{ \left(\frac{1}{N} + \frac{1}{M} \right) \operatorname{erf} \left(\frac{v_- - b}{\sqrt{2}\, a\sigma_x} \right) + \left(\frac{1}{N} - \frac{1}{M} \right) \right\} \tag{9}$$

The arithmetic mean of v_+ and v_- is the effective mean or dc feedback signal, and one half the distance between the thresholds is the effective threshold or gain feedback signal, i.e.

$$v_{dc} = (v_+ + v_-)/2 \tag{10}$$

and

$$v_g = (v_+ - v_-)/2 \tag{11}$$

Equations (8) and (9) are first-order nonlinear differential equations having nonconstant coefficients and driving functions. If $a(t)$ is constant and greater than zero, the system is stable for all values of the product SC_k and the function $b(t)$. In practice, the up-down counters can overflow if the required threshold voltages fall outside the range of the DACs. In this case a continuous hunt condition is established until the values of a and b are restored to a range for which steady state may be achieved.

The steady-state conditions are found by setting dv_+/dt and dv_-/dt to zero in Eqs. (8) and (9). This yields

$$v_{+ss} = \sqrt{2}\, a\sigma_x \operatorname{erf}^{-1} \left(\frac{M - N}{M + N} \right) + b \tag{12}$$

$$v_{-ss} = \sqrt{2}\, a\sigma_x \operatorname{erf}^{-1} \left(\frac{M - N}{M + N} \right) + b \tag{13}$$

$$v_{dc} = b$$

$$v_g = \sqrt{2}\, a\sigma_x \operatorname{erf}^{-1} \left(\frac{M - N}{M + N} \right) \tag{15}$$

The ratio of $v_g/a\sigma_x$ is usually established to minimize the quantizing error in some manner. The values of M and N are chosen in Eq. (15) to closely approximate this ratio; however, large values of M and N increase the time constant of the system which may or may not be desirable. Rodemich has shown that a ratio of 0.612 yields a minimum variance for power spectra computed from the sampled data when quantized to 3 levels (Ref. 3). Values of $N = 4$ and $M = 11$ give a close approximation to this value and are sufficiently small as to permit a fairly rapid response time.

The effective cutoff frequency of the system may be determined by determining the small signal time constant of the differential equation near the steady-state operating point. This may be accomplished by letting $v_+ = v_{+ss} + \Delta v$ in Eq. (8). This leads to a first-order linear differential equation given as Eq. (16). The effective

$$\frac{d\Delta v}{dt} = -SC_k \left(\frac{1}{N} + \frac{1}{M} \right) \frac{1}{a\sigma_x} \exp\left(- \left[\operatorname{erf}^{-1} \left(\frac{M - N}{M + N} \right) \right]^2 \right) \Delta v \tag{16}$$

time constant is the reciprocal of the multiplier of Δv in Eq. (16) and is dependent upon the standard deviation of the input noise process, $\sigma_y = a\sigma_x$, as well as the physical parameters of the system. Figure 3 shows the response of the system when $b(t)$ is a unit step function. Note that $v_g(t)$ is disturbed momentarily by the positive step because $v_+(t)$ and $v_-(t)$ do not respond equally to a positive excitation. Also shown is the step response for $a(t)$ between 1.0 and 1.75 for b equal to zero. Digital computer simulation of the system using pseudorandom gaussian noise yields essentially the same results.

Frequency analysis of the sampled function verifies that the dc components of y are removed and that the thresholds are properly established. The threshold signals exhibit a jitter caused by the stochastic nature of the sampled signal and due to the finite resolution of the digital-to-analog converters. The low-frequency components of the signal are, of course, tracked out causing the system to act as a high-pass filter having a cutoff frequency defined by the time constant of Eq. (16). If N and M are made arbitrarily large with the proper ratio maintained, the cutoff frequency may be made arbitrarily low. The dc offsets and slow drifts would be tracked out, and the fluctuation of the threshold voltages v_+ and v_- would be due primarily to the finite resolution of the DACs and equal in peak-to-peak voltage to the voltage resolution of the DACs.

References

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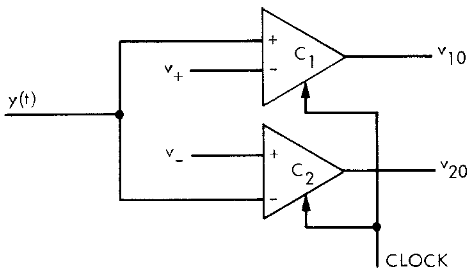
4. Brokl, S. S., and Hurd, W. J., "Digital DC Offset Compensation of Analog-To-Digital Converters," in *The Deep Space Network*, Technical Report 32-1526, Vol. XVII, pp. 45–47, Jet Propulsion Laboratory, Pasadena, Calif., Oct. 15, 1973.



v_{20}	v_{10}	SAMPLE STATE
0	0	0
0	1	1
1	0	-1
1	1	NOT POSSIBLE

Fig. 1. Simple three-level sampler and output truth table defining the three states in terms of the comparator output signals v_{10} and v_{20}

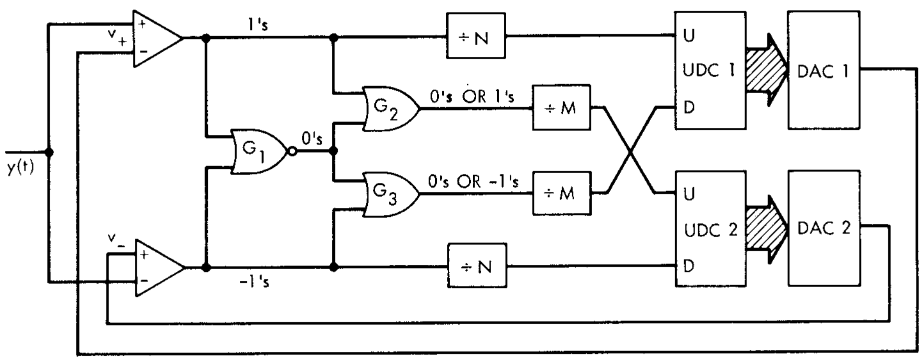


Fig. 2. Block diagram of a simple feedback controlled designed to establish the threshold voltages v_+ and v_- so as to remove dc offsets and gain variations in the input signal

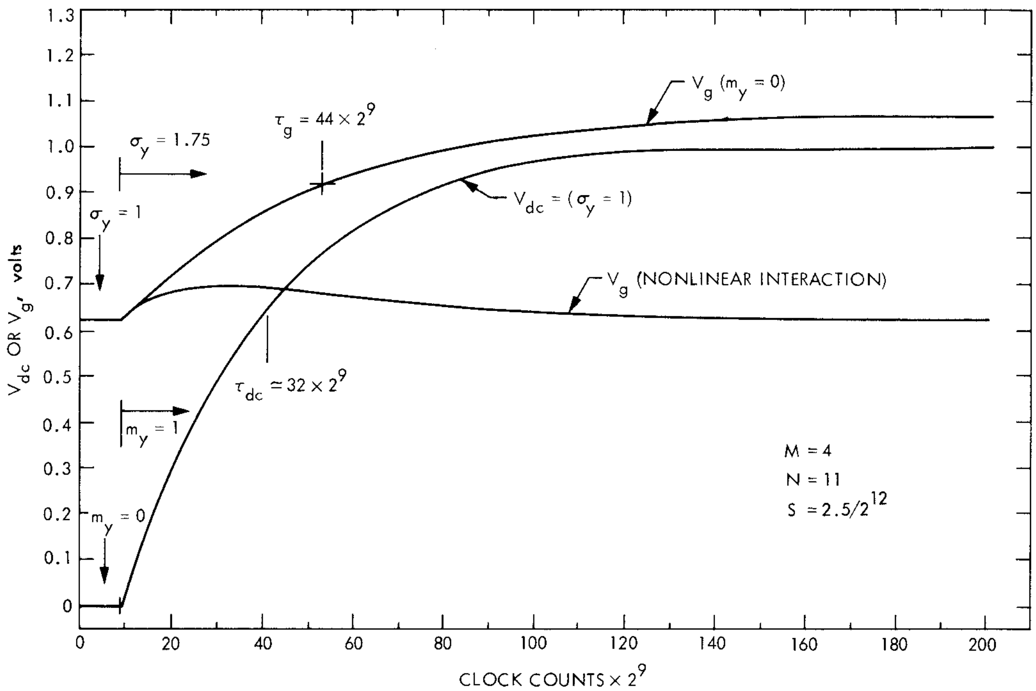


Fig. 3. Response of effective feedback signals v_g and v_{dc} to step function excitations in the mean m_y and the standard deviation σ_y. The interaction of v_g for a step in m_y is also shown. The relative size of the interaction becomes smaller as the step size is decreased.