# Implementation of a Maximum Likelihood Convolutional Decoder in the DSN

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*The DSN is implementing a high data rate convolutional decoder capability for mission support starting in 1977. This article describes the development status of this decoder and the factors which were considered in defining the specific functional requirements. The design is discussed to the block diagram level. A description of the detailed design is provided, along with a description of the test software developed and a brief summary of the performance evaluation testing completed so far.*

## I. Introduction

Beginning in late 1976, a new telemetry convolutional decoding capability will be implemented throughout the Deep Space Network (DSN) at the nine Deep Space Stations (DSSs), in response to data system requirements specified for supporting the Mariner Jupiter-Saturn (MJS'77) flight project. This new decoder, called the Maximum Likelihood Convolutional Decoder (MCD), utilizes the Viterbi decoding algorithm, and operates on short constraint length ($K = 7$) convolutional codes, providing a coding gain of about 5 dB (over uncoded data), at data rates from 10 to 250,000 bits per second. This maximum rate is significantly higher than the maximum convolutional coded data rate of 2048 bits per second presently available throughout the DSN, using sequential decoding and the Fano algorithm, as implemented in the Data Decoder Assembly (DDA). Maximum likelihood decoding allows higher data rates because a large part of the required computations can be performed in parallel.

The MCD is a special-purpose digital computing device which decodes in real-time, high-rate, short-constraint length convolutionally encoded data received from a spacecraft at a DSS. It operates as a component within the DSS Telemetry Subsystem, receiving coded, quantized symbols from a Symbol Synchronizer Assembly (SSA) and outputting decoded data to the Telemetry Processor Assembly (TPA). The TPA formats and outputs this data stream to the Mission Control Center via the Ground Communication Subsystem. The TPA controls and monitors the operation of the MCD, as well as receiving its decoded data.

## II. Specific Functional Requirements

The selection of the required codes and code rates, maximum data rate, and system interconnections was completed very early in the overall effort (Ref. 1). Alternate symbol inversion was an added requirement imposed during the development phase to assure adequate symbol transition density.

The salient functional requirements defined for the MCD, and the factors used in their selection, are discussed briefly below.

### A. Codes and Code Rates

**1. Short constraint length ($K$ = 7).** Provides simplified encoder design, adequate decoding performance and reasonable computational load (proportional to $2^K$).

**2. Transparent codes.** Provide minimum length initialization interval (called node synchronization or proper grouping of incoming symbols into pairs, for code rate 1/2, or triplets for code rate 1/3).

Transparency indicates that either inverted or non-inverted input symbols are acceptable and produce correspondingly inverted or non-inverted decoded data.

**3. Code rates 1/2 and 1/3.** Both rates are provided, 1/2 to satisfy a current flight project requirement and 1/3 to provide growth capability for future requirements. (Rate 1/3 offers about a 0.3-dB improvement over rate 1/2, but at the expense of reduced data rate, for a given symbol rate.)

### B. Maximum Data Rate—250 kilobits/second

Selected to be roughly double the existing SSA maximum symbol rate capability, to provide for future SSA rate increases, if required.

### C. Decoder Bit Error Rate

Provides current state-of-the-art performance capability, as tabulated below.

| Bit error rate | Code 7-1/2 $E_B/N_0$, dB | Code 7-1/3 $E_BN_0$, dB |
|---|---|---|
| $10^{-3}$ | 3.0 | 2.7 |
| $10^{-4}$ | 3.8 | 3.5 |
| $10^{-5}$ | 4.5 | 4.2 |
| $10^{-6}$ | 5.2 | 4.9 |

### D. Built-In Hardware Self-Test

Provides a rapid pass/fail check of decoder operability, for both code rates.

### E. System Interfaces

**1. Symbol inputs.** Received from the Symbol Synchronizer Assembly (SSA), in the form of 5-bit parallel binary numbers (quantized to 1 of 8 levels).

**2. Data output and control.** The MCD communicates with the TPA via built-in circuitry that satisfied the JPL standard 14-line interface requirement (as defined per Ref. 2), receiving mode commands from the TPA, and sending interleaved status and data bytes (8 bits per byte) to the TPA.

## III. Detailed Design Description

A brief summary of the design is presented as follows. A detailed design description is provided in the MCD Instruction Manual (Ref. 3).

### A. System Interfaces (see Fig. 1)

A block diagram of the MCD system interconnections is shown in Fig. 1, with the interfaces as previously mentioned.

### B. Input/Output Section (see Fig. 2)

The following subsections are provided:

(1) Symbol input receivers and converter, for SSA inputs.

(2) Data output register and drivers, to DDA.

(3) Standard interface receivers, drivers, registers and control logic provided for TPA communication.

### C. Decoder Section (see Fig. 3)

**1. Input processor.** Generates the branch metric values associated with the allowable branches through the decoder trellis diagram. There are 128 allowable branches for each input symbol pair (code rate 1/2). The lower the branch metric value, the better is the correlation between the possible branch and the quantized symbol pair received.

**2. Arithmetic processor and state metric memory.** The arithmetic processor, operating with the state metric memory, updates each of the $2^{K-1}$, or 64, decoder states for each symbol pair received, by adding the appropriate branch metric values to the previously computed and stored state metric values, and then storing the better (or lesser) of the two sums

as the new state metric value. This is equivalent to selecting and storing the most likely of the two possible branches for entering each decoder state.

3. **Path memory.** For each state, a path history consisting of the most recent 64 bits that define the best path leading to that state is also stored in the path memory. It is the oldest path bit, of the state with the lowest accumulated state metric value, that is the decoded data bit output by the decoder after each symbol pair is received.

4. **Node synchronization.** The node synchronization circuitry performs the function of properly grouping the incoming symbols into pairs (code rate 1/2). It does this by grouping so that all state metric values build up at the slower of two rates, as detected by the rate of the state metric normalization counter. All state metrics are normalized by subtracting a fixed constant from each metric whenever all metrics are above a certain threshold value. This normalization rate is an indicator of the quality of input symbols, or symbol error rate, being input to the MCD, and also roughly indicates decoder output bit error rate (BER). This rate is output from the MCD as a 4-bit number, within the 8-bit status byte.

### D. Self-Test Section (see Fig. 4)

Whenever the MCD is commanded to enter the self-test mode, a procedure consisting of three phases is automatically performed. The first phase consists of initializing and/or clearing all control, state metric, and path memory values to predetermined values. In the next two phases the decoder operates in its normal decoding manner, utilizing simulated input symbols derived from a self-contained PN sequence generator. The number of decoded 1's is counted during these two phases, (one phase for code rate 1/2, and one phase for code rate 1/3), and the total at the end of the test is compared with a prestored value. This value is known because the PN sequence is random but exactly repeatable. A status bit is set at the end of the test, indicating the result of the test.

### E. Physical Characteristics

(1) Size: rack-mounted unit, 13.3 cm (5-1/4 inches) high, 37.5 cm (14-3/4 inches) deep, 48.3 cm (19 inches) wide.

(2) Weight: 6.7 kg (14-3/4 lb).

(3) Power consumption: 100 watts (max), 120 Vac (±10%).

(4) Operating temperature (ambient): 13°-38°C (55°-100°F).

(5) Cooling: self contained internal fan.

(6) Reliability: computed mean time between failures (MTBF) greater than 8000 hours, using MIL-HDBK-217B, based on a total IC count of 154 units, all of MIL-STD 883 Level B quality.

(7) Operating life: 10 years minimum.

## IV. Testing and Evaluation

### A. Acceptance Testing

A typical acceptance test data sheet is shown as Fig. 5.

### B. Test Software

1. **MCD Test Program.** This program was developed during the same time span as that allotted for the prototype MCD development, using the MCD simulator as a tool for program checkout. Using this parallel approach, the program was almost totally checked out and operable at the time that the prototype unit was delivered.

The program resides in the TPA. Its primary functions are:

(1) To evaluate and verify the modes of MCD operation, including *self-test* and *operate*, for both code rates.

(2) To validate all modes of communication between the MCD and TPA, including interleaved *commands, status,* and *data* transfers.

(3) To monitor and report on MCD status, including validation of both types of MCD status outputs (responses to read status commands from the TPA, and also self-generated status outputs whenever an MCD internal sync change occurs in response to a high normalization rate condition).

In order to accomplish these functions, the program performs the following sequence of operations:

(1) Commands the MCD to the *operate* and then to the *self-test* modes.

(2) Receives and stores about 4000 bits of the PN sequence received from the MCD during *self-test.*

(3) Examines the stored data sequence to find the frame sync reference (127 consecutive 0's), and then compares each bit following frame sync with a stored reference pattern.

(4) Monitors and evaluates both types of MCD status outputs.

(5) Outputs pass/fail messages to the Terminet at the end of the test.

This program is intended to be used as a convenient tool for performing a rapid GO-NO GO test to verify the operational readiness of the MCD and its operation with the TPA. It is used both at JPL and at the DSN integration contractor (Univac) for this purpose.

2. **MCD Performance Evaluation Program (MCDPEP).** This program was developed early in 1976 to support extensive performance evaluations of the MCD, while operating within a typical telemetry string (Receiver-Subcarrier Demodulator-SSA-MCD-TPA), with simulated encoded data provided from the Simulation Conversion Assembly (SCA). These tests were performed at the JPL Compatibility Test Area (CTA 21) and the results were evaluated using a companion data reduction program called MCD DAP (Data Analysis Program). This latter program was used to compute and output MCD burst error statistics as well as error-free run length and other performance statistics, including BER versus input symbol error rate (SER).

Extensive testing was done at CTA 21 to evaluate many different combinations of data rates (from 115.2 to 44.8 kilobits per second), with the Block 4 Receiver operating in both S- and X-band modes, at various signal levels ($E_s/N_o$) and Receiver and Subcarrier Demodulator bandwidth settings. The results obtained are in close agreement with the nominal MCD bit error rate performance. These results are summarized in Ref. 4.

### C. Other MCD Testing

Late in 1975 a production MCD was provided to the JPL Spacecraft Telecommunications Systems Section where extensive MCD performance evaluation tests were performed in the Telemetry Development Laboratory, with the MCD operating with a Receiver-Subcarrier Demodulator-SSA.

The results of these tests were entirely satisfactory, with the MCD meeting (or exceeding) the BER performance requirements specified in the TRD.

## V. Conclusion

The entire MCD development effort has proceeded in an orderly and satisfactory manner, with relatively few changes of any kind required, and has closely followed all aspects of the original development plan including cost, delivery schedule, and meeting of performance requirements.

## References


1. Alberda, M. E., *Technical Requirements Document for Maximum Likelihood Convolutional Decoder (MCD),* JPL TRD 338-256, Rev. E, November 1975 (JPL internal document).

2. *Detailed Specification for Deep Space Network Standard Interface,* JPL Equipment Specification, ES 508534, Rev. B, November 1974 (JPL internal document).

3. *Instruction Manual, Maximum Likelihood Convolutional Decoder (MCD) LV 7035 Viterbi Decoder,* Linkabit Corp., San Diego, CA, January 1976.

4. Benjauthrit, B., et al., "DSN Telemetry System Performance With Convolutionally Coded Data Using Operational Maximum-Likelihood Convolutional Decoders," in *The Deep Space Network Progress Report 42-36,* pp. 81-101, Jet Propulsion Laboratory, Pasadena, Calif., Dec. 15, 1976.

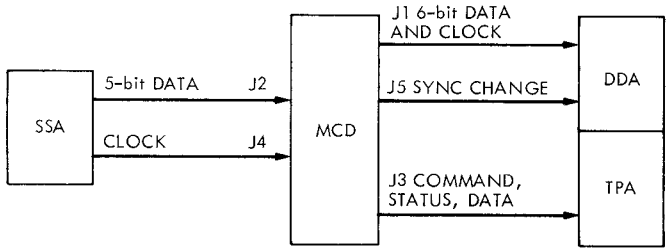


**Fig. 1. MCD system block diagram**

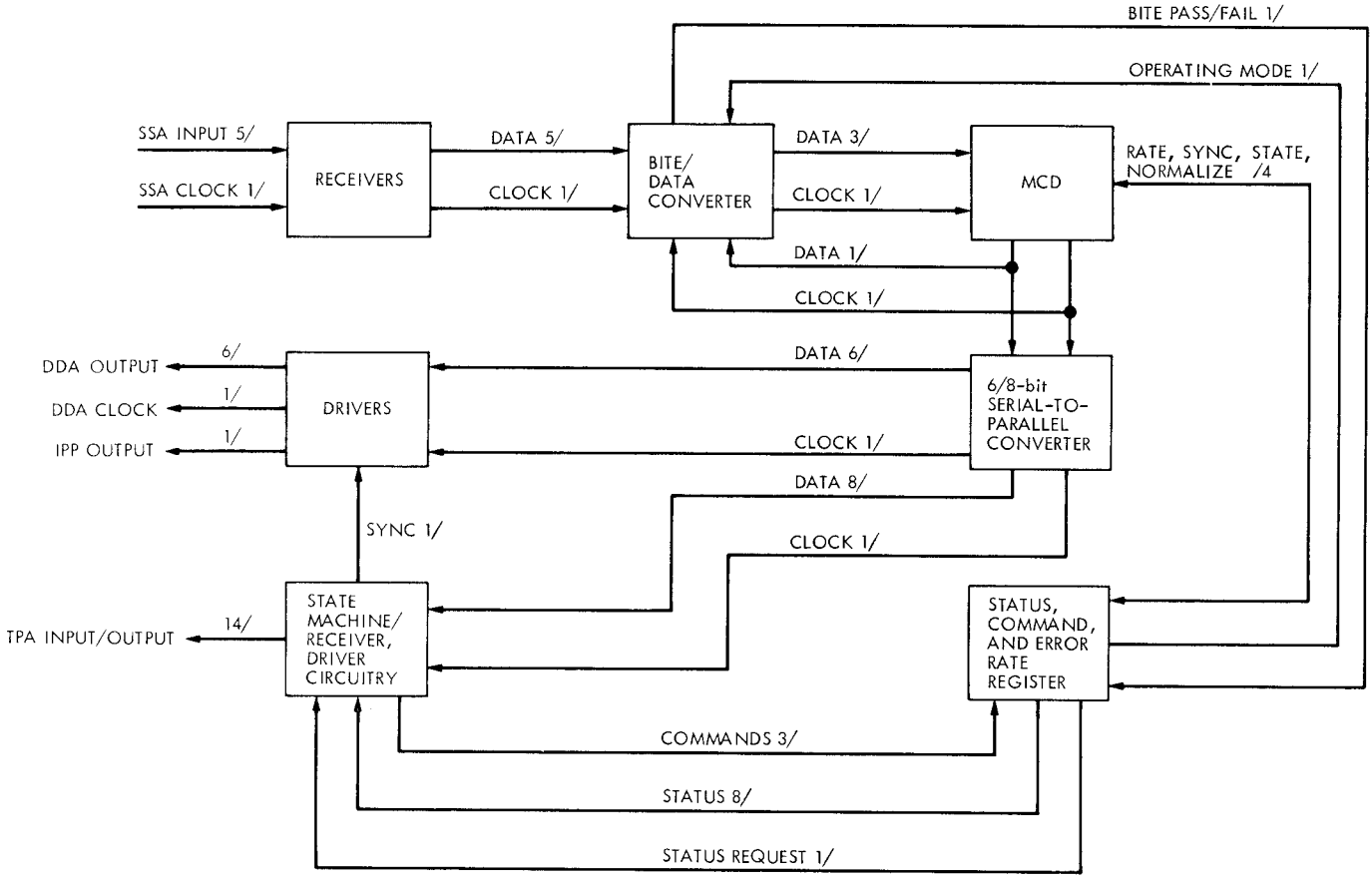


**Fig. 2. MCD input/output section block diagram**

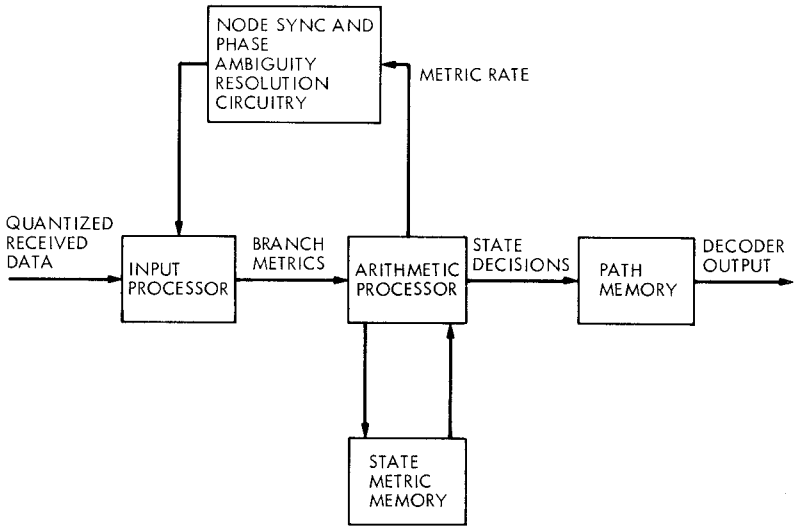


**Fig. 3. MCD decoder block diagram**

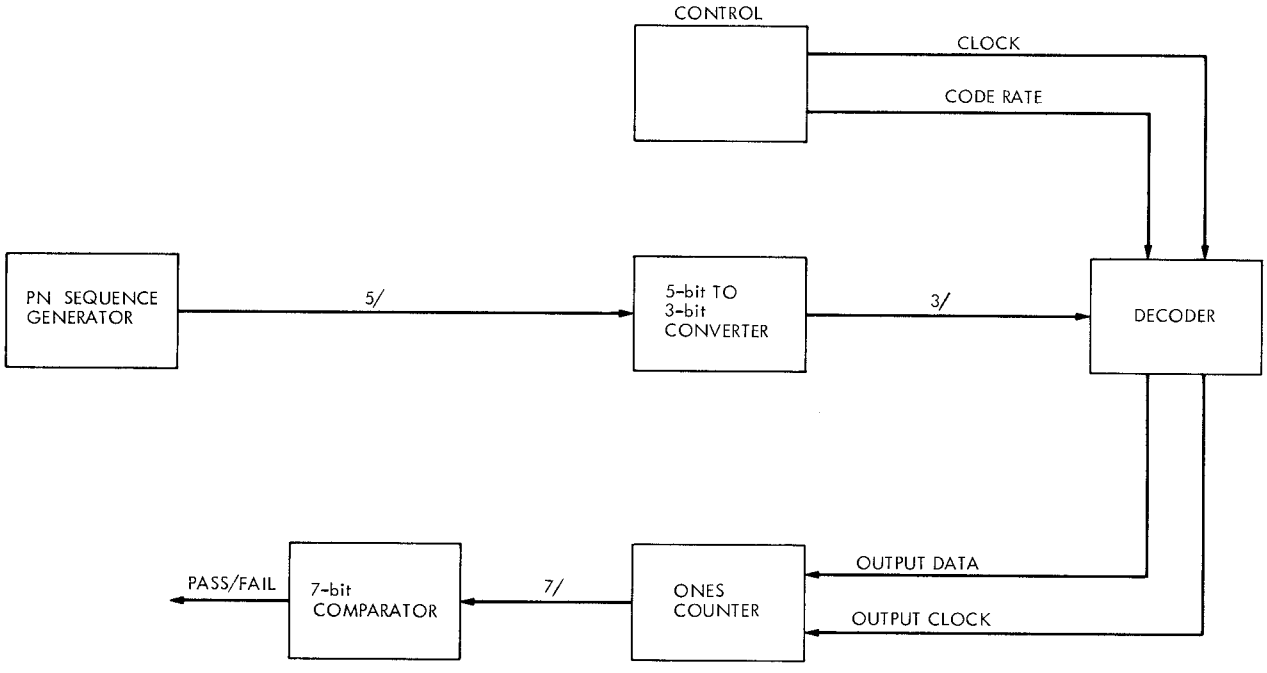


**Fig. 4. MCD self-test block diagram**

TESTING DATE

10NOV75

SERIAL NO.

0002

(3.1) TESTER BUILT-IN TEST

| OBSERVED | REQUIRED | PASSED | FAILED |
|---|---|---|---|
| 00A3 | 00A3 | X | |

(3.2) ERROR RATE PERFORMANCE

MCD-TPA

| RATE | EB/NO | NO. BITS | NO. ERRORS | ERROR RATE | UPPER BOUND | PASSED | FAILED |
|---|---|---|---|---|---|---|---|
| 1/2 | 3.0 | 0.4096E 07 | 3028 | 0.7392E-03 | 0.9000E-03 | X | |
| 1/2 | 4.0 | 0.4096E 08 | 1621 | 0.3957E-04 | 0.6000E-04 | X | |
| 1/2 | 5.0 | 0.6553E 08 | 89 | 0.1358E-05 | 0.2500E-05 | X | |
| 1/3 | 3.0 | 0.4096E 07 | 1107 | 0.2702E-03 | 0.3600E-03 | X | |
| 1/3 | 3.5 | 0.4096E 08 | 2901 | 0.7082E-04 | 0.1000E-03 | X | |
| 1/3 | 4.5 | 0.4096E 08 | 103 | 0.2514E-05 | 0.7000E-05 | X | |

MCD-DDA

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1/3 | 3.0 | 0.4096E 07 | 1234 | 0.3012E-03 | 0.3600E-03 | X | |

(3.3) MCD SYMBOL SYNCHRONIZATION RECOVERY

| SYMBOLS DROPPED | NO. SYMBOLS TO RECOVERY | PASSED | FAILED |
|---|---|---|---|
| RATE 1/2 | | | |
| 1 | 162 | X | |
| 1 | 186 | X | |
| 1 | 186 | X | |
| 1 | 198 | X | |
| 1 | 186 | X | |
| 1 | 192 | X | |
| 1 | 192 | X | |
| 1 | 186 | X | |
| 1 | 192 | X | |
| 1 | 174 | X | |
| RATE 1/3 | | | |
| 1 | 156 | X | |
| 1 | 144 | X | |
| 1 | 138 | X | |
| 1 | 132 | X | |
| 1 | 144 | X | |
| 2 | 318 | X | |
| 2 | 318 | X | |
| 2 | 288 | X | |
| 2 | 312 | X | |
| 2 | 282 | X | |

**Fig. 5. MCD acceptance test data sheet (typical)**

(3.4) MCD BUILT-IN TEST EQUIPMENT

| FAULT INSERTED | BITE VALUE | PASSED | FAILED |
|---|---|---|---|
| NO | 1 | X | |
| YES | 0 | X | |

(3.5) CHANNEL ERROR RATE TEST

| RATE | EB/NO | AVERAGE | LOWER BOUND | UPPER BOUND | PASSED | FAILED |
|---|---|---|---|---|---|---|
| 1/2 | 3.0 | 11.0 | 10 | 13 | X | |
| 1/2 | 4.0 | 8.4 | 7 | 9 | X | |
| 1/2 | 5.0 | 4.6 | 4 | 6 | X | |
| 1/3 | 3.0 | 10.5 | 10 | 12 | X | |
| 1/3 | 3.5 | 10.0 | 9 | 11 | X | |
| 1/3 | 4.5 | 7.1 | 6 | 8 | X | |

(3.6) CODE RATE AND MODE STATUS INDICATORS

| OBSERVED D3 | OBSERVED D4 | REQUIRED D3 | REQUIRED D4 | PASSED | FAILED |
|---|---|---|---|---|---|
| | 0 | | 0 | X | |
| | 1 | | 1 | X | |
| 0 | | 0 | | X | |
| 1 | | 1 | | X | |

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Fig. 5 (contd)