A High-Speed Computer Link for Moderate Distances and Noisy Environments

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To satisfy the need for a fully duplex high-speed computer data link for the antenna automation project at DSS 13, a very simple and inexpensive scheme was employed. The link requires two coaxial cables over which is sent a unipolar "digital frequency modulated" signal in which a logical 1 has twice the frequency of a logical 0. Optical isolators and filters reduce ground loop effects and increase noise immunity. Tests conducted in various environments and over different cable lengths at JPL, DSS 14 and DSS 13 have indicated that the link is highly effective.

I. Motivation

As part of the automation project being conducted at DSS 13, a need arose for a high-speed, fully duplex communication link between a microprocessor located in the teepee of the 26-meter antenna and a minicomputer located approximately 500 meters away in the control room. The harsh electrical environment at DSS 13 necessitated incorporating circuitry that was resistant to ground loops and large noise spikes.

It was desired to make the link hardware as insensitive to environmentally induced faults as possible while keeping it reasonably simple. The philosophy taken was to accept faults occurring with low to moderate probability but with high coverage (coverage is the conditional probability that a system can recover from a fault given that a fault has occurred). So fault detection is as important in the link design as fault prevention. Clearly, since the most probable type of fault, i.e., single bits, burts, etc., is a function of the nature of the electrical environment, a provision was made for incorporating various fault detection schemes or combinations of schemes in the link design to permit the use of the link in environments other than that at DSS 13.

II. Link Implementation

The link was implemented using identical modules at each computer consisting of transmitter and receiver submodules. One computer transmits to the other computer via one coaxial cable and receives from the other computer via another coaxial cable. In each transmitter and receiver submodule, a first-in-first-out (FIFO) data buffer facilitates achieving the full duplex nature of the link as well as providing a means for synchronizing the computers to the link.

Link data are encoded into a "digital frequency modulation" (DFM) signal, which encodes a logical one at twice the frequency of a logical zero. Figure 1 illustrates the modulation technique as well as the timing used in the DSS 13 link. As shown, each bit period is divided into two subperiods. The clock subperiod (C) signals the start of a bit period and is followed by a data subperiod (D). The duty cycle of the pulses as well as the separation between pulses was chosen so that the transient effect of charging the coaxial cable by a given pulse had sufficient time to decay before the occurrence of the next pulse.

A Poisson distribution was assumed for the nature of the environmental noise at DSS 13. That is, it was assumed that the probability that a given noise spike has duration t is $e^{-\lambda t}$ for some λ, a constant. It was further assumed that 95% of all noise spikes would be of duration 200 nanoseconds or less (λ = 0.015), so that if a lowpass filter eliminated all pulses of less than 300 nanoseconds, about one noise spike in 100 has a chance of being passed by the filter if no other precautions are taken.

Although this result by itself is not acceptable, when coupled with the probability of a pulse of duration greater than 300 nanoseconds having sufficient amplitude to be incorrectly interpreted, the link fault rate is reduced to an acceptably small level. Since noise spikes tend to result in common mode noise, a differential receiver front end cancels most of the effect of a noise spike. In the link, an optical isolator serves the dual function of a ground loop desensitizer and differential receiver.

It is not known at this time what the actual link fault rate is. The link has not yet made an error in approximately 10^8 bits during several hours of testing at JPL, DSS 14 and DSS 13.

III. Link Transmitter

A block diagram of the link transmitter is shown in Fig. 2. The host specific interface connects the transmitter section to the host computer that drives it. This interface communicates with the FIFO input control logic, which strobes data into a 256 by 8 FIFO data buffer. This buffer was constructed from Advanced Micro Devices 2841A 64X4 FIFO chips. The operation of the FIFO buffer is asynchronous with respect to its input and output, and thus the host computer may be entering data into the FIFO while the link is removing data.

A transmit enable flip-flop in the output control–data formatter enables data from the FIFO buffer output and parity encoder to be shifted out. The 9-bit even parity serial word is output to the coaxial cable via a high-current 75450 series driver terminated in the characteristic impedance of the coaxial cable.

At the heart of the output control–data formatter is a glitchless three-phase clock, illustrated in Fig. 3. A 4-bit binary counter counts block pulses applied to it. The three most significant bits are decoded by a four- to ten-line decoder. A single output of the decoder becomes true as a function of the four input lines. The enable line connected to the most significant input of the four- to ten-line decoder is derived from the transmit enable flip-flop.

The output of the decoder is inverted and clocked into D flip-flops by the least significant bit from the counter. This guarantees glitch-free clock pulses with phase $\phi 1$ present first, followed by $\phi 2$ then $\phi 3$.

The parallel to serial shift register is clocked by the trailing edge of $\phi 1$. Each time a new word is to be loaded into the shift register, a flip-flop in the output control-data formatter is set. This flip-flop holds the load enable line true on the shift register, which is then loaded by the trailing edge of $\phi 1$. $\phi 2$ clears the load enable flip-flop and is output as the clock pulse. At $\phi 3$, the output of the shift register is gated out and a bit counter within the output control–data formatter is incremented. The bit counter is decoded and determines when to advance the FIFO output and when to load the next word into the shift register. The output process continues until the FIFO is empty or the transmit flip-flop is cleared by the host interface.

The output control–data formatter also signals the host interface when the FIFO buffer has been cleared. This signal is used by the host interface to generate an interrupt to give the computer an indication of when it may send the next data block. In the DSS 13 configuration, this interrupt is used to fill the transmit buffer with new data if any is to be sent, but the transmit flip-flop is not set to transmit at this time. The link depends on a software handshake process for synchronizing input and output. A sending computer must wait for a message from the receiving computer signaling that it can accept a new transmission. Upon receipt of this message, the sending computer may send another block.

It should be noted that while this handshaking method is simple and effective, if not carefully applied, it can lead to a deadlock problem, e.g., neither computer is transmitting because both are waiting for an acknowledge message from the other. What was done at DSS 13 was to give the minicomputer master status. It sends a request to the microprocessor, which acts as a slave, for data and waits for that data before sending the next request. The microprocessor does not send data to the minicomputer unless it is requested to do so.

IV. Link Receiver

After isolation and filter circuits, the DFM signal is split into data and clock pulses in the data-clock pulse separator (Fig. 4). This module assumes that the first pulse it receives is always a clock pulse. Internally, a data bit latch circuit is cleared by each clock pulse and set if a data pulse is present. A strobe pulse is issued after a delay sufficiently long to guarantee that a data pulse is latched. The strobe pulse is used to clock the output of the data bit latch into a serial to parallel shift register. The parallel word is scanned for the presence of a synchronization (sync) word. If a correct parity sync word is found, the sync detector latch is set and data may be strobed into the FIFO buffer. If the data stream vanishes for a "long" period of time, e.g., 16 clock periods, the sync detector latch is cleared.

The FIFO input control waits for the sync detector to find the sync word. It strobes the sync word into the FIFO buffer and starts a bit counter. Each time a new word is available in the shift register, it strobes that word into the FIFO. FIFO input control also monitors the FIFO buffer status and signals the host specific interface when the FIFO is filled. This interface issues a computer interrupt to indicate that data is available to be read.

The host interface reads data from the FIFO buffer under computer control and signals the FIFO output control when it has transferred the data word to the computer. Output control then signals the FIFO to present the next word at its output.

Any time the parity check circuitry detects a bad parity word after the sync detector is set, it signals the host interface. This signal is used by the host interface to generate a computer interrupt.

As noted in Section I, fault detection and recovery have been left to the software. Although sophisticated detection-correction schemes are possible, the DSS 13 link employs a simple 16-bit check sum for fault detection. This scheme detects all errors not a multiple of 2^{16}. Recovery can be simply accomplished by retransmission of the data block in error. As noted in the previous section, a software handshake is performed to synchronize the sending and receiving computer. The acknowledge message sent by the receiving computer contains a word that lets the sending computer know if the block it just sent was received with an error. Normally, this error message could be used to request that the same block be retransmitted. This is not presently done at DSS 13 since, in this particular application, it is not required.

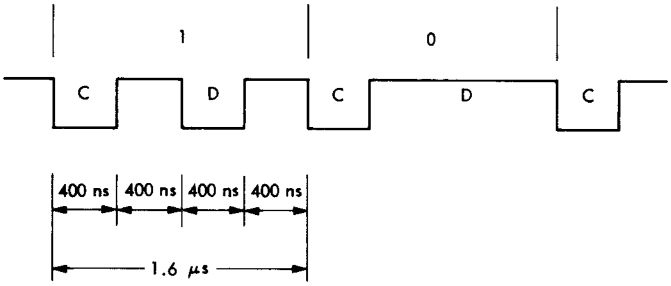

Fig.1. Digital frequency modulation

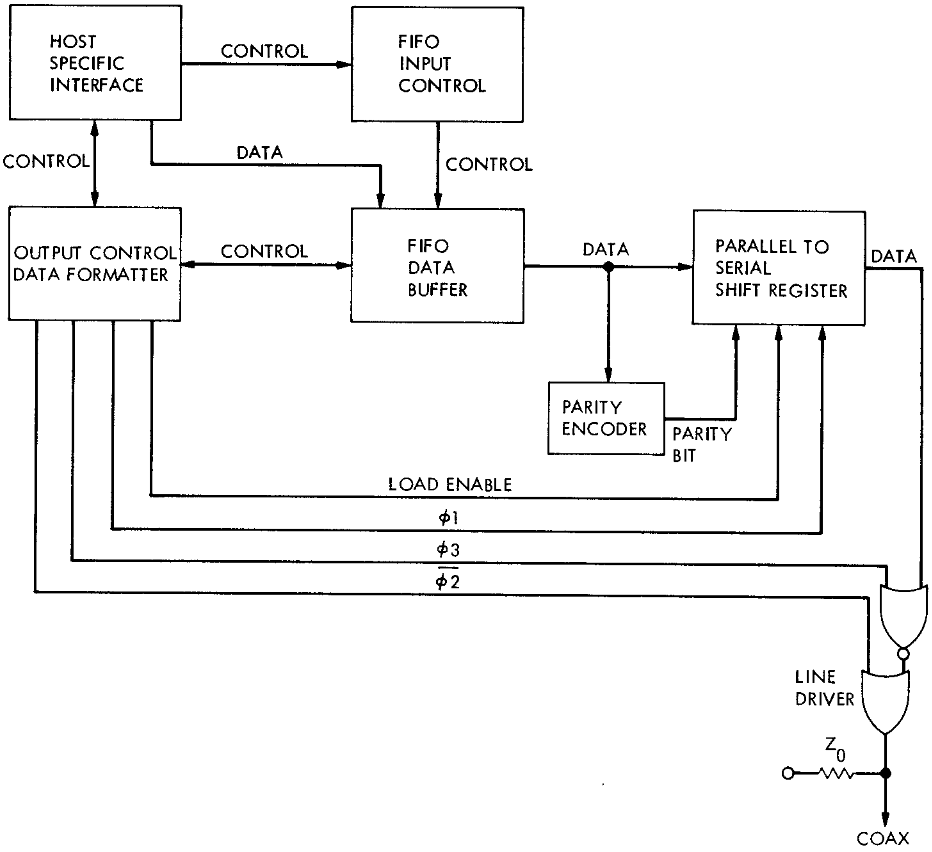

Fig. 2. Transmitter module

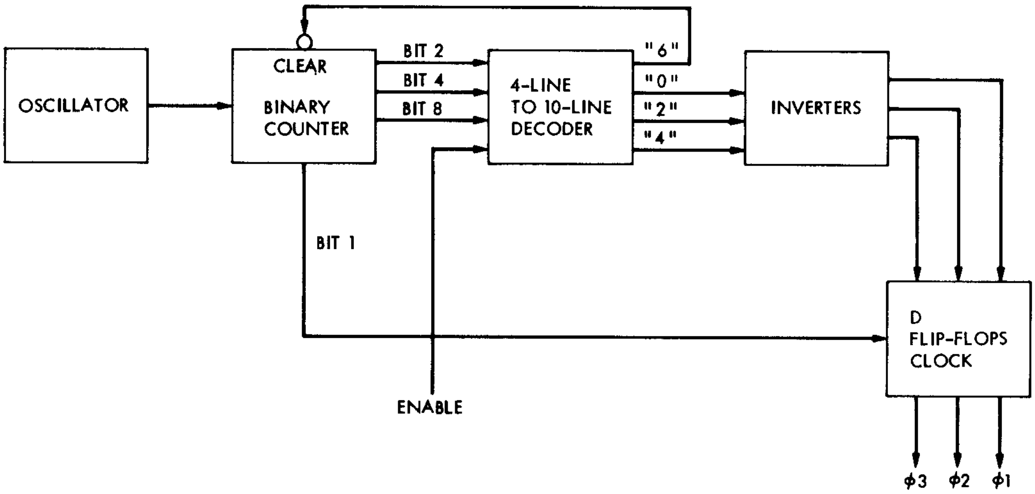

Fig. 3. Three-phase clock

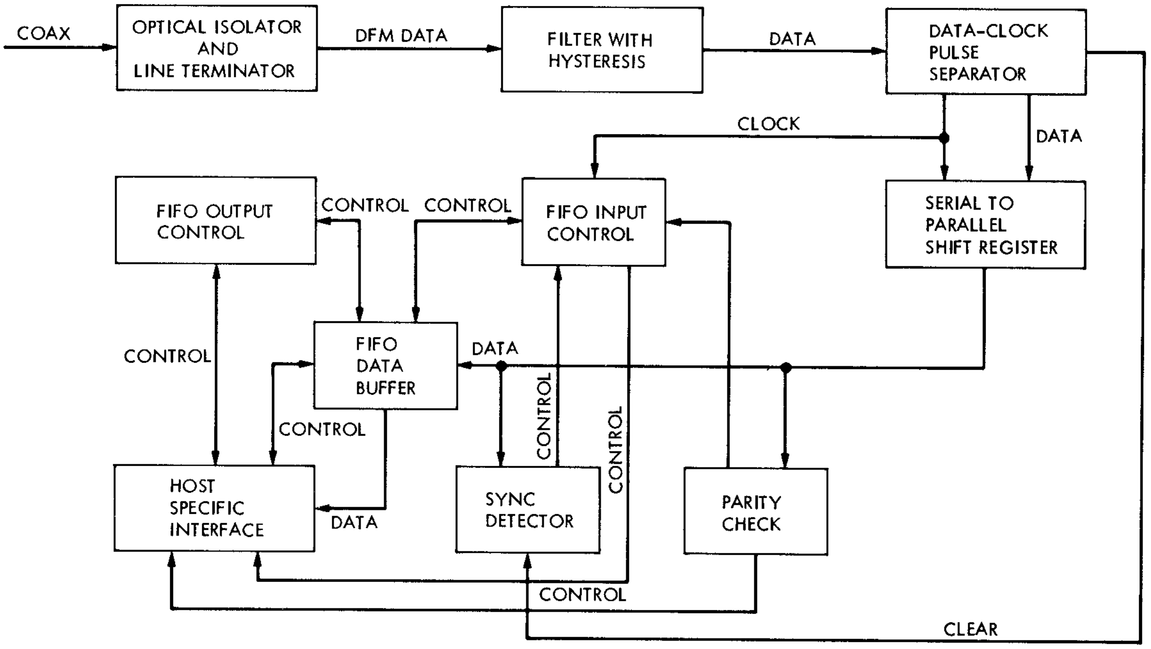

Fig. 4. Receiver module