# GCF HSD Error Control

C.–K. Hung

DSN Data Systems Section

*A selective repeat Automatic Repeat Request (ARQ) system has been implemented under software control in the GCF Error Detection and Correction (EDC) assembly at JPL and the Comm Monitor and Formatter (CMF) assembly at the DSSs. The CMF and EDC significantly improved real-time data quality and significantly reduced the post-pass time required for replay of blocks originally received in error. Since the Remote Mission Operation Centers (RMOCs) do not provide compatible error correction equipment, error correction will not be used on the RMOC-JPL HSD circuits. The real-time error correction capability will correct error burst or outage of two (2) loop-times or less for each DSS-JPL HSD circuit.*

## I. Introduction

The Ground Communications Facility (GCF) High Speed Data (HSD) Subsystem consists of the GCF Assemblies (Ref. 5) used to switch, transmit, record, process, distribute, test, and monitor digital data. The detailed functional capabilities of the GCF HSD subsystem for the Mark III period are illustrated in Fig. 1. The HSD circuits for interchange of data between the DSS/RMOC and JPL are impressed with serial bit streams at a continuous line bit rate of 7200 bits/sec in a 1200-bit block size. The blocks are either data blocks or filler blocks. Filler blocks are inserted when the user data load is insufficient to maintain contiguous data blocks on line.

A selective repeat Automatic Repeat Request (ARQ) system (Ref. 6, 9, 10, 11) in which only the particular block received in error is retransmitted has been implemented under software control in the GCF Error Detection and Correction (EDC) minicomputers at the Central Communications Termi-

nal (CCT) at JPL and the Comm Monitor and Formatter (CMF) minicomputers at the DSSs. (These minicomputers, a major portion of GCF High Speed Data subsystem, are shown in Fig. 2.) The CMF and EDC minicomputers, working together, significantly improved real-time data quality and significantly reduced the post-pass time required for replay of blocks originally received in error. The real-time error correction system corrects error burst or outage of two (2) loop-times[1] or less.

Error correction requires that both ends of the HSD line be equipped with error correction capabilities. Error correction will not be used on the RMOC-GCF CCT HSD circuits as the RMOCs do not provide compatible error correction equipment.

---

[1] A loop-time is a time between a block transmitted and the block acknowledgement received.

## II. GCF Error Control Algorithm

In describing the GCF Error Control Algorithm (Ref. 1, 2, 3, 4, 7, 8), only one direction of transmission/reception will be discussed. The reverse direction is identical though independent. A retransmission schematic diagram (Fig. 3) is given to aid in understanding the error control algorithm. The following buffers are needed for the retransmission scheme implemented:

(1) Acknowledgement Queue (A-Queue)

This queue is a first-in/first-out queue which contains data blocks that have been transmitted over the HSD line and are awaiting acknowledgement. As soon as an acknowledgement indicates that a block has been received error-free at the other end, that block is dropped from the A-Queue. Thus, at any time, no more than a loop-time of blocks are stored in the A-Queue (see Table 1, DSS-JPL Loop-Time blocks). The top-entry of the A-Queue is called the A-candidate. It is the next block to be acknowledged or to be retransmitted if the block is not positively acknowledged. For each acknowledgement received, the A-Queue pushes up thus creating the next A-candidate.

(2) Transmit Queue (T-Queue)

This is the data buffer which holds the incoming data blocks until they are called for transmission over the HSD line.

(3) Delivery Queue (D-Queue)

This queue stores all error-free HSD blocks received during retransmission until all prior blocks have been successfully retransmitted. The data blocks are delivered in order. When error correction is inhibited in the far-end, the data blocks are delivered in first-in/first-out sequence.

The error detection encoding and decoding under software control may use either a 22-bit or 33-bit error polynomial. Error correction works only with the 22-bit error code. Each block has two 8-bit fields reserved for GCF error correction use. One field (bits 9-16, word 73) contains the GCF serial number of the block. The other field (bits 1-8, word 74) contains the serial number of the just-received block which is being acknowledged as error-free. These two numbers are termed the GCF serial number and the GCF acknowledgement number respectively. Since the GCF serial number of a HSD block has 8 bits, GCF serial numbers are selected from the set: 0,1,2, - - - - - ,255. The term "in GCF sequence" means that a block is serialized in sequence with the previous transmission using the set: 1,2, - - - - - ,255,1,2, - - - - - ,255, - - - -. The zero value is skipped since it is used for filler blocks.

Data blocks transmitted in the error correction mode will carry the non-zero GCF serial numbers. Data blocks transmitted in the error correction inhibited mode will have no GCF serial number (i.e., zero). Whether or not a data block carries a GCF serial number depends on whether or not the transmit end is in error correction mode. Whether a data or filler block carries a GCF acknowledgement number depends on whether a data block with a non-zero GCF serial number was just received. Filler blocks normally will not be serialized but may carry acknowledgement numbers. Each data block that is not acknowledged (i.e., is in error) will be corrected up to N times (normally, N=2). No delay in data flow is introduced when the data string is error-free, but delay is introduced when error correction by retransmission occurs.

The GCF error control algorithm is incorporated into the receive and transmit functions of the CMF and EDC programs. The following is the logic of the error control algorithm.

### A. Receive Steps

(1) Accept a high speed data or filler block from HSD line. A normal sequence of interrupts occurs within the time of receipt of a block as predicted by the line rate (6 blocks/sec).

(2) Decode. A block may be received in error in two ways:

(a) Decoding error — Transfer of a complete block, but the 22-bit error polynomial does not correlate with the data in the block.

(b) Missing block — A normal sequence of interrupts does not occur within the time of receipt of a block as predicted by the line rate. The time slot (166.66 msec in 7.2K bits/sec line rate, 6 blocks/sec) corresponding to this missing block is treated the same as a block in error.

(3) Save GCF serial number and acknowledgement number.

(4) If near-end is in error correction mode, go to 5; otherwise skip to 6.

(5) If the acknowledgement number matches the A-candidate (in A-Queue) serial number (indicating that the block was received error-free at the distant end), then the A-candidate is deleted from the A-Queue and retransmission is not required. If the numbers do not match, retransmission is needed.

(6) If the far-end is in error correction mode and the block is received in error, then discard this block and go to 9; otherwise go to 7.[2]

(7) Test block type.

    (a) Discard filler block.

    (b) Data block with GCF serial number (non-zero) — consider far-end in error correction mode and deliver block to D-Queue for ordered delivery to user.

    (c) Data blocks without GCF serial numbers (zero) — consider error correction inhibited at far-end, deliver blocks to D-Queue for first-in/first-out delivery to user.

(8) Delivery to the user (D-Queue Management). The D-Queue is managed by a timer. This queue holds all received data blocks. After processing in the error correction mode (far-end), the blocks are delivered in GCF serial number sequence (the same order in which the blocks were originally transmitted). With error correction inhibited, the data is delivered in a first-in/first-out sequence.

(9) End of receive task.

## B. Transmit Steps

(1) If near-end is in error correction mode, go to 2; otherwise skip to 3.

(2) If retransmission is required (from receive task, step 5), the A-candidate is processed in the following way:

    (a) If the A-candidate is a data block (GCF serial number is non-zero) and if this A-candidate has been retransmitted N times, then delete the A-candidate and go to 3; otherwise, retransmit the A-candidate and go to 5.

    (b) If the A-candidate is a filler block (GCF serial number is zero), delete the A-candidate and go to 3.

(3) If the T-Queue is not empty, select the top-entry from T-Queue for transmission; otherwise select a filler block for transmission.

(4) If the near-end is in the error correction mode, insert a GCF serial number if a data block is being transmitted; otherwise, insert zeros in the serial number slots.

(5) Insert the serial number from the last received block (from receive task, step 3) as the GCF acknowledgement number.

(6) Encode in 22-bit error code.

(7) Transmit this block to HSD line and store this block in the A-Queue if near-end is in error correction mode.

(8) End of transmit task.

In the GCF error control algorithm, the transmit task is driven by the receive task. That is, each received block induces an output block containing its acknowledgement.

The GCF error control algorithm results in four (4) possible operational modes for each DSS-JPL HSD circuit:

(1) No error correction in either direction (DSS/RMOC ↔GCF CCT).

(2) Inbound error correction only (DSS→GCF CCT).

(3) Outbound error correction only (DSS←GCF CCT).

(4) Error correction both directions (DSS↔GCF CCT).

## III. GCF Error Control Implementation

The physical configuration and major components of the GCF HSD Subsystem in the Mark III Era is illustrated in Fig 2. The GCF error control algorithm has been implemented in the CMF and EDC software. Key aspects of the implementation are:

(1) The software has been designed and implemented in accordance with DSN software methodology standards (top-down implementation, structured programming principles, etc.).

(2) The implementation effort was organized into a work breakdown structure, which was then used to monitor progress.

(3) Initial inter-computer protocols (data flow) and timing analysis were completed very early in the software development.

(4) Software testing was accomplished in a hardware environment which closely matched that of the final operational configuration.

---

[2]In case of 7, either (1) far-end is in error correction inhibit mode, or (2) far-end is in error correction mode and the block is received error-free.

After the conclusion of acceptance tests of the DSS CMF in September 1977 and GCF CCT EDC and HSW software in November 1977, the GCF HSD subsystem for the Mark III period became operable and useable to support DSN missions. As of July 1978, all Voyager testing, ATRS recalls, and Manual DODR replay were used by the GCF HSD error correction capabilities. On September 15, 1978, Voyager commenced use of error correction on a routine basis.

The performance of the GCF HSD error control will be described in a subsequent issue of the DSN Progress Report.

# References

1. Adeyemi, O. H., "A New Feedback Protocol for the Ground Communications Facility" in the Deep Space Network Progress Report 42-28, pp. 49-56, Jet Propulsion Laboratory, Pasadena, California, December 15, 1976.

2. Adeyemi, O. H., "Error Control in GCF: An Information-Theoretic Model for Error Analysis and Coding", Technical Memorandum 33-699, Jet Propulsion Laboratory, Pasadena, California, October 15, 1974.

3. Adeyemi, O. H. and McEliece, R. J., "Forward Error Correction for the Ground Communications Facility?" in the Deep Space Network Progress Report 42-22, pp. 114-117, Jet Propulsion Laboratory, Pasadena, California, August 15, 1974.

4. Desens, R. B., "GCF Computer Note", unpublished data, Jet Propulsion Laboratory, Pasadena, California, January 28, 1976 (JPL internal document).

5. Evans, R. H., "DSN Ground Communications Facility" in the Deep Space Network Progress Report 42-43, pp. 9-17, Jet Propulsion Laboratory, Pasadena, California, November and December 1977.

6. Gatfield, A. G., "ARQ Error Control on the Satellite Channel" in Conf. Rec., Int. Conf. Comm., 1974, pp. 22B-1 − 22B-5.

7. McClure, J. P., "Basic Algorithm for Retransmission Error Correction", Interoffice Memorandum, October 1972 (JPL internal document).

8. McClure, J. P., "High Speed Data Outage Distribution" in JPL Technical Report 32-1526, Volume XIX.

9. Sastry, A. R. K., "Improving Automatic Repeat − Request (ARQ) Performance on Satellite Channels under High Error Rate Conditions", I.E.E.E. Transactions on Communications, April 1975.

10. Sastry, A. R. K., "Performance of Hybrid Error control Schemes on Satellite Channels", I.E.E.E. Transactions on Communications, Volume Com-23, No. 7, July 1975.

11. Sindhu, Pradecp S., "Retransmission Error Control with Memory", I.E.E.E. Transactions on Communications, Volume Com-25, No. 5, May 1977.

**Table 1. DSS-JPL loop time blocks**

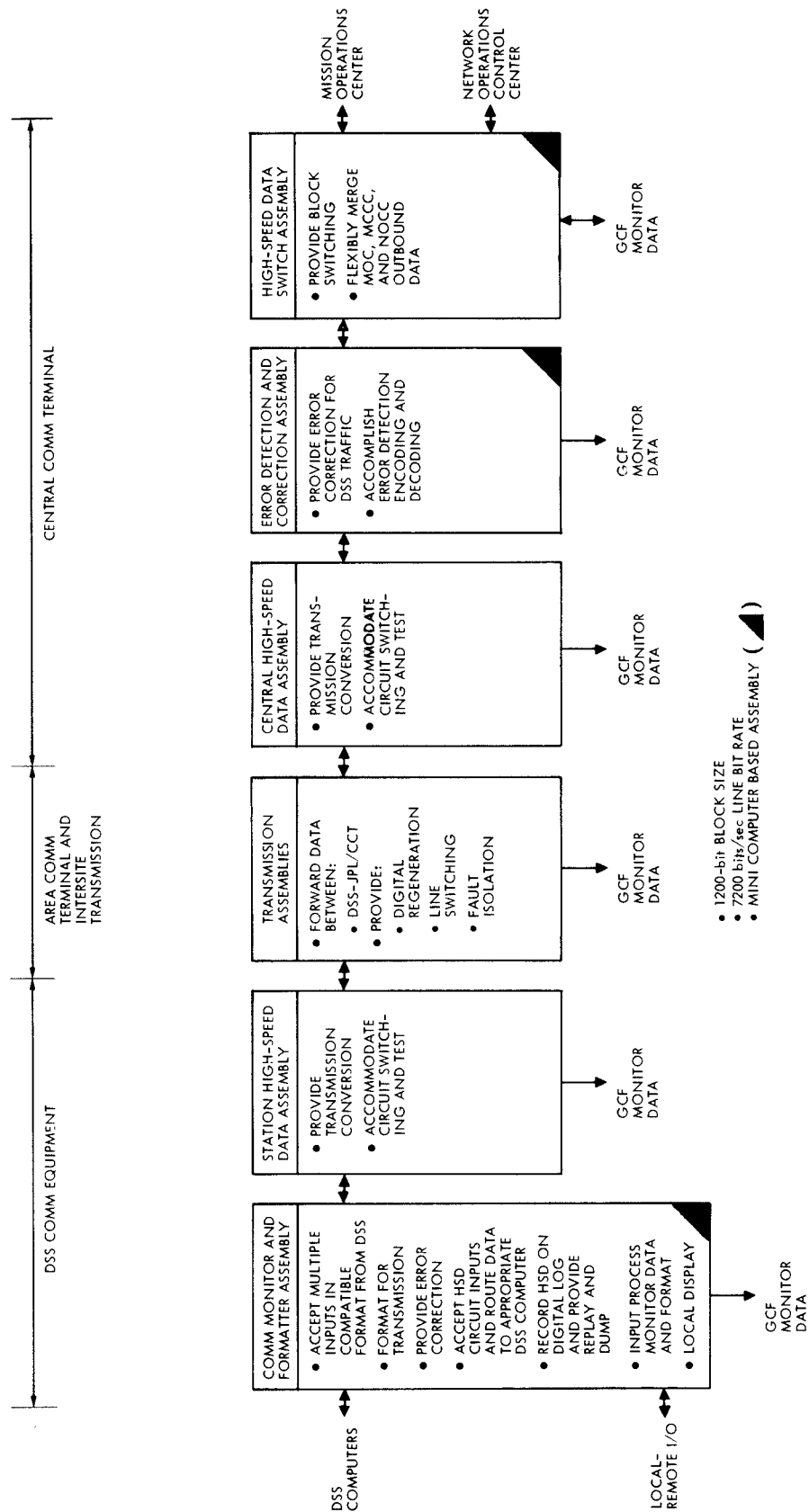| DSS-JPL | Loop-time blocks |
|---------|------------------|
| DSS44-JPL | 10 |
| DSS62-JPL | 13 |
| DSS63-JPL | 13 |
| DSS42-JPL | 11 |
| DSS43-JPL | 11 |
| DSS14-JPL | 8 |

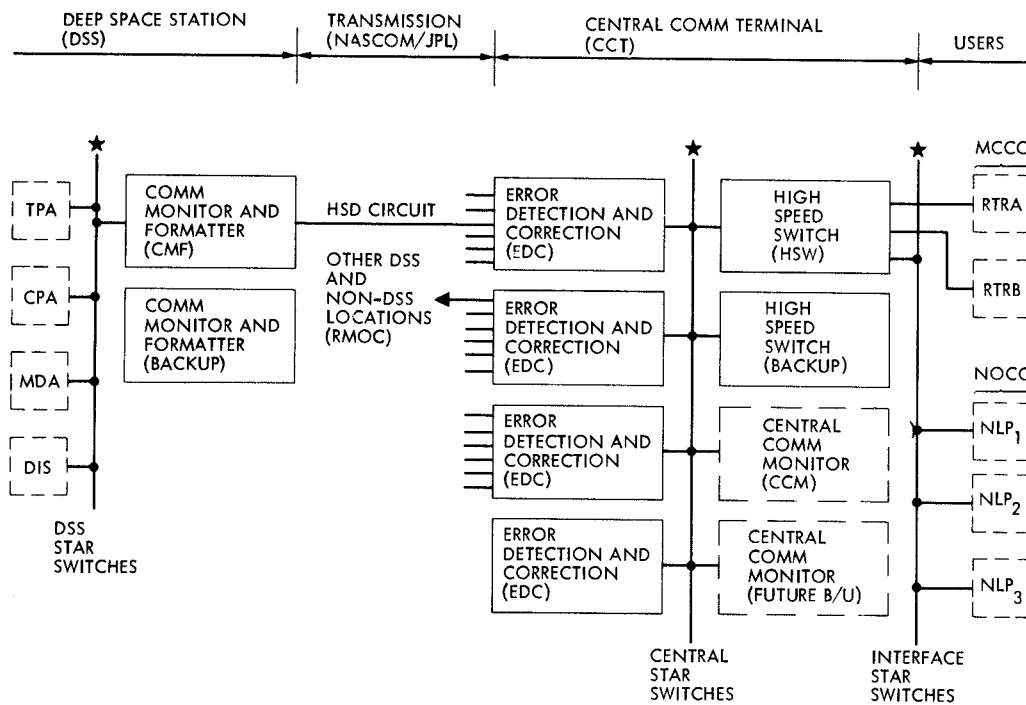**Fig. 1. GCF high-speed data subsystem functional capabilities**
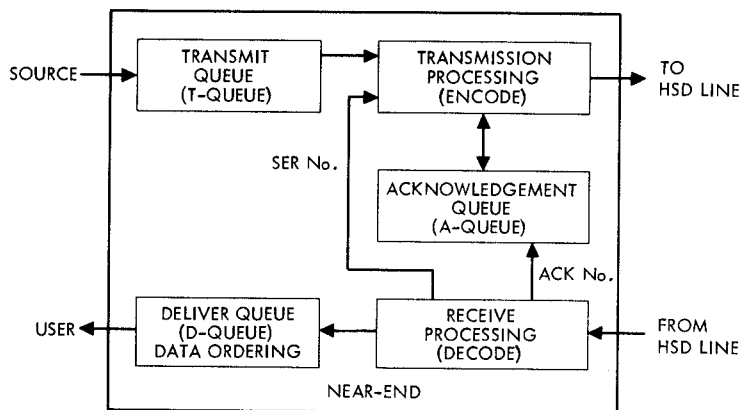
**Fig. 2. Mark III-77 high-speed data subsystem configuration**



**Fig. 3. Retransmission schematic diagram**