Dual A/D Converter With Automatic DMA Block-Transfer Capability

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A PDP-11 computer-controlled UNIBUS analog-to-digital (A/D) converter has been designed and constructed for use in the DSN Planetary Radar Data Acquisition System. The converter is intended for synchronous quadrature-pair sampling and can be programmed to automatically transmit the sample values via direct memory access (DMA) to any desired blocks of memory locations. The article describes the converter in detail, and gives information on mechanical construction, data-transfer rates, self-test and calibration provisions, and programming.

I. Introduction

A PDP-11[1] computer-controlled UNIBUS analog-to-digital (A/D) converter has been designed and constructed for use in the DSN Planetary Radar Data Acquisition System at DSS 14. Immediate applications of the A/D converter will be in the measurement of CW total reflected spectra from celestial bodies such as Venus, Ganymede, Callisto, and various asteroids. The converter fills a need in gathering measurements for the computation of high-resolution spectra (FFTs of more than 512 points) in the bandwidth range 5-350 kHz.

Prior to the availability of this A/D converter, variable-clock A/D conversion could only be done using the multiplexed A/D converter of the SDS 930 computer. Quadrature-pair sampling with the 930's A/D converter is not simultaneous and is limited to about 5 kHz bandwidth. Faster sampling can be done by the 512-channel correlator, but this limits the spectral resolution to 512 points. The available CSPI Spectrum Analyzer (Array Processor) at DSS 14 can compute spectra to 8K points, but requires a direct memory access (DMA) source of quadrature-pair samples having both adequate speed and the ability to load alternate banks (or blocks) of memory locations in order to obtain continuous spectrum computation. The new A/D converter meets these requirements in a very general way, and can work with types of processing equipment other than the CSPI Spectrum Analyzer.

The A/D converters commonly available on the market generally lack three design features deemed essential for planetary radar data-taking:

(1) DMA block transfers of arbitrary length to arbitrary memory locations, with bank-switching to load data

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alternately to two different banks of memory locations.

(2) Simultaneous quadrature-pair sampling with minimal skew (order of 10 nanoseconds) using video-type high-speed sampling technology, and with sampling controlled by a variable-frequency external source.

(3) Self-test and diagnosis provisions for computer-controlled testing.

It was, therefore, decided to design an A/D converter having the required features, and incorporating design concepts based on needs which have been identified over many years of experience in planetary radar data-taking. This new design is based on an existing type of video A/D converter module, which was then embedded into an appropriate mechanical package and DMA computer interface having the requisite data transfer and self-test functions.

II. Description of Equipment

A. General Description

The equipment (the "box") is a computer-controlled (PDP-11) dual A/D converter of 8-bit resolution. The two A/D converters are Computer Labs MATV-11 video types with 50-ohm inputs, ±2.5-volt input range, and 2's complement encoding. Sampling can be commanded directly by the computer program, using data-input instructions, and also the sampling can be controlled by an "external clock" input. When the external clock is enabled, the box will sample automatically, and will transfer the samples automatically to blocks of memory locations specified by the program. The box may be commanded to produce program interrupts at end-of-block. The box also provides for computer-controlled self-test. The logical complexity of the box is 105 integrated circuit packages plus three component headers. Mechanically, the box is an 3-1/2 in. (8.89 cm) rack-mounted drawer with internal forced-air blowers. Due to thick shielding plates, the box weighs approximately 36 kg (80 lb). The box is designed to be electromagnetically and thermally compatible with most Deep Space Station rack-mounted equipment installations. Figures 1 through 5 present photographs of the equipment.

B. Data Transfer Rates

Data transfer rates are dependent on whether the computer and/or other peripherals are competing for data-bus usage. With other peripherals off, and with the PDP-11 computer in its WAIT state, the box can transfer pairs of 16-bit numbers at a pair-rate (or "bandwidth") of 270,000 pairs per second (540,000 words per second). These rates were observed with a PDP-11 having a relatively slow type of core memory.

The internal timing of the box has been designed to transfer at the theoretical maximum rate for NPR "DATO" transfers, 2.4 million words per second (into zero-delay memory, of course), but the timing is currently set about 5 percent slower. The operational scenario for which the box was designed, however, envisioned somewhat slower transfer clocking. For this reason, the box responds to the external clock by NPR (request), waiting for the computer's NPG (grant), doing one or two word transfers, and then dropping BBSY. Thus, the box is not designed to capture the data bus during an entire block transfer, and, therefore, cannot actually transmit at the theoretical maximum rate.

C. Self-Test Provisions

The box is designed for computer-programmed self-test. The self-test features include:

(1) Direct write-read tests of writable registers MARPA, PTC, MARPB and also the control bits CS 0, 1, 2, 3, 4, 6, 7.

(2) Indirect write-read tests of MAR and TC, by setting CS 7 (SOFTINIT) and writing, respectively, to MARPB and PTC. The result is that the contents of MARPB and PTC can be read, respectively, from MAR and TC.

(3) Verification of the hardwired interrupt vector (0170) by reading IVAD. Note: Because of other test provisions (see 4, below), either CS0 must have previously been cleared or both CS1 and CS2 must have previously been cleared, to prevent spurious NPR transfers from being triggered during testing.

(4) Simulation of the "external clock," made available by having the program input ("move") data from IVAD, preferably using an available general register in the computer as the destination, for maximum speed. Output "moves" should not be used, due to artifacts of the computer. This simulated external clock is equivalent to an actual clock, and will produce NPR data transfers under the same rules as for the external clock (i.e., the GO conditions must be met).

D. Calibration Provisions

The calibration potentiometers of the two MATV-11 video A/D converters are accessible from the rear of the box, and may be adjusted without opening the box. Calibration is conducted by connecting a precision voltage source to one of the A/D converter coaxial input jacks, and reading the converter under program control. In calibration, the potentiometers are adjusted to produce "flutter" in certain bit-combinations for various input voltages. The flutter statistics may, of course, be displayed by an appropriate computer program.

E. Sampling Control

The two A/D converters can be caused to sample under the following stimuli:

(1) *Input from Device Addresses* 00, 04, and 20 which produce, respectively, the "real," "quadrature," and "both" samples. Under input, the box uses asynchronous technique to delay SSYN response until the requested conversion is complete.

(2) *Input or Output to Device Address* 14, when "GO" conditions are met. This action simulates an external clock and causes the automatic block transfer logic to trigger new A/D samples and to transmit them.

(3) *External Clocks.* A TTL gate input (with 4.7K pullup to +5 volts) and an analog clock input are provided. The TTL gate input triggers the automatic block transfer logic on the fall of the input. This input should be left open-circuited when not in use. The analog clock input is 50 ohms (nominal) and is shunt zener protected. The analog signal is normally a zero-bias sinusoid obtained from a variable-frequency synthesizer, whose output is +13 dBm in 50 ohms (3 volts peak-peak). The analog signal is compared to zero by a μA 710 comparator, and the 710's TTL-compatible output triggers the automatic block transfer logic on the negative-going zero-crossing of the sinusoid. The 710 is wired with output-to-input positive feedback that induces a Schmitt-trigger type of action: When the analog signal crosses the trigger threshold (voltage), the 710 begins to change its output state. Feedback of this output state causes the threshold to move approximately 55 millivolts in that direction which enhances the change of state which was initiated by the threshold crossing. An unsymmetrical pair of thresholds are used: the threshold for the negative-going analog input is -5 millivolts which, considering the intrinsic 5 millivolt uncertainty of the 710, does not significantly affect the 710's ability to detect the negative-going zero-crossing. The threshold for the positive-going signal is, however, +50 millivolts, but with the same hysteresis characteristic.

III. Programming

A. Block Transfer Description

The box, when under control of the "external" (or simulated) clock, does real, quadrature, or real-quadrature pair sampling, and then transfers one or both conversion results (as numbers) to any desired block of contiguous addresses in the computer's memory system. On each external clock transition, the number of conversion words to be transferred (one or two) is determined by the number of A/D converters enabled (CS1, CS2 in the control-status register). The number of word or word-pair transfers is controlled by the contents of PTC, which holds the twos complement of the number of such transfers that are to be accomplished. A block can consist of from 1 to 32,768-word or word-pair transfers. The addresses of the memory locations to which transfers will be made are specified by either of two base-address "preset" registers, MARPA and MARPB, and a moving address register, MAR, which increments from a preset value contained in either MARPA or MARPB. The MARPB preset address is used by default, but the box can be commanded to "cycle" two or more block transfers in which MARPB and MARPA are used, *alternately*, as base-address initialization. This cycling capability is used to load data into array-processing equipment such that while one block is being loaded by the box, the other block is being processed and vice versa.

B. Block Transfer Control Under CS Bits 1, 2

CS Bit 1 enables the "quadrature" sampler hardware, and CS Bit 2 enables the "real" sampler hardware. The sequencing recognizes three cases of this pair of bits:

(1) *None Enabled.* The box holds, same as GO released state.

(2) *Either Enabled, But Not Both.* Whichever of the two samplers is enabled furnishes the word to be transferred. After the transfer, MAR (the "word" storage address) and TC increment. If TC has been in the carry state (TC = 0177777) during the transfer, then both MAR and TC will receive preset values as soon as the transfer is complete.

(3) *Both Enabled.* The real sample is transferred first, and then MAR is incremented. Then, the quadrature sample is transferred, and then both MAR and TC increment. Thus, TC increments after a *quadrature-pair* has been transmitted. If the TC has been in the carry state during the transfer of the quadrature sample, then both MAR and TC will receive preset values as soon as the transfer is complete.

C. Master Enabling (GO)

The box will do conversions under NPR and (if enabled) interrupts under BR, only when the following conditions (the "GO" conditions) all appear in the CS register:

Bit 7 (Software-Controlled Initialization) released

Bit 0 (GO) set

Bit 1 or Bit 2 (Conversion Select/Enable) set

Otherwise, the box holds its position in its internal sequencing logic, and will "resume where it left off" when the running conditions are met. When the box is running NPR, it is possible that the box, as master, could address nonexistent storage. This error situation cannot be detected by the program, because the box has no NPR timeout to permit the CPU to reacquire the bus to command the box to hold (drop Bit 0, or drop both Bits 1 and 2) or to initialize (assert Bit 7), even though such control is available. NPR hang can, however, always be cleared by asserting bus INIT, which forces Bit 0 off (no-go), and cancels all NPR or BR activities. When the program succeeds in commanding no-go, the effect on the sequencing logic is benign, because the box cannot be bus master at such a time.

D. Interrupt Logic

The box can interrupt after the last data-word transmission of a block (as determined by TC = carry state), provided the interrupt is enabled (Bit 6 a "one"), with the box otherwise in the running state. The interrupt guarantees that the entire block transmission is complete, and does not preclude further sampling and NPR transmissions while the interrupt is being processed by the program.

E. Data Sampling Synchronization

When "GO" conditions are all met, the next (subsequent) pulse from the external clock governs the actual sample time. The leading, negative going edge of the external clock produces the start-convert (ENCODE) command to the A/D hardware.

F. Programmer's Reference Guide

The Appendix gives a programmer's reference guide to the control and status registers of the A/D converter. The reference guide, prepared in the condensed form preferred by programmers, identifies the registers by name and low address bits, and gives descriptions of register and control bit functions.

Appendix

Programmer's Reference Guide

Real (Inphase) Sample Output

	15							8	7							0	Low ADRS
RSAM																	8
																	00

The 8-bit A/D converter output is in the low byte. Bit 7 (sign) is extended to the high byte. The real sample is updated synchronously to an external clock when the box is in NPR mode, and is also updated asynchronously on any read of RSAM or PSAM, and the updated result is what will be read.

Memory Starting Address Preset "A"

	15														1	0	Low ADRS
MARPA																x	8
																	02

This read-write register contains the bus address, which will be used in the cycling mode, to preset MAR to the starting address for a new block transfer, whenever MARPB was used as the starting address for the previous block transfer. The preset occurs at end-of-block when the box is set to cycle (Bit 4 of CS). Bit 0 of MARPA is read-only, and will always be read as a zero. Thus, the field of Bits 15-1 is the word address to be used.

Quadrature (Imaginary, or 90-Degree Phase) Sample Output

	15							8	7							0	Low ADRS
QSAM																	8
																	04

The 8-bit A/D converter output is in the low byte. Bit 7 (sign) is extended to the high byte. The quadrature sample is updated synchronously to an external clock when the box is in NPR master mode, and is also updated asynchronously on any read of QSAM or PSAM, and the updated result is what will be read. This register is read-only.

Memory Address for Next Word-Transfer

	15														1	0	Low ADRS
MAR																x	8
																	06

The bus word address to which the next word-transfer will be directed is right-justified in the field Bits 15-1. This moving address is a register which is preset from a 2:1 multiplexer which selects either of the preset registers, MARPA, MARPB, in accordance with which of these is to be used by sequencing logic for the next block transfer. This register is read-only.

Transfer Count

	15 … 0	Low ADRS + 8
TC		10

This read-only register is automatically initialized (from PTC) to the two's complement of the number of transfers comprising the data block. The words being transferred and counted are those enabled by Bits 1-2 of the control status register CS. When both samplers are enabled, the real sample is transmitted first, and then the quadrature sample is transmitted, and the TC is incremented. After TC has been used at the carry state (Bits 15-0 all 1 on the last word of a block), it is automatically preset to the actual number contained in the register designated as PTC. The preset from PTC occurs on initialization (Bit 7 of CS) on every DATO to the block of addresses assigned to the box, provided CS 7 is set or being set on the leading edge of the DATO. If PTC is being written by the DATO, then the new value being written will appear (CS 7 permitting) at the trailing edge of the DATO.

Preset Value For Transfer Count

	15 … 0	Low ADRS + 8
PTC		12

This read-write register is loaded by the program with the two's complement of the number of 1- or 2-word transfers comprising the data block. The contents of PTC are automatically loaded into TC on initialization (setting Bit 7 of CS to 1), and at the end of the data block if the cycling mode of continuous block transfer is selected by having Bit 6 of CS previously set. PTC assumes the value transmitted to it by the CPU on the leading edge of the transmission.

Interrupt Vector Address

	15 … 0	Low ADRS + 8
IVAD		14

This hardwired, read-only output is used by the program to verify the word location to which program control will be transferred when there is an interrupt from the box.

Control-Status Register

	7 6 5 4 3 2 1 0	Low ADRS + 8
CS		16

Bits 7, 6, 4, 3, 2, 1, 0 are read-write. Bit 5 is read-only.

Bit 7 – A "one" is set by the program to initialize the sequencing logic in the box, and to load PTC to TC, and MARPB to MAR. Any current NPR/BR activities are aborted "in a benign way." *Note:* The only other initialization available in the box is obtained by asserting unified-bus INIT, which aborts NPR/BR (abnormally, if these were active) and drops Bit 0 (placing the box in hold), guaranteeing a benign state for all drivers.

Bit 6 – A "one" will enable the interrupt at the end of each data-block transfer. The bit is tested internally only when the logic is in the end-of-block state.

Bit 5 – This read-only bit is a "one" when the box is using memory addresses initialized from MARPB, and can become a "zero" only in the cycling mode, when the box switches to the MARPA preset register. The "one" indicates that the use of the address sequence starting from MARPB is not finished, and the "zero" indicates similarly for the MARPA address sequence.

Bit 4 – The program sets this bit to "one" to enable the external analog clock (3 volt peak-peak) input to control the sampler timing. This control was provided so that the external analog clock jack can be left open-circuited while testing is in progress.

Bit 3 – A "one" will enable continuous cycling of the data block transmission, and causes presets of PTC to TC and MARPA or MARPB to MAR. MARPB is used if MAR was running from the MARPA value, and vice versa.

Bit 2 – A "one" will enable the "REAL" sampler for automatic sampling synchronously to subsequent external clock pulses occurring after release of Bit 7 (initialization) and assertion of Bit 0 (GO).

Bit 1 – A "one" will enable the "QUAD" sampler for automatic sampling, synchronously to subsequent external clock pulses (see description for Bit 2). Quadrature samples are obtained simultaneously with real samples when both quadrature and reals are enabled.

Bit 0 – A "one" will enable the box's automatic NPR (and INTR, if enabled) sequencing when conditions on Bit 7, 2, and 1 are also met. A "zero" will cause the box to suspend operations, subject to resuming the sequencing at a later time, without loss of sequencing information or other control information. Bit 0 is cleared by unified-bus INIT, and automatically after the last word or word-pair transmission of a block, if cycling has not been enabled. When Bit 0 is commanded from set to clear, any sampling operation currently in progress will have been completed.

Note: The setting of Bit 0 to "one" cannot actually produce NPR sequencing unless Bit 7 was previously commanded to "zero," i.e., simultaneous clearing of Bit 7 and setting of Bit 0 will not produce "GO" conditions.

Packed Quadrature and Real Sample

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Low ADRS
PSAM																	8
																	20

This read-only register contains both the real and quadrature sample bytes packed into one 16-bit word. The left (high-order) byte contains the 8-bit 2's complement quadrature sample and the right (low order) byte contains the 8-bit, 2's complement real sample. Both samples are updated whenever the program reads PSAM, and it is guaranteed that both of the byte samples will be read as the updated samples. Packed samples are not transmitted in NPR master mode.

Memory Starting Address Preset "B"

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MARPB																x

Low ADRS
8
22

(Note: Addresses 24-77 are available for other use)

This read-write register contains the bus address which is used for initialization of the MAR to the starting address for the first block transfer, and alternately with MARPA thereafter if the box is in the cycling mode. MARPB is loaded to MAR on initialization (Bit 7 of CS) on every DATO to the block of addresses assigned to the box, provided CS7 is set or being set on the leading edge of the DATO. If MARPB is being written by the DATO, then the new value being written will appear in MAR (CS7 permitting) at the trailing edge of the DATO. If the box is in the cycling mode (Bit 4 of CS), then MARPB will be used at end-of-block to preset MAR after any block in which MARPA was previously used as the preset. Bit 0 of MARPB is read-only, and will always be read as a zero. Thus, the field of Bits 15-1 is the word address to be used.

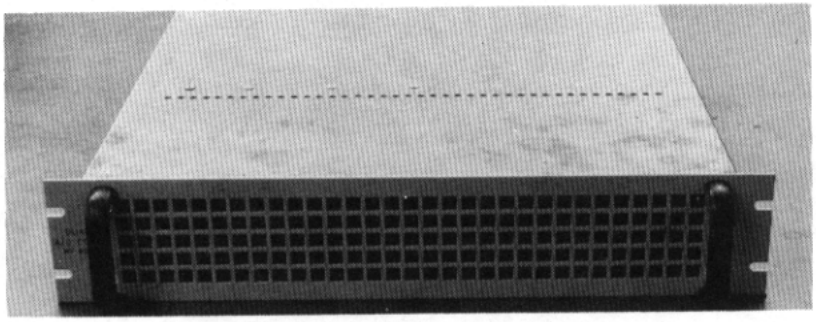

Fig. 1. Front view, showing 19 by 3-½ in. (48.26 by 8.89 cm) shielding grille and 5-volt power indicator LED

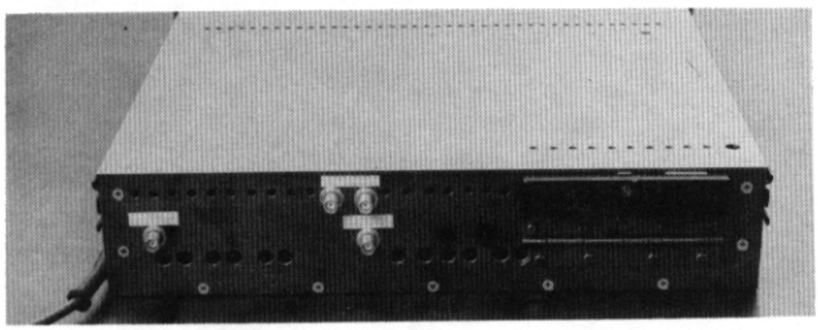

Fig. 2. Rear view, showing real and quadrature signal inputs, TTL and analog external clock inputs, UNIBUS connector, and converter module calibration access holes (at bottom)

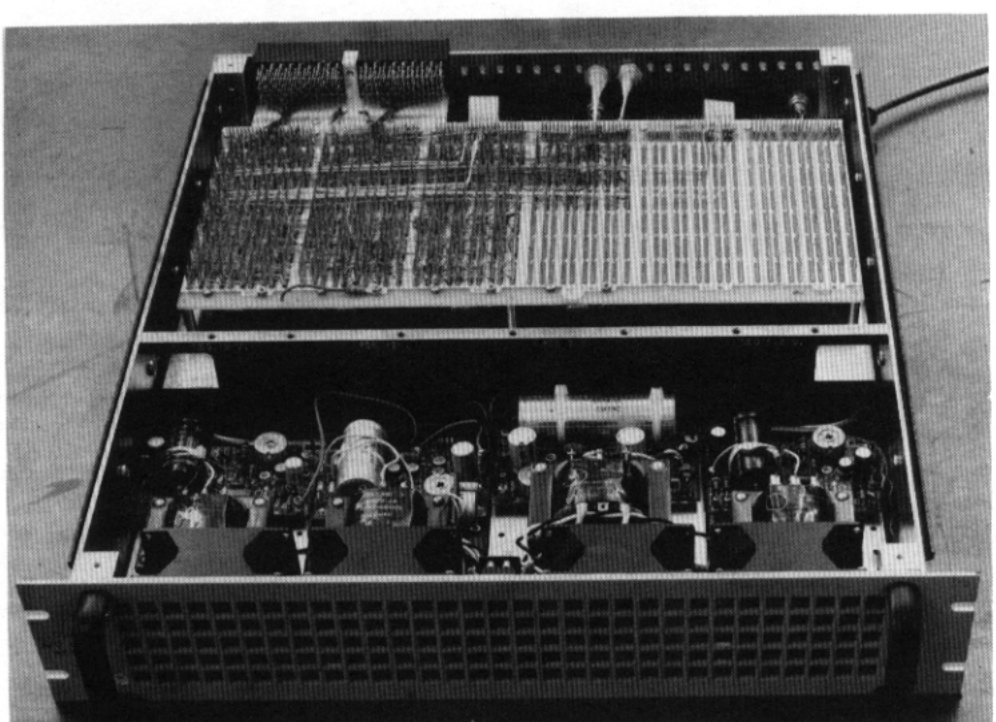

Fig. 3. Top cover removed for logic probing, showing power supplies and power-supply shield used as airflow divider

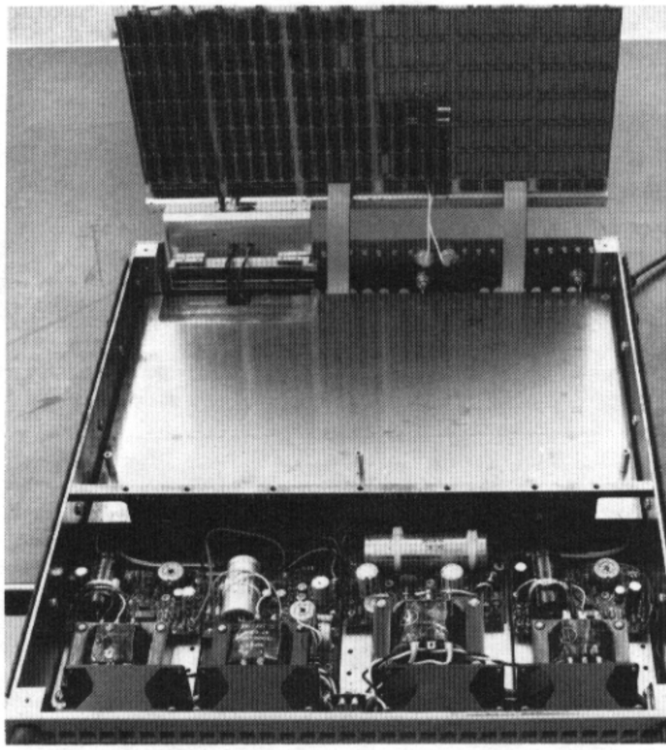

Fig. 4. Logic board folded upward on hinge for IC replacement, showing horizontal shield between logic circuits and A/D module compartment below; shield plate is also an air divider between compartments

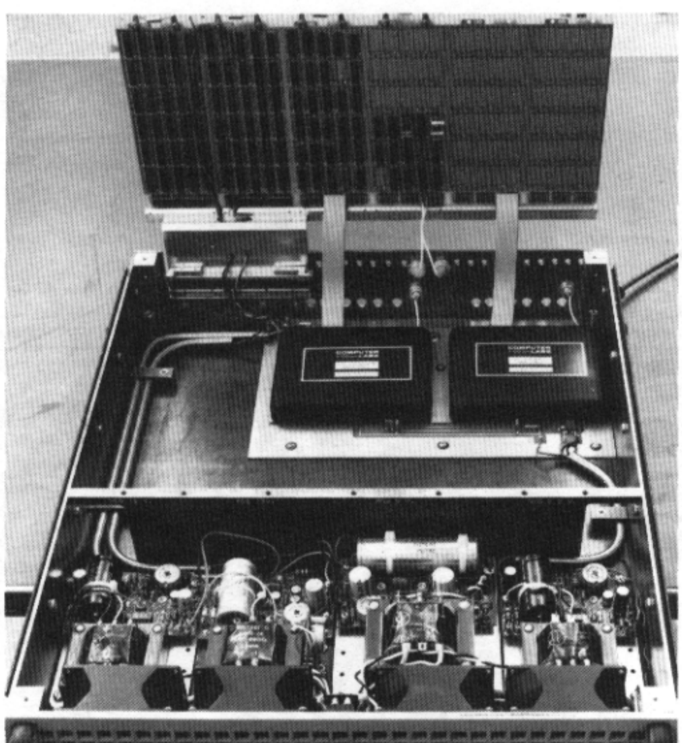

Fig. 5. Horizontal shield plate removed, revealing A/D converter modules on PC board