Progress Report on the Block I VLBI Correlator Implementation

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This article is a status report and final design summary for the DSN Block I VLBI Processor Subsystem.

I. Introduction

The DSN is currently in the process of implementing a very long baseline interferometry (VLBI) system for the determination of station clock-sync parameters, UT1 and polar motion, and station platform parameters and for use in spacecraft tracking. This article is directed toward what is referred to as the Block I VLBI Processor Subsystem (VPS) portion of this implementation effort. *DSN Progress Report 42-50*, page 226, presents a discussion of the correlator overall design and hardware detailed design, while here we are giving the current status of the VPS implementation and some of its key characteristics.

The Block I VPS performs three basic functions: it receives the 500-kbit/sec video data over the GCF wideband data lines from each of the three DSN 64-m antennas; it cross-correlates data; and finally, it performs several postcorrelation data reduction operations on the correlated data including calibration, editing and parameter estimation. The VPS hardware consists of a Digital Equipment Corp. (DEC) VAX 11/780 computer and the special purpose correlator hardware designed and built by the DSN and attached to the VAX computer via high-speed DMA interfaces. The VPS software consists of a real-time interrupt driven program which resides in the VAX computer and controls the cross-correlation process, and of five non-real-time but interactive routines which also reside in the VAX computer and perform the postcorrelation functions.

II. Hardware

The communications hardware (Fig. 1) for tying the VPS to the GCF wideband data line has been installed and is currently undergoing tests. This equipment consists of 56 K-band modems and computer interfaces which will permit data to be transferred directly to the VPS from two DSN stations simultaneously for near-real-time data correlation.

The design and construction of the special purpose cross-correlation hardware has been completed. Validation tests have been performed module by module and also as a system. The hardware is presently being used together with the correlation software to process some preliminary VLBI video data. Results of these tests indicate that the system is

performing well. In its final configuration this hardware consists of six DSN standard subchassis including two Phase Processors, one Buffer/Mixer, one Cross-Correlator, one Correlator Processor, and one I/O Controller.

The Phase Processors, one for each video-data input stream, contain 32-bit microprocessors made up from AMC 2900 bit-slice chips. They perform the phase and phase-calibration linear updates every bit-time and the quadradic model updates every 5000 bit-times.

The Buffer/Mixer contains the delay line, the phase mixers, and the phase-calibration tone tracking for both data streams. The delay line, which is implemented using eight 16k dynamic RAMS, is 100k bits in length. The 3-level phase mixers, implemented in PROMS, has its output accumulated on the Cross-Correlation board. The phase-calibration tone trackers consist of 256-level mixers, 1k X 8 PROMS, and 32 bit accumulation for both sine and cosine.

The Cross-Correlator computes the cross-product sums using a 3-level by 3-level complex multiplication for 16 lags, and then accumulates the 32 results at the bit rate. Every 5000 bit-times this accumulated data is sent to the Correlator Processor for further processing.

The Correlator Processor performs a fast Fourier transform (FFT) and a fractional-bit-shift correction on the cross-correlated data. The FFT process results in series of 32 values representing the real and imaginary part of the input data cross-correlated at 16 lag points. These 32 values are then multiplied by a predetermined twiddle-factor to provide the fractional-bit-shift correction. The values are then accumulated for later transfer to the controlling computer.

The I/O Controller performs all information transfer between the correlation hardware and the controlling computer, except for the video data which is transferred through the Buffer/Mixer.

Each board has built-in self-test capabilities, some of which are performed at startup, some continuously, and some under computer control. All self-test status is available to the controlling computer.

III. Software

The RECEIVE program for receiving the VLBI video data over the wide-band data lines has been designed, coded and tested using IDR tapes as the source of input. The VAX system I/O driver for operating the wide-band line hardware interface to the computer has been written but not fully tested. Once this is completed, the video data can then be sent from each of the DSN 64-m antennas directly to the VPS, where it will be reformatted into records appropriate for the correlation process.

The MAKESCN program for converting the ancillary data into a correlation control record has been completed and tested (Fig. 2). The ancillary contains all the source scan information, recorder start-stop times, observing frequencies, weather data, etc., and is sent to the VPS over the wideband data lines in front of the video data. MAKESCN determines how this data is edited, merged together with similar data from both DSN stations and used to form the scan blocks for running the correlation process.

The CORLATE program for controlling the correlation process is completed and presently undergoing system tests with the correlator hardware. This routine is in the form of an interrupt handler. It reads the VLBI data and meters it time-synchronously to the correlator hardware. It calculates the geometric model parameters needed to perform proper correlation of the data and sends these to the hardware. It also outputs these model parameters, together with the correlation coefficients, to the postcorrelation record. Finally, it displays various status information and samples of the correlated data to the operator. All of these functions are normally performed under control of the Processor Control Record produced by MAKESCN, but with operator override capability.

The post-correlation software has been running in an RD mode for several years on the IBM 370 computer on the Caltech campus. This software consists of FORTRAN programs running in batch mode. These programs are to be converted to structured FORTRAN and made to run on the VPS VAX 11/780 computer. This conversion process is nearly complete at the present time.

In addition, the postcorrelation routines are to be restructured where necessary so that they can be run in an automatic mode under control of a control-record similar to that in the correlation process. Some of the routines will also be made to run interactively, with capability for operator intervention. This part of the implementation is still in the development stage and will not be complete until July 1981.

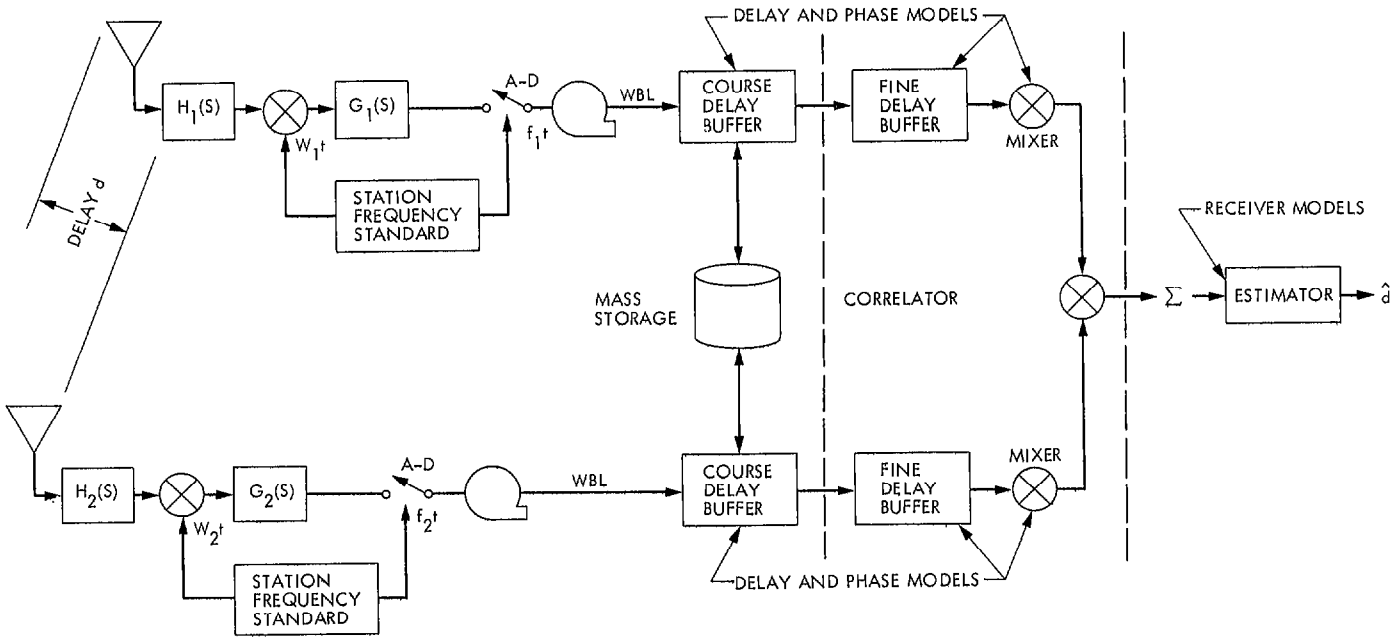

Fig. 1. VLBI data acquisition and processing (simplified)

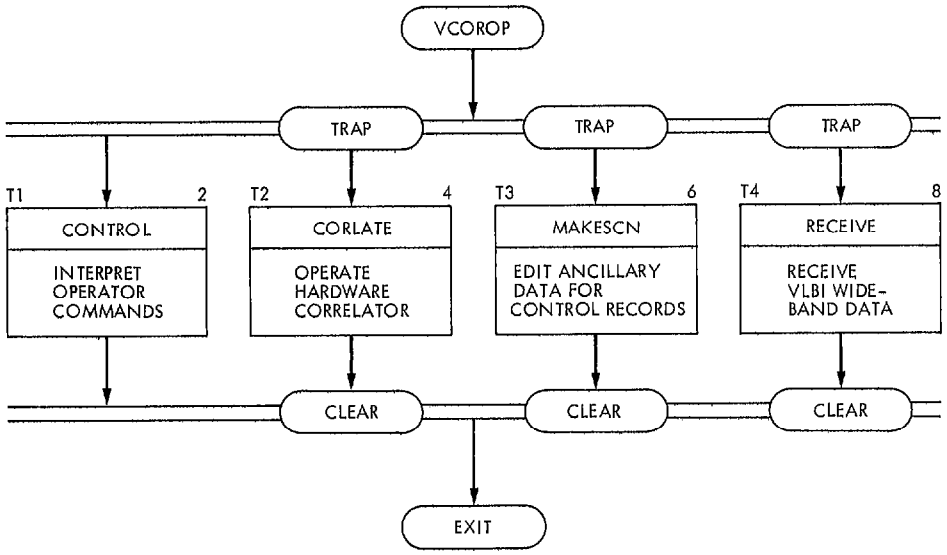

Fig. 2. Block I VLBI correlator software