Input Signal Conditioner for the Multimegasymbol Telemetry System Feasibility Model

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Described in this article is the input signal conditioner portion of the Multimegasymbol Telemetry Demodulator and Detector Feasibility Model (MTDD-F). The input signal conditioner accepts the 55-MHz wideband IF signal of a Block IV DSN receiver and provides selectable bandpass filtering, total power automatic gain control (AGC), and frequency translation providing inphase and quadrature (I&Q) outputs at baseband.

I. Introduction

Future spacecraft carrying synthetic aperture radars (SAR's) will require telemetry systems capable of much higher symbol rates than can currently be supported in the Deep Space Network (DSN). Radar return signals received by a SAR-equipped spacecraft may be digitized and retransmitted to earth in real-time, with little or no data compression performed onboard the spacecraft. Current technology, coupled with spacecraft size, weight and power constraints, discourages onboard processing of the radar signals. As a consequence, the high rate data must be relayed to earth to be recorded and processed, producing radar reflectivity maps of the planetary surface.

In the mid-1980's the Venus Orbiting Imaging Radar (VOIR) spacecraft will carry a SAR into a Venusian orbit where it will probe through heavy clouds and gather radar information necessary to produce high-resolution radar images. This mission will require a telemetry system capable of symbol rates of several megasymbols per second (msps). Currently the highest symbol rate which the DSN can support is about 250 kilosymbols per second (ksps).

A Multimegasymbol Telemetry Demodulator and Detector-Feasibility Model (MTDD-F) is currently being developed at JPL which will be capable of demodulating and detecting telemetry streams having symbol rates of 125 ksps to 30 msps. The input signal conditioner portion of this equipment has been completed and is the subject of this article.

II. System Hardware

Figure 1 is a block diagram of the MTDD-F. Of the five elements shown, only the input signal conditioner will be discussed in this article. Other parts of the MTDD-F will be described in subsequent articles.

Figure 2 is a detailed block diagram of the input signal conditioner. Provided in the input signal conditioner is a set of IF band pass filters, an AGC loop and a complex mixer. The input signal conditioner receives its input from a wideband 55-MHz IF output port of a Block IV receiver. Inphase and quadrature baseband output signals are generated and supplied to the high-speed front end section of the MTDD-F.

A. Input Filter Module

The input filter module contains a set of five selectable 55-MHz bandpass filters which limit the receiver IF bandwidth for symbol rates in the range of 125 ksps to 4 msps. Another filter select position consists of a straight-through connection which is used when the telemetry symbol rate lies between 4 and 30 msps. In this wideband mode, system bandwidth is limited by the maser bandwidth (approximately 60 MHz two sided at -1 dB) and by the 5-pole, 40-MHz, Butterworth low-pass arm filters in the complex mixer.

Filter selection is accomplished with a pair of six-position coaxial RF relays which are controlled by a three-line TTL interface.

The bandwidths of these five filters vary in steps of one octave and are listed in Table 1 with their respective symbol rates. All of these filters are three-section Butterworth designs. Filters 2 through 5 use conventional topologies with coupled L-C sections and, in the narrow filters, input and output impedance transformers to bring element values into a realizable range. The sixth and narrowest bandpass filter is a three-section helical resonator design which exhibits a fractional frequency bandwidth of about 2-1/2 percent.

Associated with each bandpass filter is an attenuator which is used to maintain a constant gain bandwidth product for all filters. This feature makes the noise output power independent of which filter is selected, thereby reducing the required AGC range.

Shown in Fig. 3 is the input bandpass filter set with mechanical details of filter 6 shown in Fig. 4. Figure 5 shows frequency response plots of filters 2 through 6.

B. AGC Module

The input signal conditioner is designed to operate with a 55-MHz IF signal whose total signal-plus-noise (S+N) power is in the range of -20 to -50 dBm, and with symbol signal-to-noise ratios (SNR's) between -4 and +20 dB. Because of the bandlimiting which occurs in the input filter module, the AGC module must accommodate input power levels of -53 to -6 dBm.

A wideband AGC amplifier was developed which incorporates a pair of current-controlled attenuators manufactured by Mini-Circuits Laboratory (Part No. PAS-1). The configuration of this AGC amplifier is shown in Fig. 6. Simple, two-breakpoint diode linearizers are inserted in the dc control lines of the attenuators, producing a net gain coefficient of approximately 10 dB per volt over the entire 47-dB operating range. The performance of the AGC amplifier is summarized below:

(1) Total AGC range: 60 dB.

(2) Operating AGC range: 47 dB.

(3) Gain control sensitivity: 10 dB/volt.

(4) Deviation from linear phase: $< 7^\circ$ (25 to 85 MHz).

(5) Frequency response: $\pm$ 0.2 dB (25 to 85 MHz).

(6) Phase shift vs gain setting: $< 2^\circ$ (Δ gain = 60 dB).

The output of the AGC amplifier is fed through a wideband IF amplifier and then passes out of the module. A sample of the AGC amplifier output is supplied to the AGC detector which is a square law, total power device. It produces an output dc voltage which is proportional to the total signal plus noise power present in the 55-MHz IF spectrum at the output of the AGC amplifier. This high-performance detector has an operating range of greater than 30 dB and is similar to one described in Ref. 1. The heart of the detector is a germanium back-diode which has a parabolic region in its current/voltage relationship. The detector output is supplied to the AGC loop filter shown in Fig. 7 whose transfer function is:

$$F(s) = \frac{\frac{R_2}{R_1}}{1 + R_2 CS}$$

This loop filter transfer function results in a first-order AGC control loop with a closed loop bandwidth of 16 Hz and a steady-state output power level held constant to within $\pm$0.3 dB over an input dynamic range of 60 dB. A dc voltmeter with special scale markings indicating proper operating range monitors the AGC control voltage.

C. Complex Mixer Module

The complex mixer receives the 55-MHz IF signal from the AGC module and a 55-MHz local oscillator (LO) signal from the MTDD-F carrier loop hardware. In the suppressed carrier mode of operation, the IF and LO signals are centered at exactly 55 MHz. In the residual carrier mode, the IF and LO signals are at 55 MHz $\pm$20 kHz, with the offsets being a function of the carrier doppler shift. Generated within the complex mixer are the I and Q output signals which are supplied to the high-speed front end.

Upon entering the complex mixer module, the local oscillator signal is passed through a saturating RF amplifier to establish a fixed power level. Then a 7-pole, 65-MHz low-pass

filter removes any second harmonic distortion from the limited signal. This must be done to prevent LO energy at 110 MHz from translating a portion of the input spectrum's upper sideband (which extends above 85 MHz in the wideband mode) into the dc to 30-MHz output spectrum. The filtered LO signal is further amplified and applied to a quadrature hybrid which produces 0° and 90° outputs at 55 MHz. These signals drive the LO ports of a pair of high-level, double balanced mixers.

The 55 MHz IF signal is split with a two-way power divider and applied to the R-ports of the mixers. Frequency difference terms comprise the desired baseband signals. Also included are the original input spectrum and LO signals (both attenuated by the double balanced mixer), the frequency sum terms and higher order mixer products.

Filters were designed to suppress the undesired high-frequency components at the mixer outputs, yet pass the desired dc to 30-MHz baseband signals with minimum distortion. The filters which follow the mixers are passive, lumped constant 5-pole Butterworth low-pass filters with -3 dB corner frequencies of 40 MHz. At 30 MHz these filters are down 0.5 dB, yet they provide 14 dB of attenuation to the LO leakage at 55 MHz and a minimum of 30 dB attenuation at 80 MHz, which is the lower band edge of the image spectrum centered at 110 MHz.

When the widest IF bandwidth is selected, the input spectrum extends below 25 MHz (55 MHz ±30 MHz at -1 dB). Therefore, there is an overlap in the spectra of the input and output signals and the suppression of the undesired components of the input spectrum at the mixers' outputs is limited by the isolation through the mixers and by other leakage paths. Careful layout and reasonable RF construction practice minimize the external leakage paths. Proper terminating impedances for the quadrature hybrid, inphase power splitters and mixers are insured by fixed, 50-ohm pads between these devices. Symmetry of layout and careful selection of filter components result in excellent gain and phase tracking of the I and Q channels over the entire operating frequency range of dc to 30 MHz.

After passing through the low-pass arm filters, the I and Q signals are applied to direct-coupled wideband amplifiers which boost the signal levels, provide a 50-ohm source impedance for driving terminated coaxial output cables, and include clamp circuits which hard limit the outputs at 140 percent of the full-scale output voltage.

Commercially available, ultrawideband hybrid operational amplifiers which appeared to meet the requirements of gain bandwidth product, slewrate, output current, and dc stability were procured and evaluated. These hybrid op-amps were unstable in the configuration required by this application. A discrete wideband op-amp was developed which fulfilled the requirements of the complex mixer output amplifiers. The design uses two stages of differential amplifiers plus a high current output structure. An inverting amplifier configuration is used with the voltage gain of -33 set by input and feedback resistor values. A diode clamp network limits the peak output voltage to 140 percent of the normal full scale value to protect the input circuits of the high-speed analog-to-digital converters in the high-speed front end.

These amplifiers have a closed-loop frequency response which is flat to beyond 40 MHz and operate at slew rates exceeding 400 volts per microsecond. Group delay matching of the two amplifiers permits excellent phase tracking of I and Q channels to beyond 30 MHz. DC offset controls provided in the op amps null internal offsets and also cancel mixer-generated dc offset currents. A schematic of this operational amplifier is shown in Fig. 8. The amplifiers used in I and Q channels are identical.

The complex mixer performance is summarized in Table 2.

III. Packaging

The input signal conditioner hardware is packaged in three aluminum RF modules. These modules were designed to mount in the same rack-mounted cages which are used to hold wire wrap logic boards and can therefore be conveniently employed in systems requiring a mixture of digital and RF hardware. These modules measure approximately 35 cm wide by 15 cm tall. Depth of a two-card slot module is 5.5 cm, and a three-slot module's depth is 9 cm.

Cover plates secured to each side of the modules form an RF tight enclosure. Power and dc control lines pass through multiple inductance – capacitance cavity wall feedthroughs before entering the main cavity, thus providing adequate RF isolation from outside sources of interference. Three terminal voltage regulators provide local power supply regulation within each module, generating all required voltages from single positive and negative supply mains. Shown in Fig. 9 is the complex mixer module with its cover plate removed.

IV. Summary

The MTDD-F input signal conditioner has been designed, constructed and tested. This hardware represents a significant portion of the overall system hardware. Other elements of this system are presently in development and will be the subjects of future articles.

Reference

1. Reid, M. S., Gardner, R. A., and Stelzried, C. T., *A New Broadband Square Law Detector*, Technical Report 32-1599, Jet Propulsion Laboratory, Pasadena, CA, Sept. 1, 1975.

Table 1. Bandpass filter characteristics

Number	Symbol rates	Measured, 2-Sided 3-dB bandwidths
1	4-30 msps	*
2	2-4 msps	21.8 MHz
3	1-2 msps	12.0 MHz
4	0.5-1 msps	5.9 MHz
5	250-500 ksps	2.9 MHz
6	125-250 ksps	1.25 MHz

*Bandpass filtering for the wideband mode (filter 1) is provided by the master amplifier frequency response (–1 dB at ±30 MHz) and the 5-pole, 40-MHz low-pass arm filters in the complex mixer module.

Table 2. Complex mixer performance

Parameter	Value	Comment
Total IF input power	+ 16 dBm	From AGC module output
Data peak voltage	± 0.5 volt	Noise free signal, in phase
3σ noise peaks	± 1.0 volt	Noise only, no signal
Output noise voltage	0.33 vrms (+3.5 dBm)	Noise only, no signal
Output clamp level	± 1.4 volts peak	
I&Q phase relationship	90° ± 4.3° worst case	25 MHz < F_{in} < 85 MHz
I&Q gain tracking	Within 0.2 dB	DC through 30 MHz
I&Q gain matching	Within 0.2 dB	At 10 MHz
55-MHz LO leakage	–30 dBm max.	At I&Q outputs
IF signal leakage	–40 dBc max.	At I&Q outputs

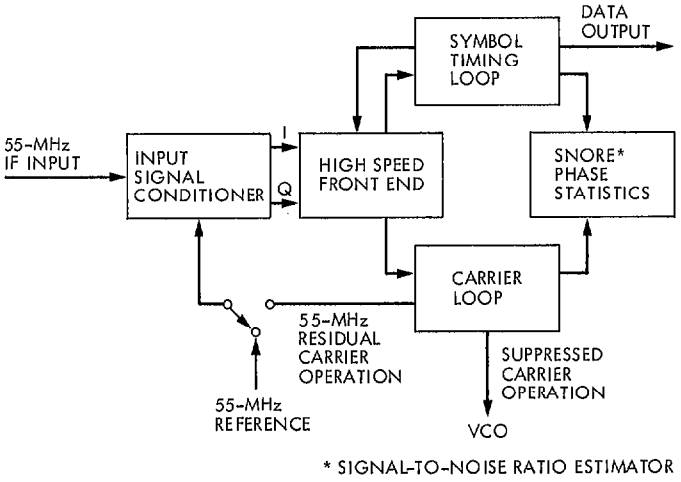

Fig. 1. Multimegasymbol demodulator and detector

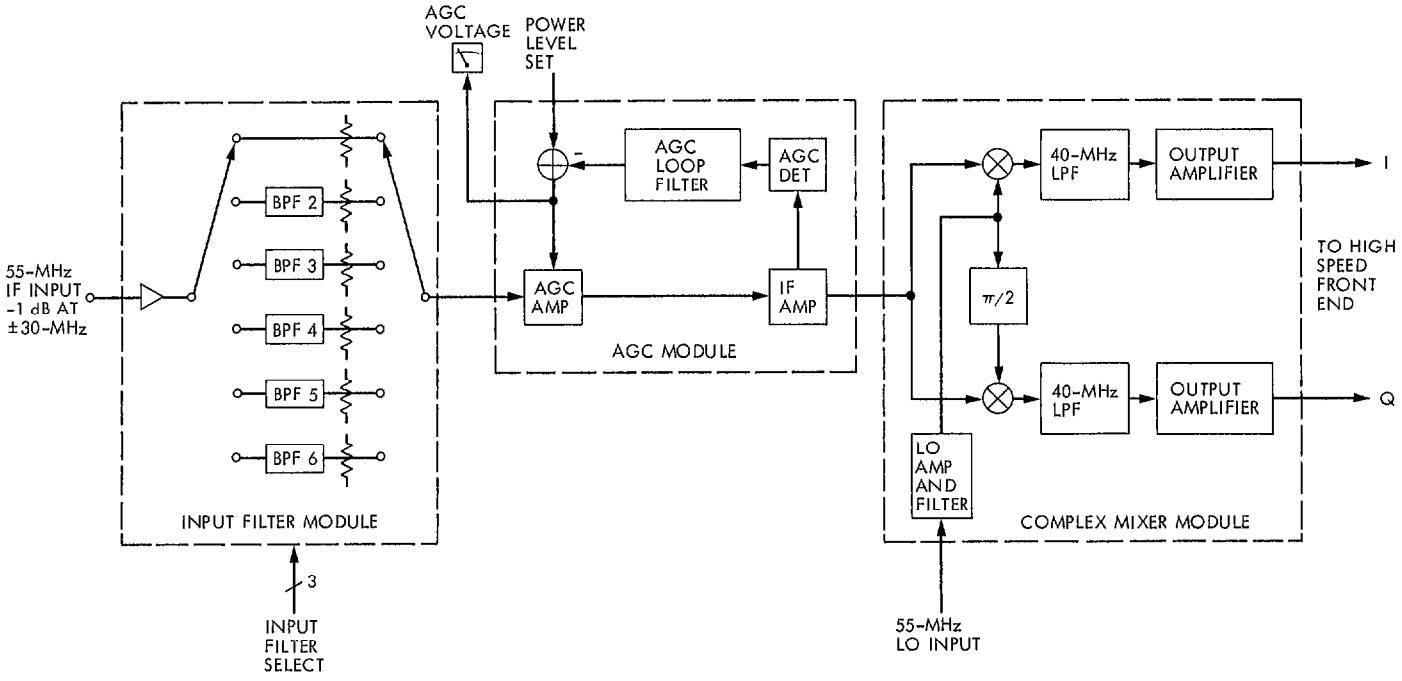

Fig. 2. Block diagram of input signal conditioner

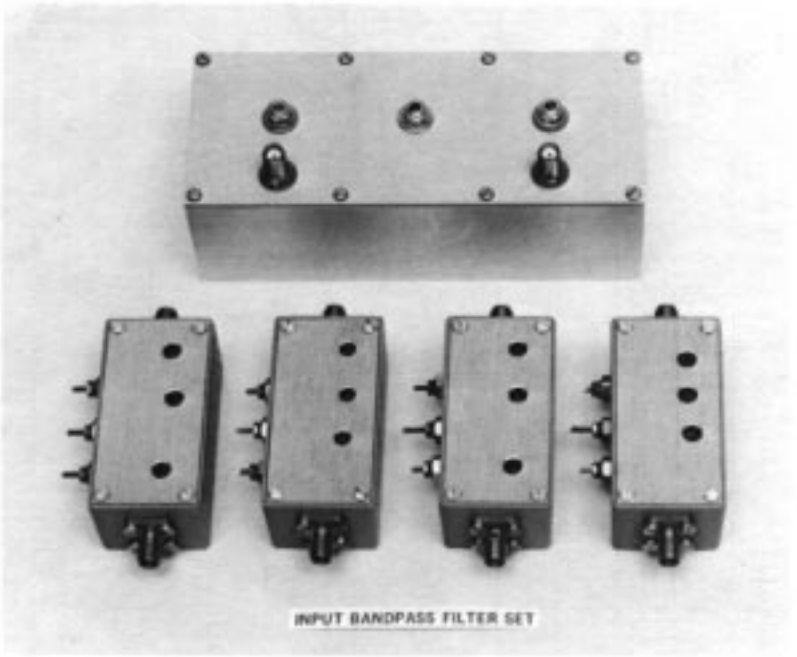

Fig. 3. Input bandpass filter set

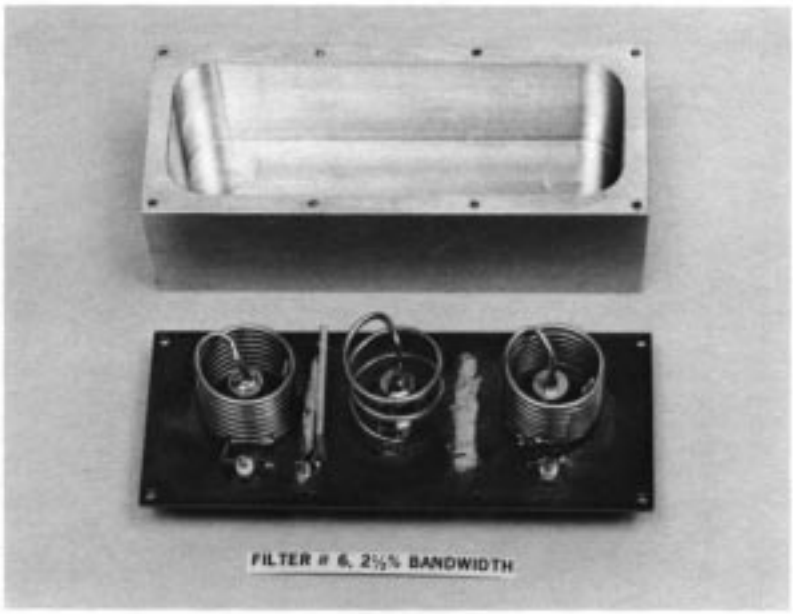

Fig. 4. Filter 6 disassembled

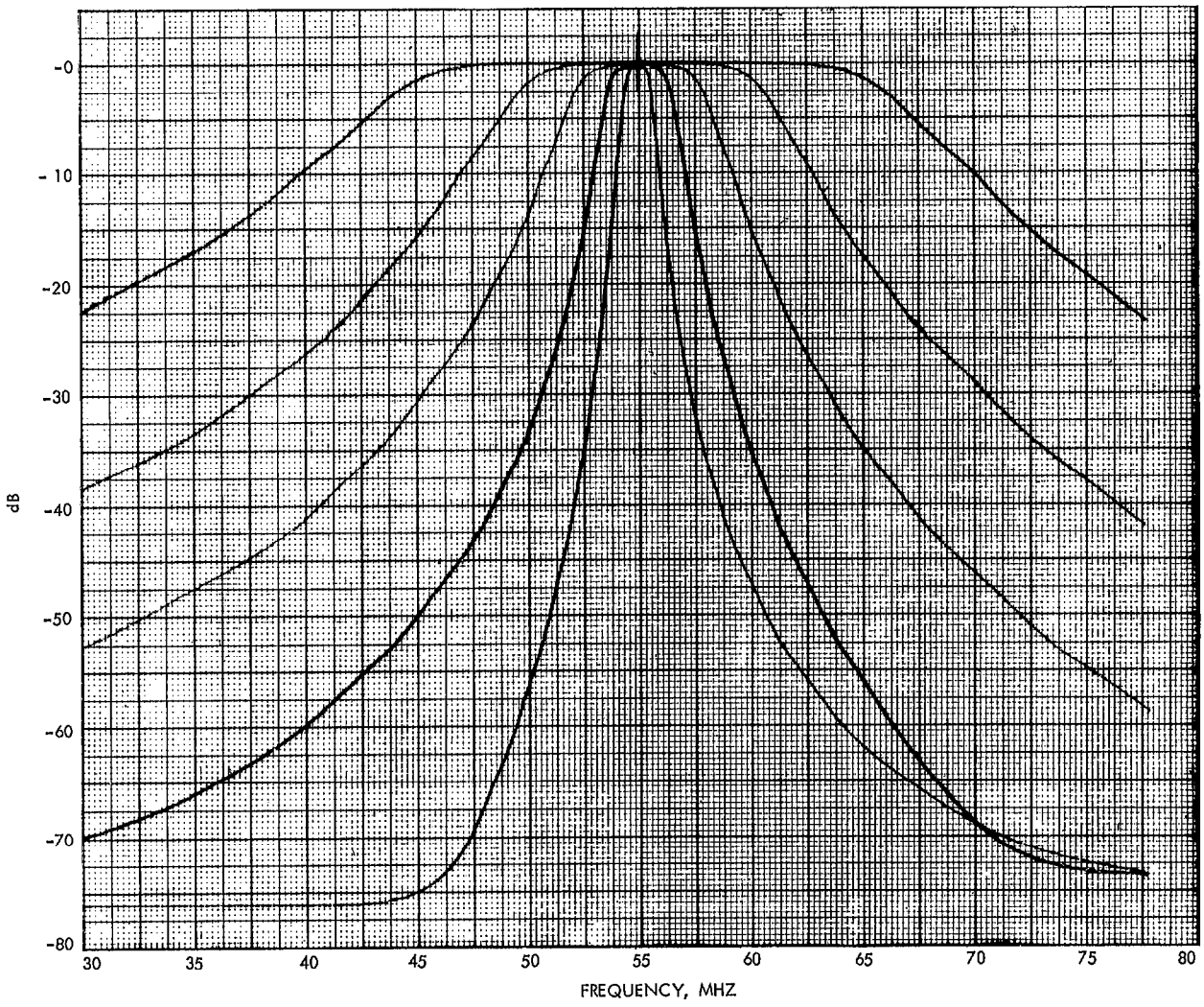

Fig. 5. Frequency response plot of filters 2 through 6

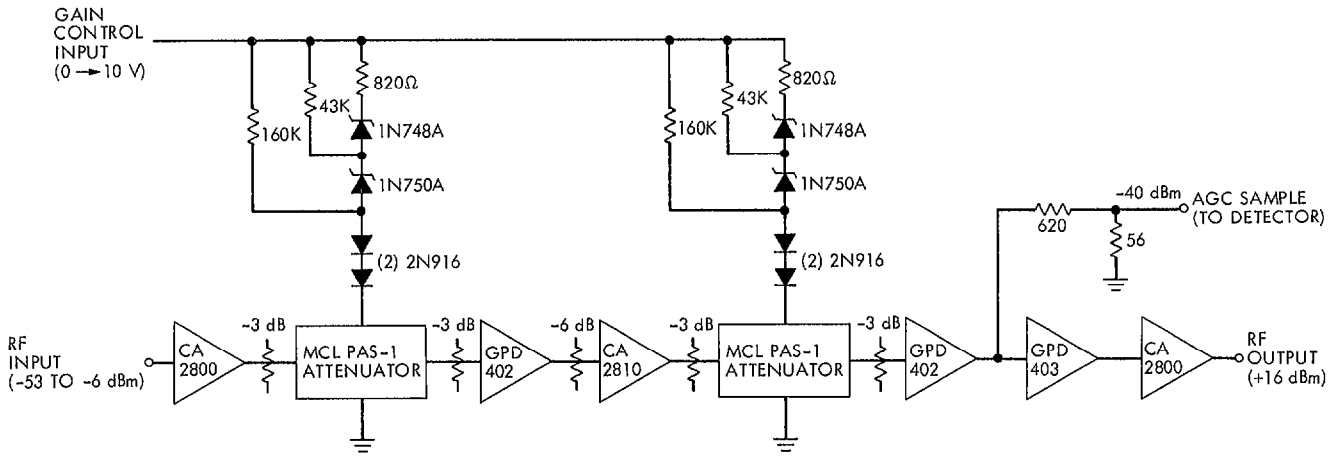

Fig. 6. Wideband AGC amplifier

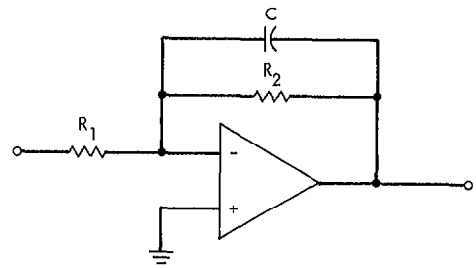

Fig. 7. AGC loop filter

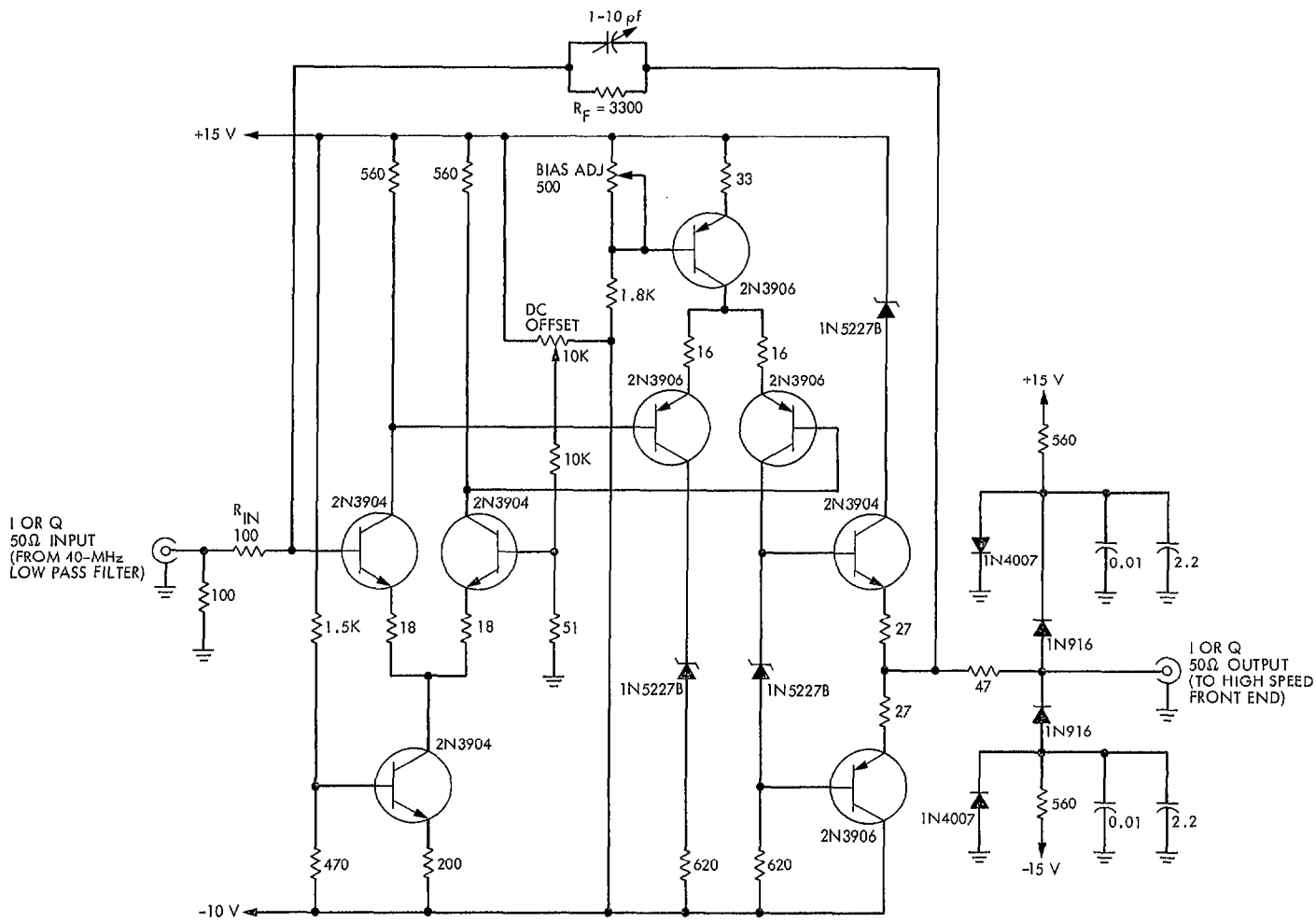

Fig. 8. Complex mixer I and Q output amplifiers

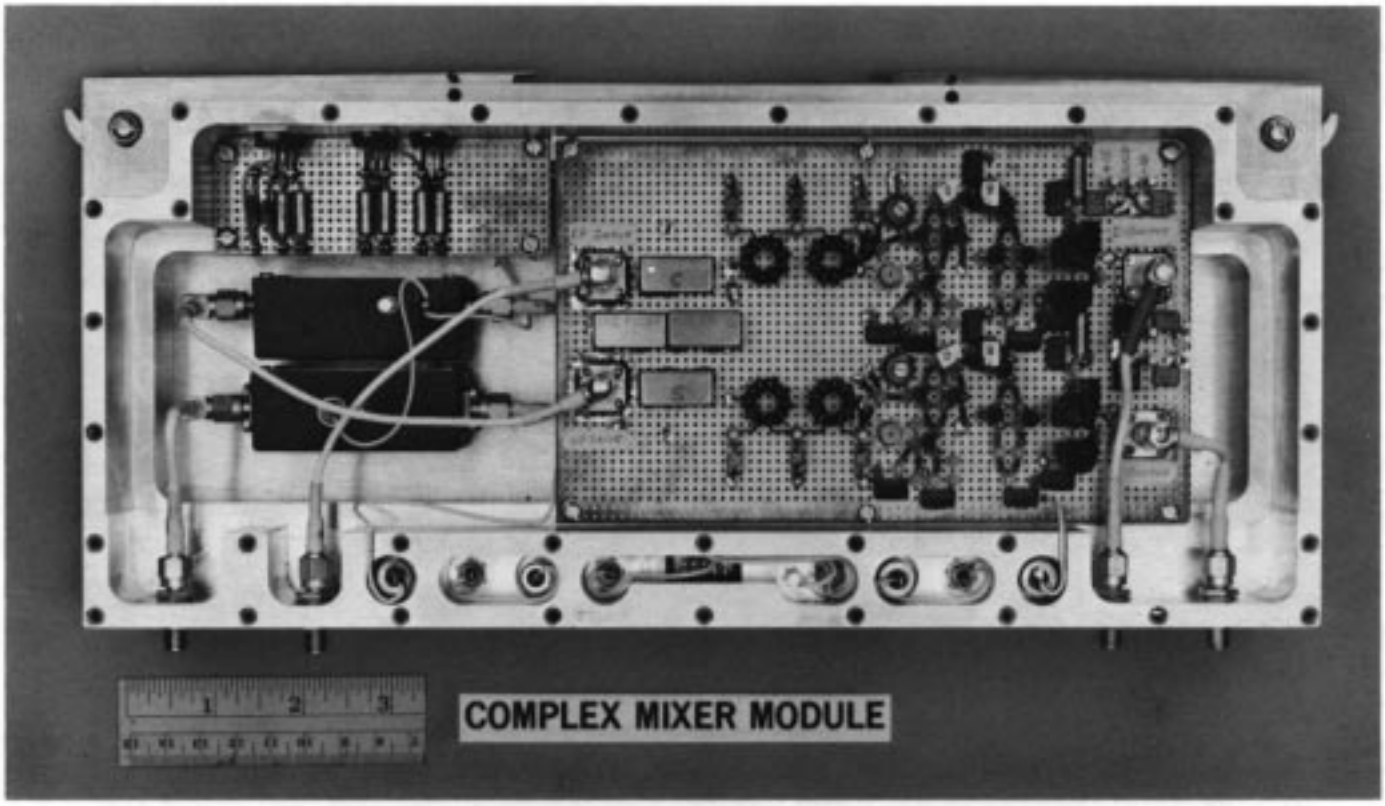

Fig. 9. Complex mixer module