Command System Output Bit Verification

C. W. Odd and S. F. Abbate
Deep Space Network Support Section

Command System bit-verification is a means of testing for errors in the command or idle bit sequences radiated from the Command Subsystem at a Deep Space Station. Errors are tested for by comparing the radiated sequences with reference sequences generated externally by the Command System Performance Test software. The test is used to determine whether or not the detected bit error rate exceeds the allowable rate specified in the Deep Space Network System Requirements document for the DSN Command System.

I. Introduction

An automatic test has been developed to test the ability of the Deep Space Station (DSS) Command Subsystem and exciter to generate and radiate, from the exciter, the correct idle bit sequence for a given flight project, or to store and radiate received command data elements and files without alteration. This test, called the Command System Output Bit Verification Test, is an extension of the Command System Performance Test (SPT) and can be selected as an SPT option.

The test compares the bit stream radiated from the DSS exciter with reference sequences generated by the SPT software program. The Command Subsystem and exciter are verified when the bit stream and reference sequences are identical. It is a key element of the acceptance testing conducted on the Command Processor Assembly (CPA) Operational Program (DMC-0584-OP-G) prior to its transfer from Development to Operations.

II. Test Configuration and Subsystem Functions

Figure 1 shows the test configuration used for bit verification testing. It is divided into two parts: a Mission Operation Center (MOC) section and a DSS section. Within the MOC section is the SPT Assembly (SPTA), which consists of the SPT software and the computer in which the program runs to simulate command functions of the MOC. The DSS section contains the following subsystems: The Communication Monitor and Formatter (CMF), the Command Subsystem which is made up of the Command Processor Assembly (CPA) and Command Modulator Assembly (CMA), the Receiver-Exciter Subsystem (exciter, test translator, receiver) and the Telemetry Subsystem which consists of the Subcarrier Demodulator Assembly (SDA), Symbol Synchronizer Assembly (SSA) and Telemetry Processor Assembly (TPA).

The SPTA simulates a MOC by generating command elements, formatting them into high-speed data (HSD) blocks and sending them to the DSS Command Subsystem. It also produces a model of the expected command bit stream radiated from the Command Subsystem. The bit verification program consists of several subprograms and overlays to the SPT program which add the capability to receive telemetry HSD blocks, reclaim the command bit stream from the telemetry blocks, generate idle sequences and compare two bit streams.

In the DSS section, the Receiver-Exciter and Telemetry Subsystems intercept the command bit stream at the output of the exciter, reformat it into telemetry HSD blocks and return it to the SPTA.

III. Software Functional Description

The ability of the bit verification test to compare command sequences in the bit stream with reference sequences is made possible by combining the capabilities of the command SPTA, with those of the Receiver-Exciter and Telemetry Subsystems. In operation it works as follows: the SPT program detects a returning telemetry block, places it in an HSD block buffer and calls a subroutine to extract its data content – whether it be an idle or a command sequence. Next, a routine is called which determines the mode of the CPA, the spacecraft for which it is configured and the presence or absence of Manchester coding. The SPT program then generates a reference sequence with which to compare the returning sequence.

When the CPA is in idle mode, the reference sequence generated is the idle sequence corresponding to the CPA project configuration. The SPT program (using the bit verification capability) compares the returned sequence with the reference sequence, one bit at a time, starting with the first bit returned. Since there is no starting point in the reference sequence, the two sequences may not be synchronized. Therefore, if the initial bits compared are not alike, the bit verification program attempts to synchronize the two sequences by shifting the output sequence one bit with respect to the reference sequence and again compares the first bit of the output sequence with the next bit of the reference sequence. This shift is repeated up to three times if no comparison is found. Finally, if this fails to find a match, a comparison is attempted with the complement of the reference sequence. If this also fails, the program will halt and display an operator message indicating an improper idle sequence. If a match is found, the program will continue to compare subsequent bit pairs until either a mismatch occurs or the SPT program sends an active mode directive to the CPA. All mismatches will cause an operator message to be displayed and identify the block containing the mismatched bit.

If an active mode directive is sent to the CPA, the idle sequence will be replaced with command data sequences in the form of contiguous command elements and files. These will be compared to reference sequence as were the idle sequences and any mismatch logged. The output and reference sequences will be synchronized with the occurrence of the active mode directive from the SPT program. However, unlike idle sequences, the reference sequences are reproductions of the actual command elements sent to the CPA. This is possible because each element generated in the SPT program is a number (or dummy command) generated by a pseudo-random number generator from an initial integer value (or seed word) saved by the SPT program. These elements are sent to the CPA in HSD blocks where they are stored by the CPA in files until ready for radiation. When they are radiated, the SPT program (which independently models these CPA functions) notes which elements are supposed to be radiated and regenerates them from the stored seed words to produce the correct reference sequence.

IV. Procedures

The bit verification option of the command SPT test procedure is a part of the DSN series 850 Standard Test Procedures.

V. Conclusion

The test was used as part of acceptance testing of the CPA software (DMC-0584-OP-G) to verify that the undetected bit error rate for data radiated from the DSS Command Subsystem did not exceed the maximum rate of one in 10^6 bits specified in the DSN System Requirements document. Four hours of error free radiation of both Helios and Voyager test commands were confirmed. This represents continuous error free radiation of approximately 115 kbits of Helios data and 230 kbits of Voyager data.

This test is incorporated in the Mark III 78 (Store-and-Forward) command program for use with the Helios, Voyager, Galileo and International Solar Polar Mission. It is useful for acceptance testing of new Command System software and software in which algorithms have been changed which affect the bit content of the Command System output. It may also be used to verify the system following Engineering Change Order implementation.

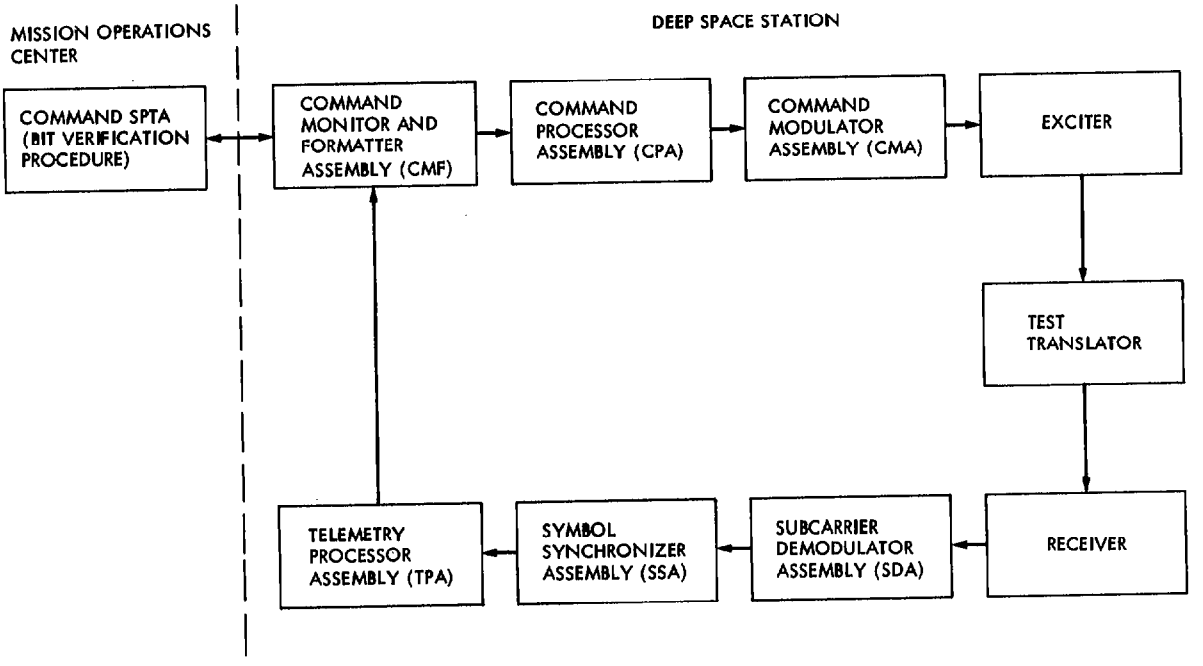

Fig. 1. Bit verification test configuration