Narrow Channel Bandwidth Receiver for VLBI

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An introduction to the Phase 4 Receiver Subsystem to be implemented into the DSN for VLBI applications is presented. The key design areas are discussed along with the design approach. Preliminary evaluation data indicate that a feasible, straightforward design may be obtained.

I. Introduction

Navigation techniques utilizing very long baseline interferometry (VLBI) were successfully demonstrated in 1979 using the Voyager spacecraft near Jupiter encounter. Since this demonstration, which essentially used existing receiving and processing equipment, a series of improvement phases have been in progress to arrive at a major phase (Phase 4) that will implement the receiver described below. The configurations of phases 1, 2, and 3 were unchanged with respect to the receiver and the principal changes were related to the Network Operational Control Center and VLBI Processing Area. The Phase 4 receivers operate at both S- and X-band and will replace the DSS Block IV receivers for this application.

The Phase 4 receiver being developed employs double conversion and narrowband filtering to permit the utilization of tape recording and/or data transmission lines that operate in the audio and video frequency range. The first downconverter takes the RF signals down to IF, and the second downconverter converts the IF signals to video frequencies. The problem with the above scheme is that image noise foldover becomes an important consideration. To overcome this problem, a single sideband (SSB) down-conversion technique is used, but the complete IF-to-video down conversion is comprised of analog and digital techniques. This combination provides good spectrum rejection to prevent image noise foldover and also provides low-amplitude ripple and phase ripple, which are necessary to meet system requirements. The receiver subsystem is required to furnish only the analog portion of the IF-to-video downconverter, i.e., two video signals in quadrature, 0 and −90 deg, to the Radio Science Subsystem (DRS). In turn, DRS will use digital techniques to generate the second −90-deg phase lag and summation to accomplish the image rejection and the low phase ripple. Another significant feature of this new receiver is its low phase noise and small phase dispersion contributions to the down-converted signal. This is necessary to limit the group delay error to the desired signals.

A general description of this receiver is given below along with more detailed description of its principal components.

II. Design

The open-loop receiver under development for Phase 4 is characterized by double conversion, high phase stability, and output channels in quadrature. In addition, the receiver will be

operable from a central facility for controlling and monitoring, and will be capable of unattended operation. The receiver subsystem comprises two independent receivers for simultaneous S- and X-band reception. Each of these receivers has independent IF-to-video downconverters. Within a span bandwidth of 100 MHz and 40 MHz for the X- and S-band, respectively, eight narrowband data channels will be available for X-band and four for S-band. An important characteristic of the analog portion of the IF-to-video downconverter is the use of 12 digitally controlled local oscillators. This design maintains continuous operation of the individual oscillators and ensures that signal phase continuity of the individual channels is preserved as they are multiplexed during observations of either radio star or spacecraft signals. A simplified block diagram illustrating the principal components of the receiver is shown in Fig. 1, and the receiver subsystem design parameters are given in Table 1. Of these, the critical ones are the quadrature channel balance (which relates to image rejection and low phase ripple) and the phase stability.

To meet the design goals of the receiver subsystem, the initial approach is to modify the existing front end of the multimission receiver (MMR) and to generate a new design for the analog portion of the IF-to-video downconverter. A significant part of IF-to-video downconverter task comprises the selection of the synthesizers that serve as local oscillators. Because there are 12 synthesizers per X- and S-band IF-to-video downconverter, a total of 36 synthesizers plus spares will be required for three 64-m station sites. Therefore, the design approach had to include an evaluation program to arrive at a cost-effective synthesizer. The evaluation of the synthesizers is currently in progress and will be completed in August.

While the IF-to-video downconverter is primarily concerned with the phase quadrature and amplitude imbalance requirements, the local oscillators and mixers are the main concern with respect to the phase stability. Simplified models of the receiver subsystem have been generated (Refs. 1 and 2), and these have been discussed in terms of phase-error contributions. The phase error as a parameter is of interest because it is involved directly in the VLBI application. Unfortunately, phase error as a function of integration time is not a criterion used in the industry with respect to specifying mixer and local oscillator performance. Single sideband spectral density in the frequency domain and frequency deviation in the time domain are widely used as performance criteria by industry. Fractional-frequency deviation measurements are presently being used to measure the stability of receiver components and these measurements can be directly related to the stability of the hydrogen maser. Therefore, a frequency stability technique is desired for the measurement of receiver subsystem stability. Attempts to generate a sufficiently accurate frequency-to-phase transformation are in progress. Success in generating the transform will permit verification that the frequency stability of the receiver subsystem is in keeping with the phase error required in the VLBI application.

Using a simplified model of the receiver subsystem (as in Refs. 1 and 2) a fractional-frequency deviation analysis has been made to generate stability criteria for the synthesizers and to relate the frequency stability of the subsystem to a phase error as a function of time. This analysis is given in the Appendix. A simple frequency-to-phase transformation was used, and the results indicated the receiver subsystem was close to the range of the desired phase stability. While more refinement is still in progress with respect to relating the frequency deviation and the phase error, the analysis has given sufficient confidence for going forward toward the building of breadboard assemblies that would support the design goals given in Table 1.

The other components of the receiver subsystem are considered to be straightforward in design and will not be described in this report. However, the initial design of the receiver subsystem including all the components is shown in Fig. 2.

A. IF-to-Video Downconverter

The analog section of the IF-to-video downconverter is a four-port assembly consisting of two inputs and two outputs. One input is the IF signal and the other is the LO signal from the Synthesizer Subassembly. The outputs are two identical video frequency signals possessing a phase shift of approximately 90 deg between them and having nearly equal amplitudes. These outputs are subsequently delivered to the digital subsystem. The block diagram of the analog portion of the downconverter is shown in Fig. 3 and the key design goals of the analog section are given in Table 2. To limit the noise contribution of the suppressed sideband to the desired signal, a system requirement of 23-dB image rejection ratio has been imposed. The method of implementing the IF-to-video downconverter function is described by Weaver (Ref. 3) and image rejection ratio and phase ripple characteristics of the outputs are dependent on the amplitude and phase balance of the components comprising the converter. The image rejection ratio, I, in terms of amplitude and quadrature imbalance components, is given by

$$I = 10 \log \left(\frac{A_1^2 + A_2^2 + 2A_1A_2 \cos \delta}{A_1^2 + A_2^2 - 2A_1A_2 \cos \delta} \right) \quad (1)$$

in which A_1 and A_2 are the amplitudes of the two signals in quadrature and δ denotes their phase difference. The analog portion of the phase and amplitude imbalance is given in Table 2.

To investigate the manner in which the respective imbalance of each component contributes to the overall performance, a partial model of the analog section was assembled using available parts. The antialiasing filters and video amplifiers were not included due to the unavailability of suitable filters with a cutoff frequency of 300 kHz. Figure 4 is the block diagram of the test assembly used for initial design parameter measurements. Low-pass filters with 150-MHz cutoff frequency were used to eliminate the upper sideband from the inputs to the gain-phase meter.

Amplitude and phase data were measured by setting the signal levels for maximum beat note amplitude. In Fig. 5 are shown the measured relative phase shift and the amplitude ratio of the 250-kHz beat note output from the test assembly.

The amplitude imbalance is 0.1 dB over the band 265 MHz to 400 MHz. The observed differential phase shift is within 90 ±2 deg. Maximum image rejection is obtained when the differential phase shift is 90 deg assuming the digital subsystem processes the signal ideally. Data were taken also across small (0.2-MHz) frequency increments over selected portions of the band. These data indicate both amplitude and phase characteristics were free of rapidly varying ripples. The experimental data generated with the test assembly are expected to degrade somewhat when the low-pass filter and video amplifiers are included. However, the experimental data taken with the test assembly indicate that with the use of components selected for closer tolerance, the present design objectives of 90 ±4 deg, ±0.4 dB, and ±0.75 deg for phase shift, amplitude balance, and phase ripple respectively, can be achieved.

B. Synthesizer Subassembly

The technique of bandwidth synthesis (BWS), used in determining group delay in narrow channel bandwidth VLBI, requires a controlled selection of stable signal sources, used as local oscillators, into the IF-to-video downconverter. A block diagram depicting the control and use of the synthesizers is shown in Fig. 6. A digital control interface to the receiver controller provides the controlling and monitoring functions to this subassembly. Time tagged predicts from the control computer will be sequenced to provide BWS channels. The stability of the synthesizer signals is derived from the highly phase-stable reference provided by the hydrogen maser through the FTS.

While the function of the subassembly is straightforward, the primary concern is the procurement specification of the synthesizers. It was previously mentioned that a total of 36 synthesizers plus spares are required for the three station sites. Thus, there is a tremendous cost leverage that prompted an evaluation program to obtain a cost-effective synthesizer. The prices of commercially available synthesizers range from $6K to $30K and their performances are also widely varied. In addition, the digitally controlled synthesizer (DCS) used in the Mark III System is also considered a prime candidate because of its previous use and because of the possibility of lower costs due to its single-purpose function (the commercially available synthesizers all have multipurpose functions). The performance parameters the synthesizers must meet to support the overall performance of the receiver subsystem are given in Table 3.

The plan for the synthesizer selection centers about the evaluation of some commercial synthesizers and the Mark III type DCS with respect to the parameters delineated in Table 3. From the spectral-purity and frequency stability requirements, the number of synthesizer candidates was narrowed to four: Hewlett-Packard Model HP8662, Ailtech Model 460, John Fluke Model 6071, and the Mark III type DCS (also called the Haystack DCS). These units meet all the requirements except that of phase stability, which is still under study. However, the key performance parameter measured has been the fractional-frequency deviation, which relates directly the synthesizers' stability to that of the hydrogen maser.

To obtain the most meaningful and precise stability measurements, the synthesizers were locked to a hydrogen maser. A block diagram depicting the method used to measure the stability of the various synthesizers is found in Fig. 7. Fractional-frequency data were taken over a range of integration times up to 1000 s. The results of three units are shown in Fig. 8. The data indicate that a JPL-built Haystack DCS and the Fluke 6071 exhibit essentially the same stability. The HP8662 synthesizer is far superior in performance at integration times below 100 s and about the same as the other two synthesizers in the 100- to 1000-s integration times. The JPL-built Haystack DCS used in this measurement is one of three units especially fabricated for evaluation for use in the Phase 4 receiver.

The Ailtech Model 460 synthesizer does not have the frequency setting resolution of the other synthesizers tested. Therefore, its frequency stability was measured with a larger offset frequency, ν_b. For example, the data shown in Fig. 8 were taken with ν_b equal to 1 Hz while the Ailtech was measured with ν_b equal to 10 kHz. For consistent comparison with the other synthesizers, data were also obtained with the other synthesizers for ν_b equal to 10 kHz. The data are shown in Fig. 9. An apparent loss of stability is observed when a much larger offset and measurement bandwidth are used; these data can be normalized to the 1-Hz offset, if desired. The key point, however, is that the relative merit of the synthesizers is fairly obvious. The HP8662 exhibits the best performance. The JPL-built DCS and Fluke 6071 are about a factor of 5 less

stable than the HP8662 at $\tau \leqslant 10$ s and have comparable stability with the HP8662 at integration times 100 to 1000 s. The Ailtech Model 460 exhibited the lowest stability and is marginal with respect to the VLBI application.

Other measurements, e.g., single sideband phase noise and rms phase jitter at short integration times (<10 s), have been performed on the synthesizers. In addition, initial temperature effects on phase drift have been measured on the JPL-built DCSs. The continued refinement of these measurements and those described in this report, in conjunction with cost analysis, will be used to make the final selection in August 1981.

III. Future Plans

To support the VLBI plans, the receiver subsystem must be designed, fabricated, and tested as a breadboard model by March 1982. This is a key milestone and signifies the earlier completion of experimental and analytical investigations with respect to the analog portion of the IF-to-video downconverter, including the synthesizers. Additional significance to this milestone is that it is the start of the procurement cycle for six complete receivers plus spares. This procurement is expected to take about 22 months for completion by January 1984.

While trade-offs among the various parameters will still occur until all the system and subsystem designs are consolidated, the design parameters given in Table 1 are presently the targets for the receiver breadboard model. Based on the data acquired thus far and on the planned modifications to the front end, the indications are that a receiver subsystem breadboard model capable of meeting the design parameters delineated in this report can be achieved.

References

1. Ham, N. C., "Frequency Down-Converters as Applied to VLBI," *DSN Progress Report 42-53*, pp. 74-82, Jet Propulsion Laboratory, Pasadena, Calif., July 1979.
2. Ham, N. C., "VLBI Receiver Phase Stability Specification," Interoffice Memo NCH:3300-80-214, Jet Propulsion Laboratory, Pasadena, Calif., November 1980. (JPL internal document.)
3. Weaver, D. K., "A Third Method of Generation of Single Sideband Signals," *Proc. IRE*, pp. 1703-1705, December 1956.

Table 1. VLBI, Phase 4 Receiver Subsystem design parameters

Performance parameters	Values	
	X-band	S-band
Input		
Frequency range, MHz	8400 to 8500	2265 to 2305
Span bandwidth, MHz	100	40
Sinusoid input power, dBm	−67 to −114	−65 to −124
Noise input power, dBm/Hz	−131 to −173	−132 to −162
Output		
Number of data channels	8	4
Bandwidth of data channels, kHz	360	360
Channel tuning resolution, kHz	$\leqslant 10$	$\leqslant 10$
Channel time multiplexing, s	0.2	0.2
Output signal level, V	±5	±5
Quadrature channel balance		
Amplitude, dB	$\leqslant \pm 0.4$	$\leqslant \pm 0.4$
Phase, deg	90 ±4 deg	90 ±4 deg
Data channel phase ripple, deg	±0.75	±0.75
Phase stability		
Nonrandom, deg peak ($\Delta t \leqslant 30$ s)	$\leqslant 1$	$\leqslant 1$
Phase jitter, deg rms ($\tau < 10$ s) 1 Hz $< f_{offset} <$ 250 kHz	6	6
Random error, deg rms		
1 s $< \tau <$ 10 s	4	4
10 s $< \tau <$ 25 s	0.4 τ	0.4 τ
25 s $< \tau <$ 600 s	10	10

Table 2. Design goals for analog section IF-video downconverter

Parameter	Value
Input frequency range	265 to 400 MHz
Input, signal level, sinusoid	−3 dBm max
Output signal level (5000 Ω)	±5 V max
Output frequency range	10 to 250 kHz
Mixer synthesizer drive	+7 dBm
Differential phase of output	90 ±4 deg
Output amplitude balance	±0.4 dB
Output phase ripple	±0.75 deg

Table 3. Digitally controlled synthesizer performance parameters

Parameters	Value
Frequency range	265 to 400 MHz
Frequency resolution	$\leqslant$10 kHz
Frequency stability	4×10^{-13} at 30 s
Output power over frequency range	$\geqslant$0 dBM ±1 dB
Spectral purity	
Harmonics	<−25 dBc
Spurious	<−40 dBc
Power line related	<−60 dBc
Remote programming	IEEE-488 [GPIB]
Frequency selection	<5 s
Status monitor	—
Leakage/susceptibility	<10 μV
Operating temperature range	20 to 30°C

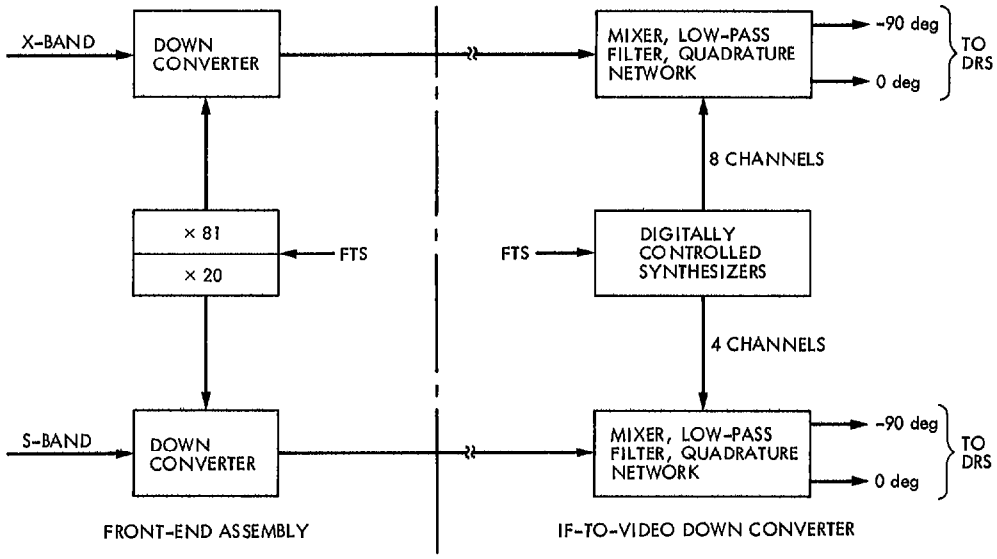

Fig. 1. Simplified block diagram of Phase 4 receiver

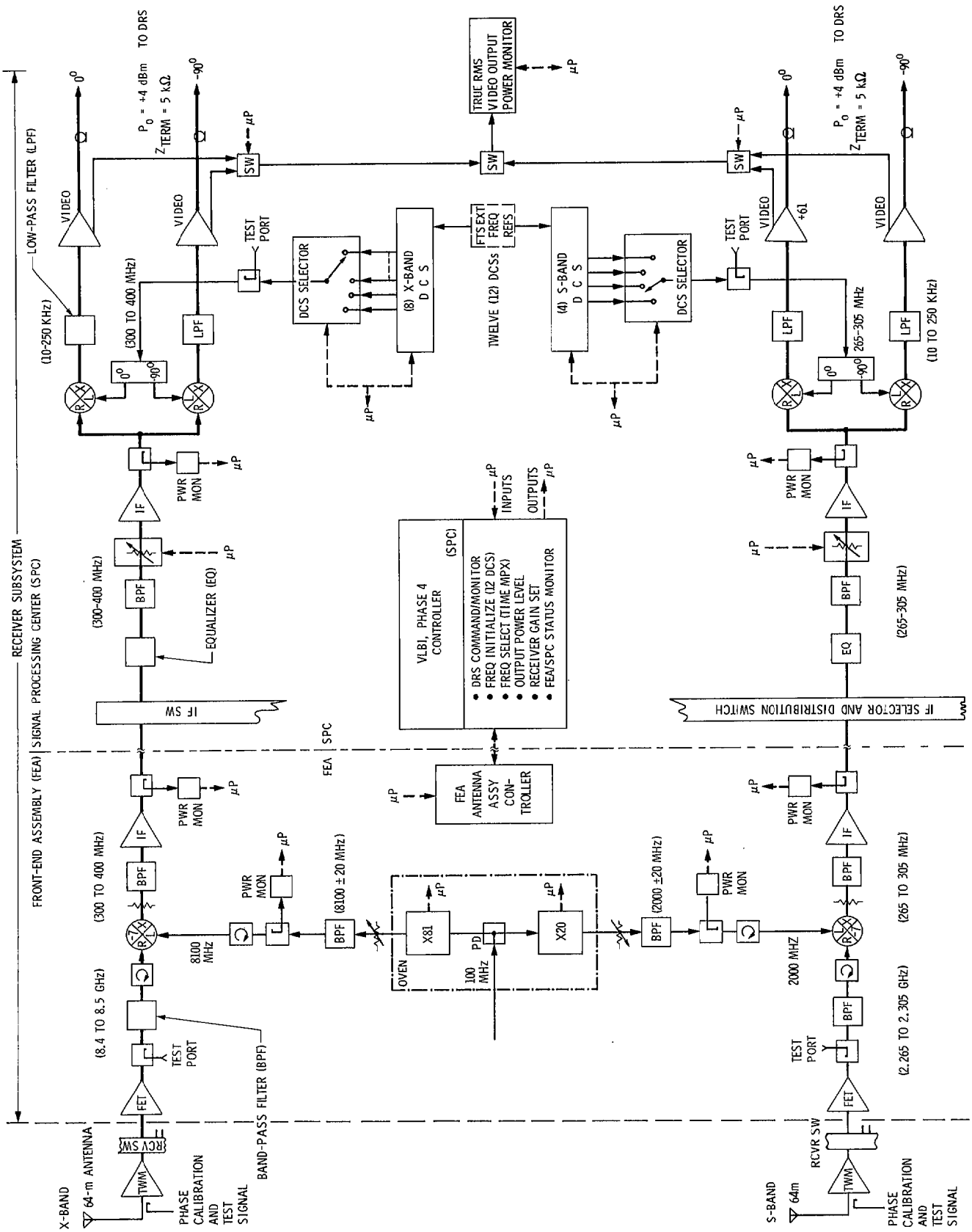

Fig. 2. Initial design of the Phase 4 Receiver Subsystem

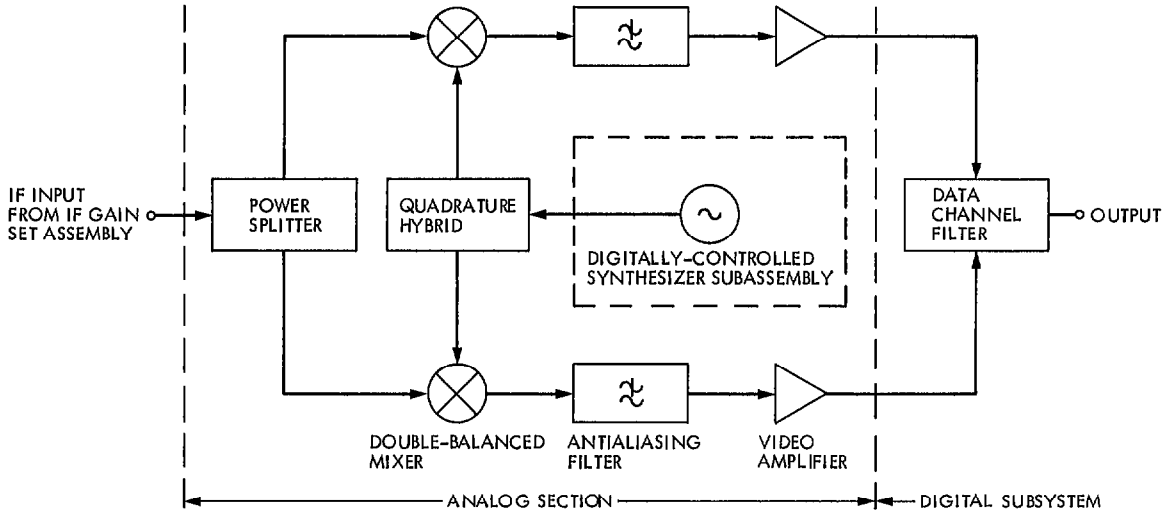

Fig. 3 IF-to-video downconverter

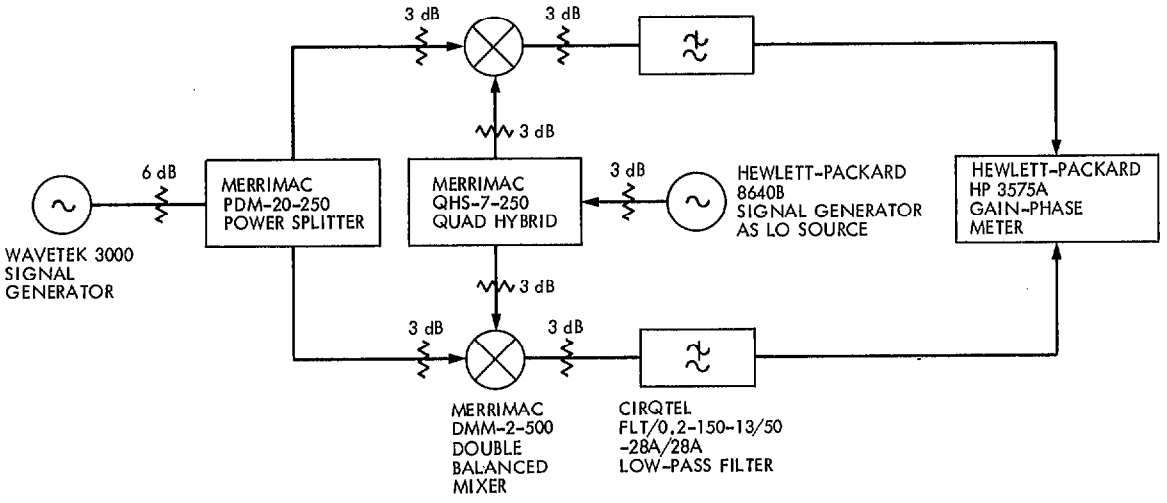

Fig. 4. IF-to-video downconverter, analog section test assembly

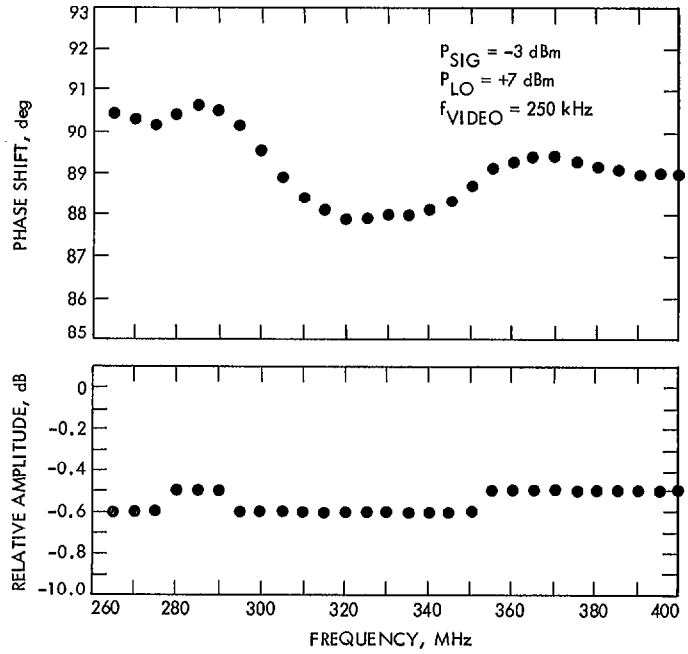

Fig. 5. Test assembly relative phase and amplitude ratio at 250-kHz output frequency

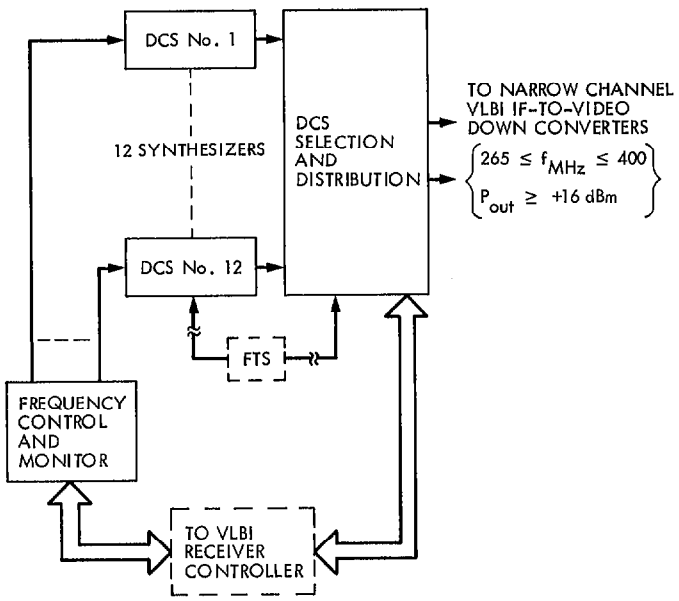

Fig. 6. Synthesizer subassembly

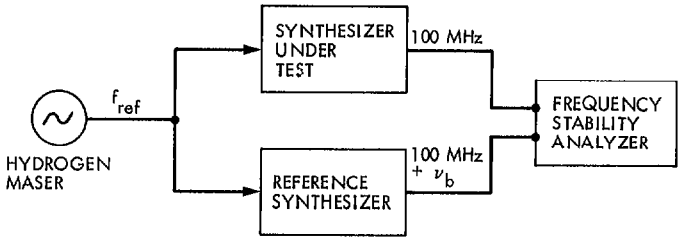

Fig. 7. Measurement method for synthesizer comparison

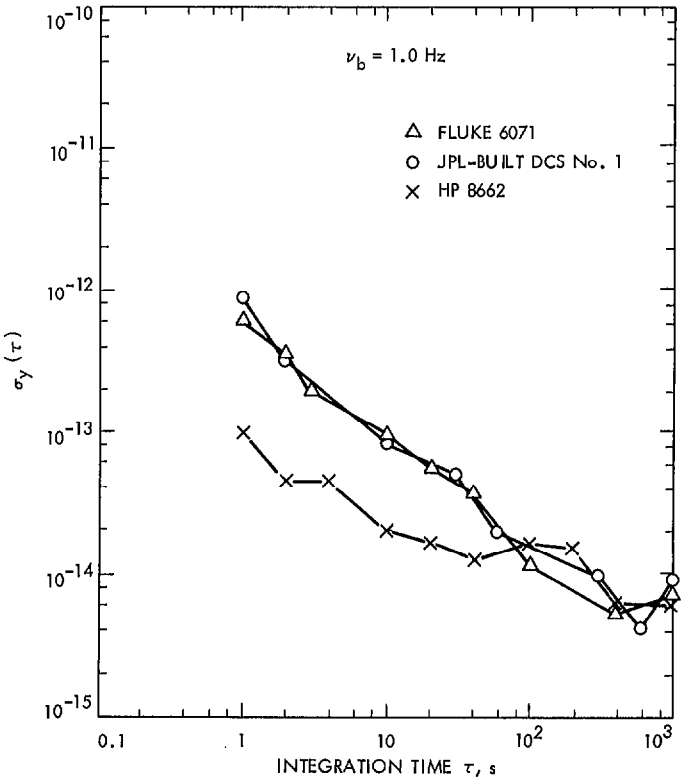

Fig. 8. Fractional frequency deviation of Fluke 6071, HP8662, and JPL-built DCSs

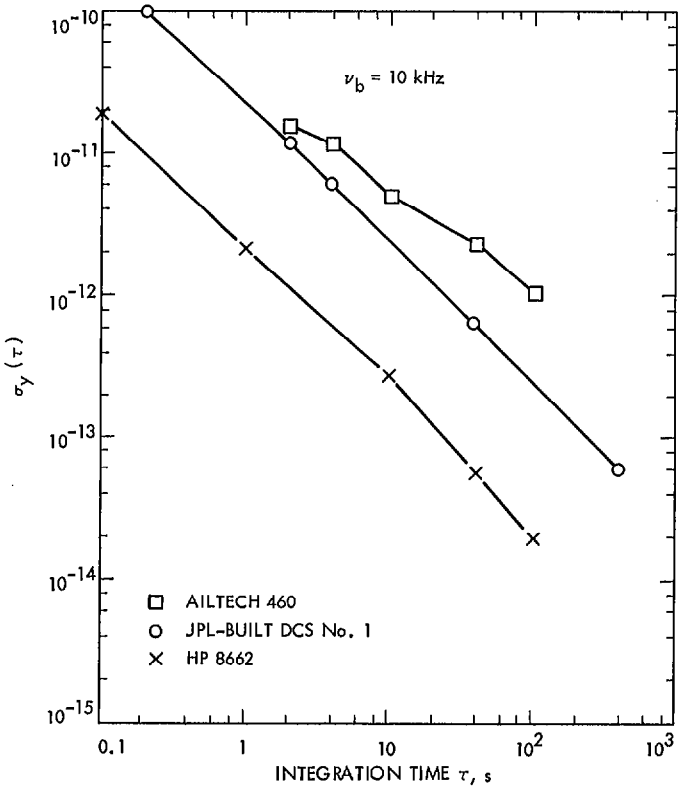

Fig. 9. Fractional frequency deviation of Ailtech 460, HP8662 and JPL-built DCSs

Appendix
Frequency Stability Model

To obtain an idea of the frequency stability expected at the receiver's output for a double down-conversion process, a simplified receiver model is generated below. The principal components of this model are shown in Fig. A-1. In this model, σ's denote the fractional-frequency deviation as a function of integration time and the frequencies, f's, pertain to the different ranges, e.g., microwave, IF, and video.

The relationship of the inputs to a mixer and its output in terms of fractional frequency deviation is

$$\sigma_{mixer\ out} = \sqrt{\left(\frac{f_{input}}{f_{mixer\ out}}\ \sigma_{input}\right)^2 + \left(\frac{f_{LO}}{f_{mixer\ out}}\sigma_{LO}\right)^2} \qquad (1)$$

For our particular case, the above equation is applied twice; once for the first downconverter, and again for the IF-to-video downconverter. The net result of the operation gives a working equation, which is

$$\sigma_{out} = \sqrt{\frac{f_{in}^2}{f_{out}^2}\ \sigma_{in}^2 + \frac{f_{LO}^2}{f_{out}^2}\ \sigma_{LO}^2 + \frac{f_{DCS}^2}{f_{out}^2}\ \sigma_{DCS}^2} \qquad (2)$$

By ascribing some practical values to the variables of Eq. (2), one can see the dependence of σ_{out} on σ_{DCS} i.e., on the stability of the synthesizer. For example, if we let $\sigma_{in} \cong \sigma_M \cong 6 \times 10^{-15}$, f_{in} = 8500 MHz, f_{LO} = 8100 MHz, f_{DCS} = 400 MHz, f_{out} = 10 kHz, and $\sigma_{LO} \cong 7.5 \times 10^{-15}$, for an integration time of 30 s and a measurement bandwidth of 1 Hz we obtain the graph shown in Fig. A-2. The graph indicates that the DCS stability can be as large as 10^{-13} before it starts affecting the output signal's frequency stability of 7.6×10^{-9}. Using 4×10^{-13} as the value for minimum frequency stability for the synthesizer gives a fractional-frequency deviation, σ_{out}, of 1.8×10^{-8} for the output signal. One obtains a phase jitter equivalent by using

$$\Delta\phi = \sigma_{out}\ f_{out}\ \tau\ 360 \qquad (3)$$

where $\Delta\phi$ is the phase jitter, f_{out} is the output signal at 10 kHz, and τ is the integration time (30 s). Substitution of the aforementioned values yields, $\Delta\phi \approx 2$ deg.

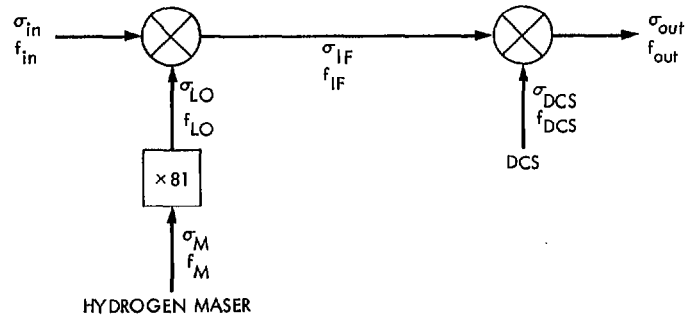

Fig. A-1. Double conversion model

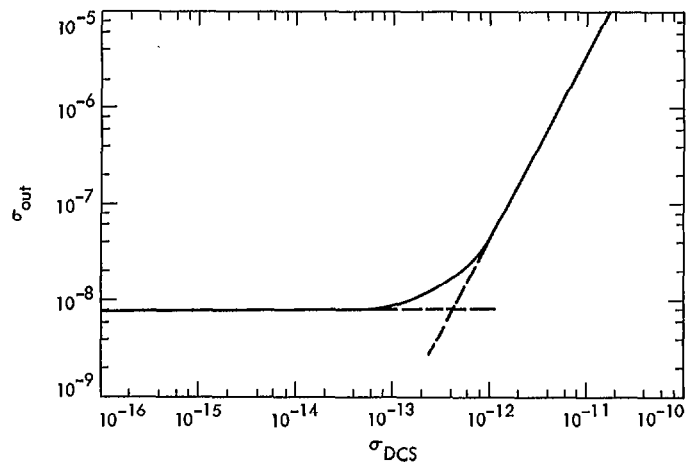

Fig. A-2. Fractional frequency stability of the output signal as a function of synthesizer stability