SETI Downconverter

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The SETI (Search for Extraterrestrial Intelligence) breadboard subsystem was begun in order to develop the technology to efficiently implement a SETI instrument capable of searching wide bandwidth with high resolution. Due to the recent directive from Congress to terminate the program, NASA has tasked JPL to complete the SETI breadboard (since it is more than half complete) so that it will be available for use by a NASA-selected user by the end of FY 82. The downconverter covered in this report is the interface hardware between the receiver IF output and ADC used as the input to the spectrum analyzer.

The SETI (Search for Extraterrestrial Intelligence) downconverter has been developed to interface between an IF input and provide complex baseband outputs for use in the SETI breadboard system (see Fig. 1).

The SETI downconverter subassembly (see Fig. 2) has been built in a modular fashion with 13 modules in the SETI downconverter drawer and the required monitor and control and power supplies in a second drawer. The downconverter accepts both a 30-MHz IF (for use at an Arecibo receiver) and a 50-MHz IF (for use with a Block III DSN receiver). The 50-MHz IF is translated to 30 MHz in the downconverter. Two types of signal gain control are available: (1) an AGC loop with loop time constants of 0.1, 1, and 10 sec, and (2) a computer control gain control that offers a 35-dB dynamic range. An ADC is provided to measure the output of the AGC detector and is calibrated to provide an indication of output power. The IF signal is basebanded in the complex mixer where careful attention has been paid to the amplitude and phase balance between the two baseband signals (see Fig. 3). An internal test signal is available to allow stand-alone testing of the downconverter (and the SETI breadboard). The downconverter is controlled and monitored by a PDP 11/44 and is currently operating as designed in the development laboratory.

Table 1 is a list of the technical requirements and the measurements that have been made to confirm the downconverter performance.

Table 1. Downconverter requirements vs measured performance

Parameter	Requirement	Measurement
Input bandwidth	10 MHz	16 MHz
Input frequency	30 MHz 50 MHz Test signal	30 MHz 50 MHz 28 MHz
Baseband output	.1 VRMS	.1 VRMS
AGC dynamic range	>30 dB	50 dB
AGC time constant	0.1, 1, 10 sec	0.1, 1, 10 sec
Compute controllable gain range	⩾30 dB	35 dB (see Fig. 4)
Input impedance	50 ±5 ohm	58 ohm
Baseband frequency response	4 MHz	4.3 MHz
Rejection of unwanted harmonic	⩾30 dB	2nd harmonic = −46 dB 3rd harmonic = −52 dB
Phase and amplitude balance	90 ±3 0 ±0.5 dB	See Fig. 3 See Fig. 3
Linearity	Pin max ⩽−25 dBm	See Fig. 7
Noise figure	—	See Fig. 6
ADC power readout	—	See Fig. 5

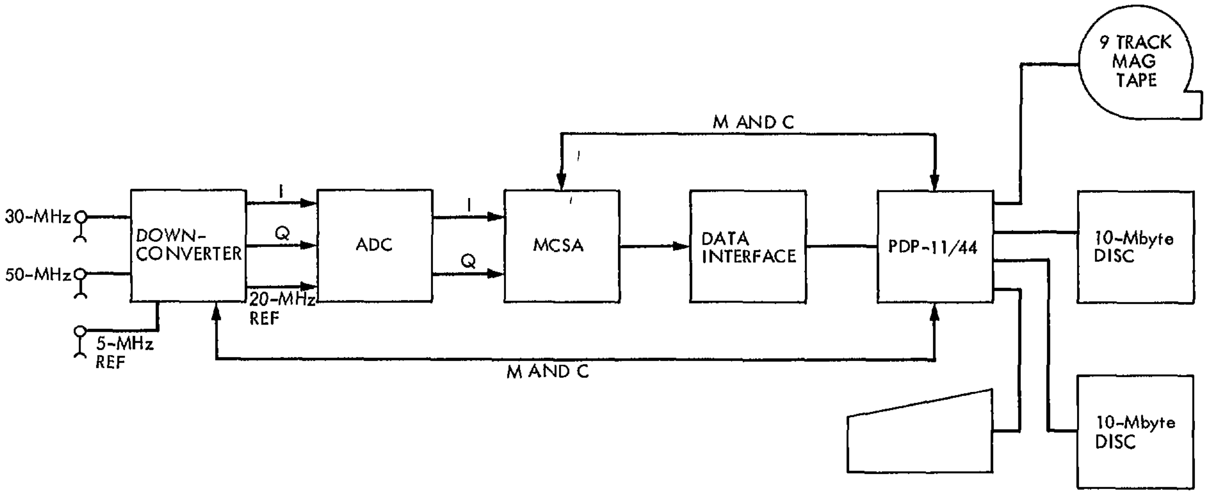

Fig. 1. SETI breadboard

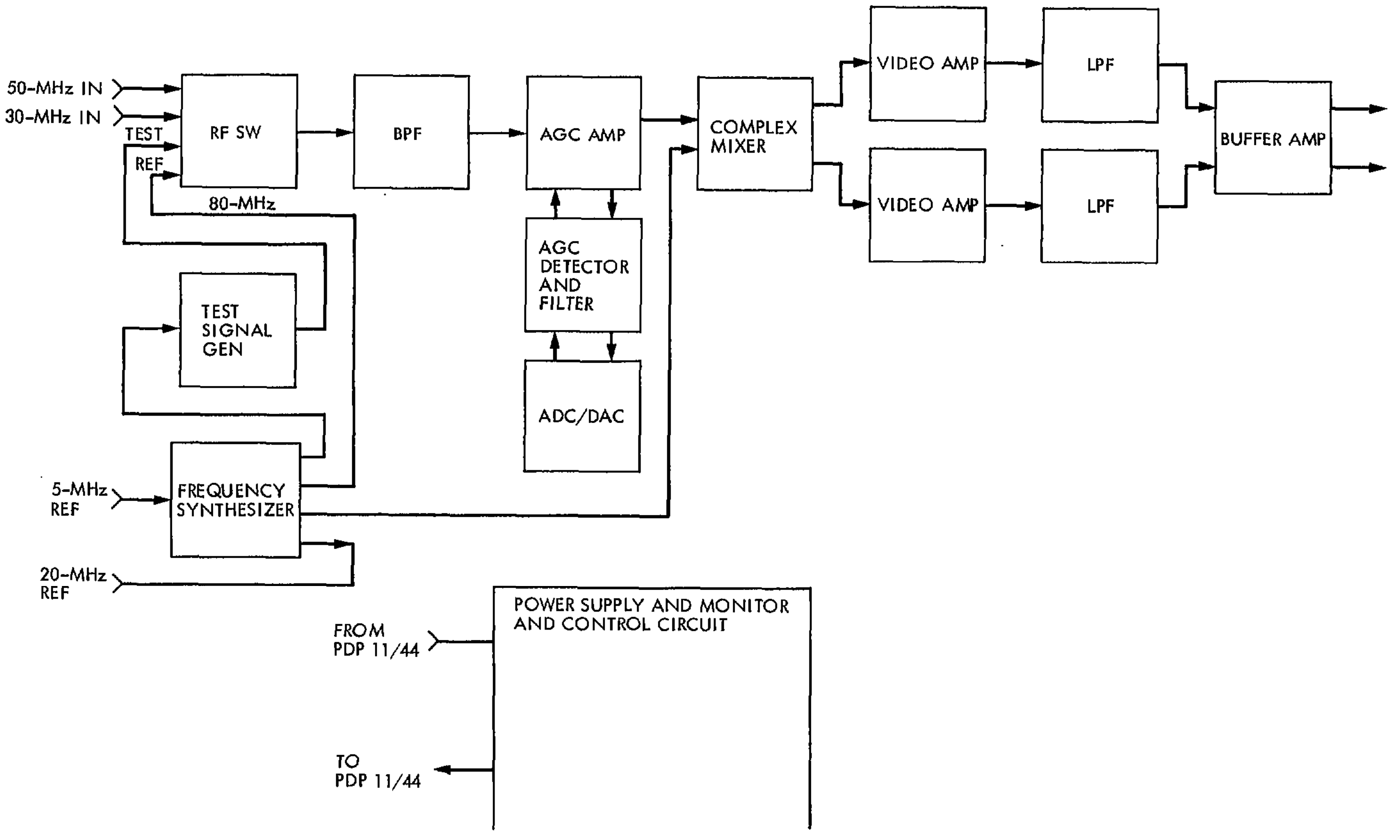

Fig. 2. SETI downconverter block diagram

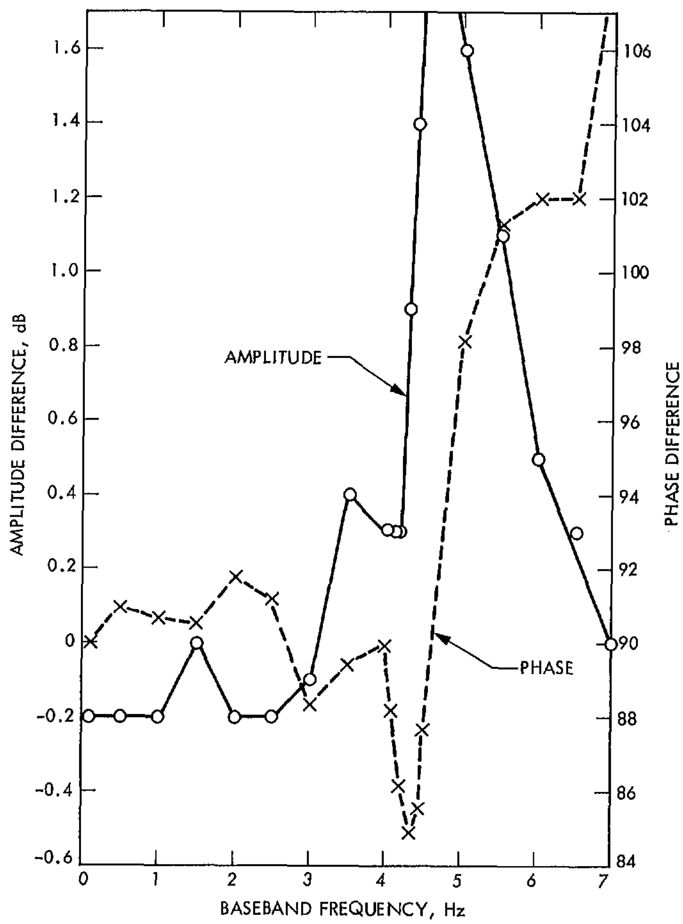

Fig. 3. SETI downconverter phase and gain balance vs frequency

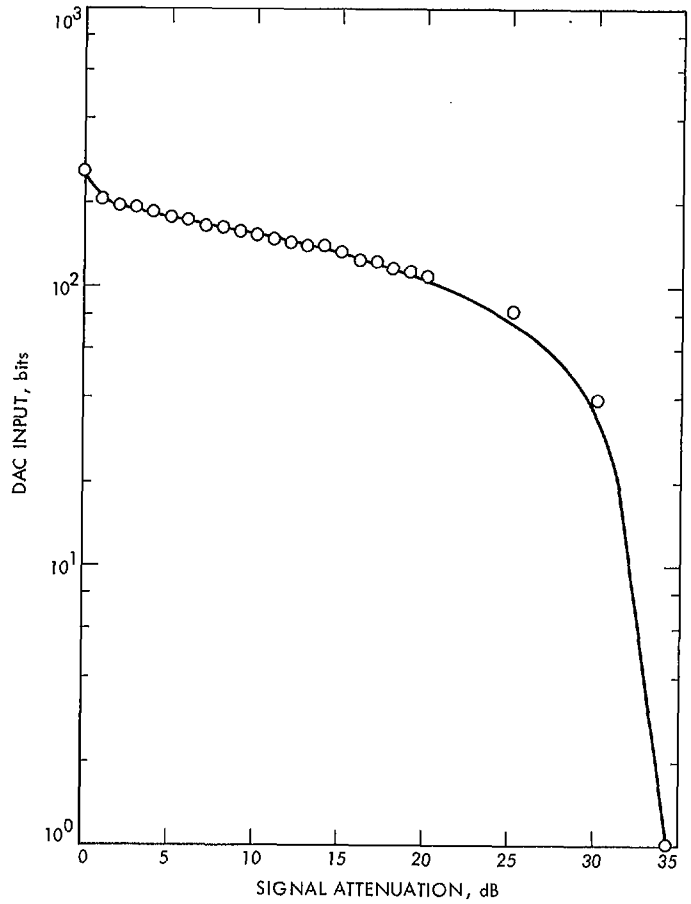

Fig. 4. SETI downconverter DAC input vs signal attenuation

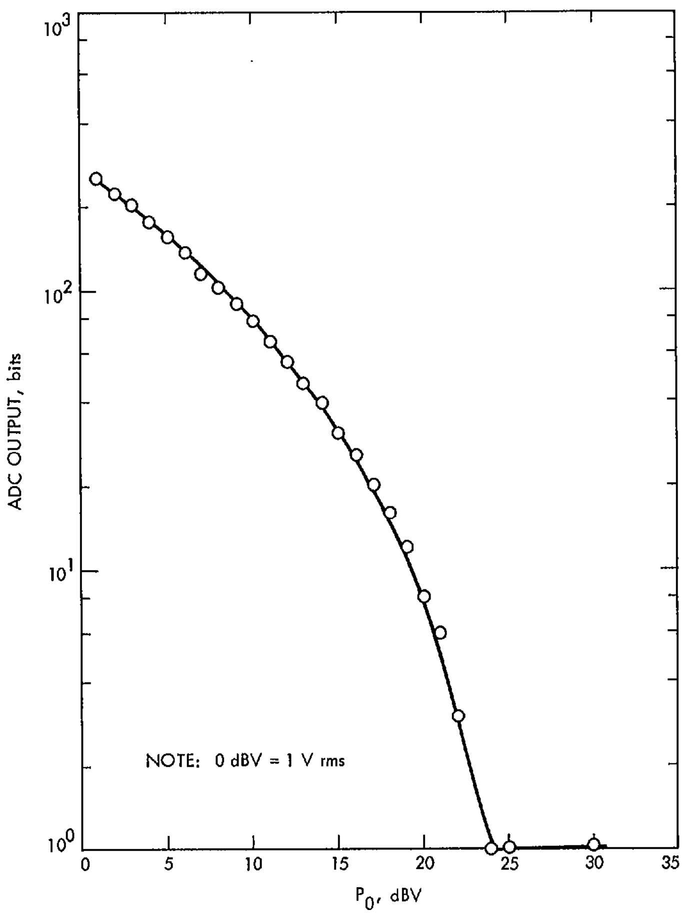

Fig. 5. SETI downconverter ADC output vs signal power output

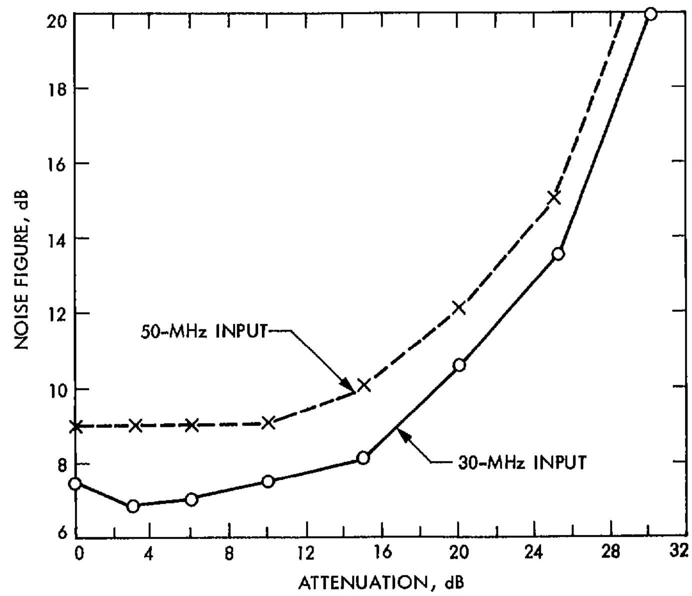

Fig. 6. SETI downconverter noise figure vs downconverter attenuation

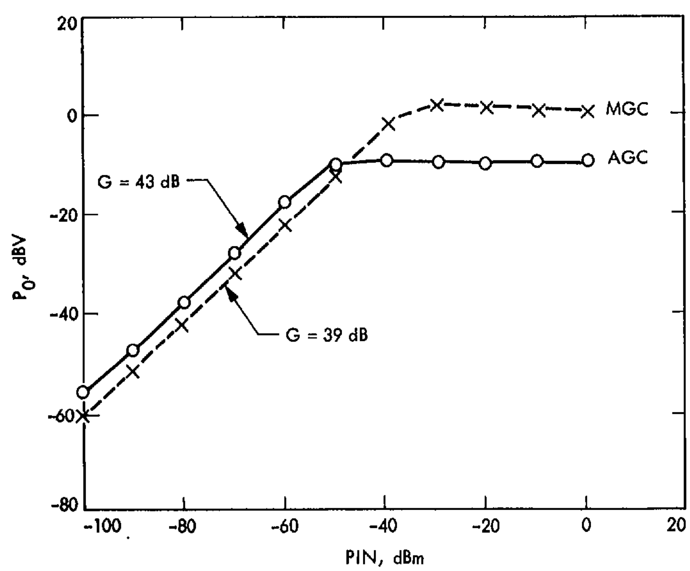

Fig. 7. SETI downconverter gain linearity for both AGC and MGC