A PPM Modulator and Demodulator for the 2.5-Bit/Detected Photon Demonstration

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The design and operation of a 256-ary pulse position modulation (PPM) modulator and demodulator is described. The unit is an integral part of the 2.5-Bit/Detected Photon Demonstration Program.

I. Introduction

The use of quantized pulse position modulation over the photon channel has been much discussed (Refs. 1,2) but little practiced. This article gives a functional description of a hardware PPM modulator and demodulator/analyzer which has been built for use in a 2.5-bit/detected photon, 256-ary PPM demonstration project (Ref. 3). The basic setup is shown in Fig. 1.

In addition to performing the basic pulse position modulation and demodulation, the hardware described also indicates the occurrence of erasures and errors of various types. The "analyzer" portion of the circuit counts the number of pulses received in a word, demodulates a second input pulse (if one is received), indicates the occurrence of erasures, and detects PPM word errors. Word errors are detected by comparing the modulator input word to the corresponding demodulator output. These functions are provided mainly for testing and diagnosis of the system during the feasibility demonstration period.

The hardware consists of two circuit boards (the modulator and the demodulator/analyzer) and a power supply in a single enclosure (see Figs. 2 and 3). The system was designed primarily for 8-bit (256-ary) PPM operation, but can be very easily modified for up to 12-bit (4096-ary) PPM operation. The maximum clock rate is 10 MHz (yielding 100-ns minimum slots), resulting in 256-ary PPM operation at up to

$$\frac{8 \text{ bits/word}}{256 \text{ slots/word} \times 100 \text{ ns/slot}} = 3.1 \times 10^5 \text{ bits/sec}$$

Hardware interfaces are at TTL logic levels – external circuitry must be provided to drive the laser and to convert the photomultiplier output (typically 10-ns pulses corresponding to individual photon or noise counts) to the required "count detected" decision for each slot.

II. The Modulator and Demodulator Hardware

The modulator (Fig. 4) consists of a binary downcounter, a phase-locked loop clock multiplier, and a serial-to-parallel converter. The PPM output is a one-slot pulse, position-modulated over the 256-slot word time (slot 0 is first, 255 is last). Each

8-bit word transmitted is also hard-wired to the error detection circuit in the demodulator. The clock multiplier generates a slot clock running at 256 times the word rate, and also a one-slot-per-word synchronization pulse. Both signals are available at the front panel.

After passing through the laser, the optics, and the detector, the PPM pulse enters the demodulator as a logic "true" (actually a TTL '0') during the appropriate time slot. Erasure of the pulse in transmission or the introduction of noise may result in any number of slots being "true" during any given word time. In the demonstration setup, the timing from the modulator is wired to the detector circuitry and to the demodulator, bypassing the problem of slot and word synchronization at the receive end. The demodulator can be adjusted to account for any number of full slot delays (up to one word time) through the system.

The demodulator/analyzer (Fig. 5) consists of two demodulators each with a parallel-to-serial converter, a pulse counter and decoder, and an error detector. The error detector compares the 8 bits demodulated from the first input pulse received in a word to the 8 bits provided by the modulator. This tests the success or failure of the basic PPM modulation-transmission-demodulation sequence. Demodulation of the second input pulse received is provided for diagnosis of systematic errors in transmission. All outputs are available one slot time after the word ends.

The pulse counter output indicates the number of slots which were "true" during the previous word time. Decoded outputs are available to indicate erasures (0 pulses received), normal PPM (1 pulse received), and error conditions (2 pulses received and > 2 pulses received). In the demonstration setup, only the "single pulse received" output is used, to indicate an (assumed) normal transmission. In this case, a nondetected error occurs only when an erasure and one noise count occur during the same word.

III. Remarks

The hardware provides the desired functions of PPM modulation and demodulation. Additional features are provided to increase the usefulness of the hardware in testing the system prior to use. Flexibility is provided by keeping the immediate interface to the optical channel external to the modulator/demodulator hardware.

The optical transmission and detection components will be connected soon in preparation for the 2.5-bit/detected photon phase III (uncoded PPM) demonstration. In this phase of the demonstration, a setup similar to that shown in Fig. 1 will be used.

Reed-Solomon coded PPM (phase IV of the demonstration) will be possible using the same modulator/demodulator hardware, by encoding data given to the modulator and decoding the output from the demodulator. In this setup, final verification of the 2.5-bit/detected photon transfer efficiency (at a reduced error rate from that of phase III) is expected.

References

1. Pierce, J. R., "Optical Channels: Practical Limits with Photon Counting," *IEEE Transactions on Communications*, Vol. COM-26, No. 12, pp. 1819-1821, Dec. 1978.
2. McEliece, R. J., "Practical Codes for Photon Communications," *IEEE Transactions on Information Theory*, Vol. IT-27, No. 4, pp. 393-398, July 1981.
3. Lesh, J. R., Katz, J., Tan, H. H., and Zwillinger, D., "2.5-Bit/Detected Photon Demonstration Program: Analysis and Phase I Results," *TDA Progress Report 42-66*, Jet Propulsion Laboratory, Pasadena, Calif., pp. 115-132, Nov. 1981.

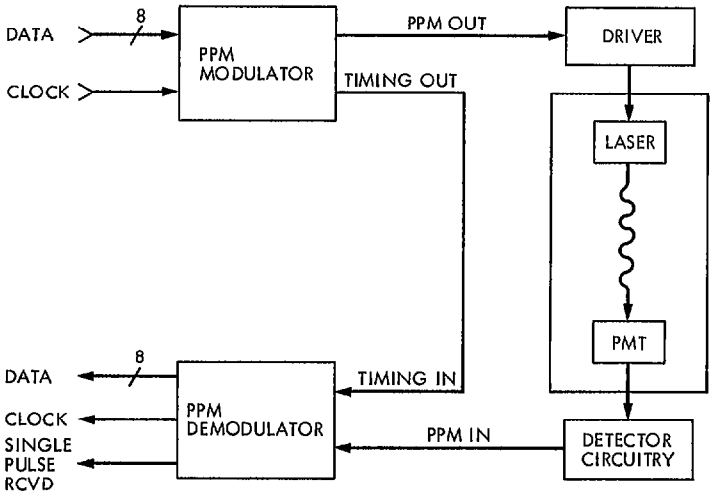

Fig. 1. Basic setup for the 256-ary PPM optical channel

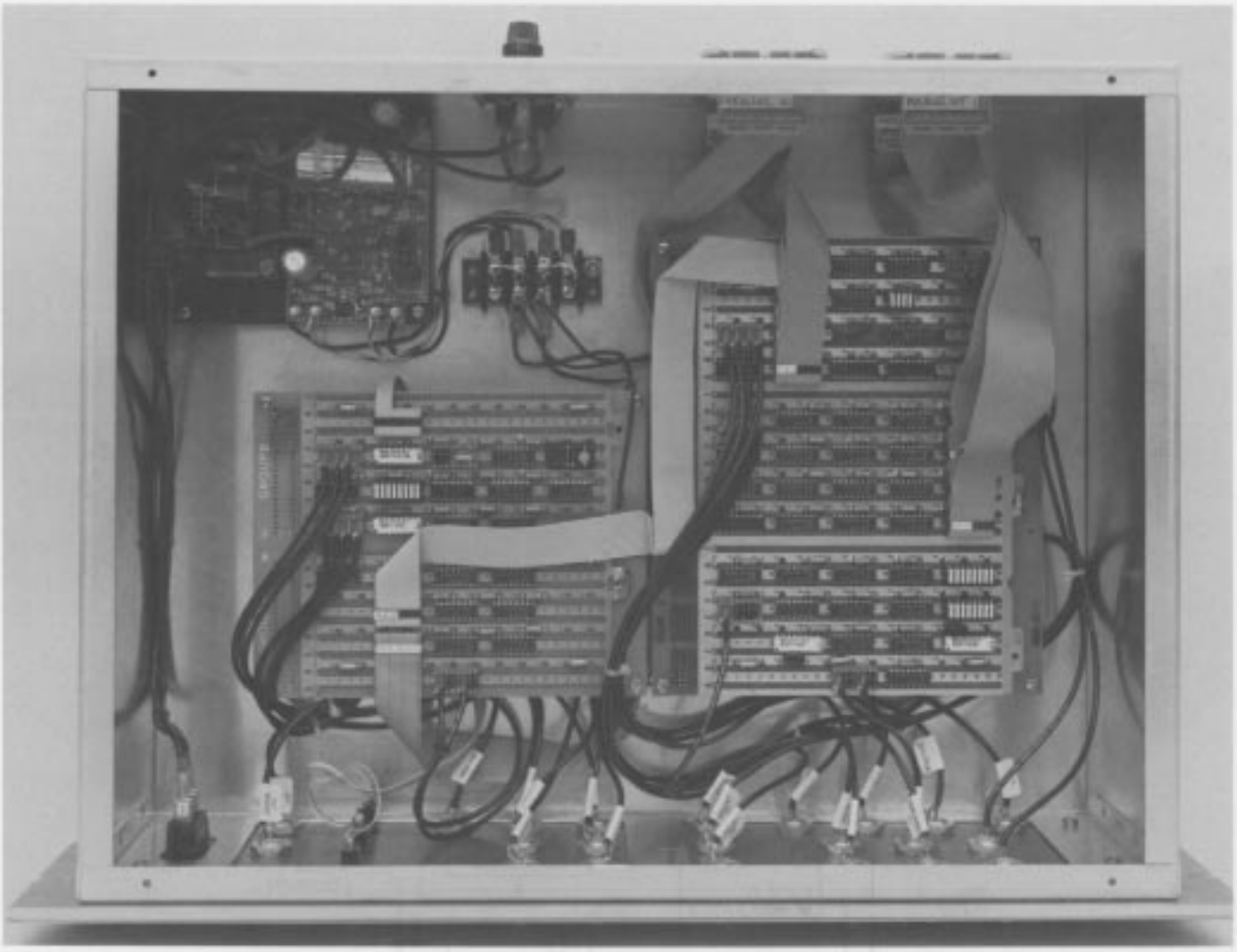

Fig. 2. Top view of the PPM modulator and demodulator hardware

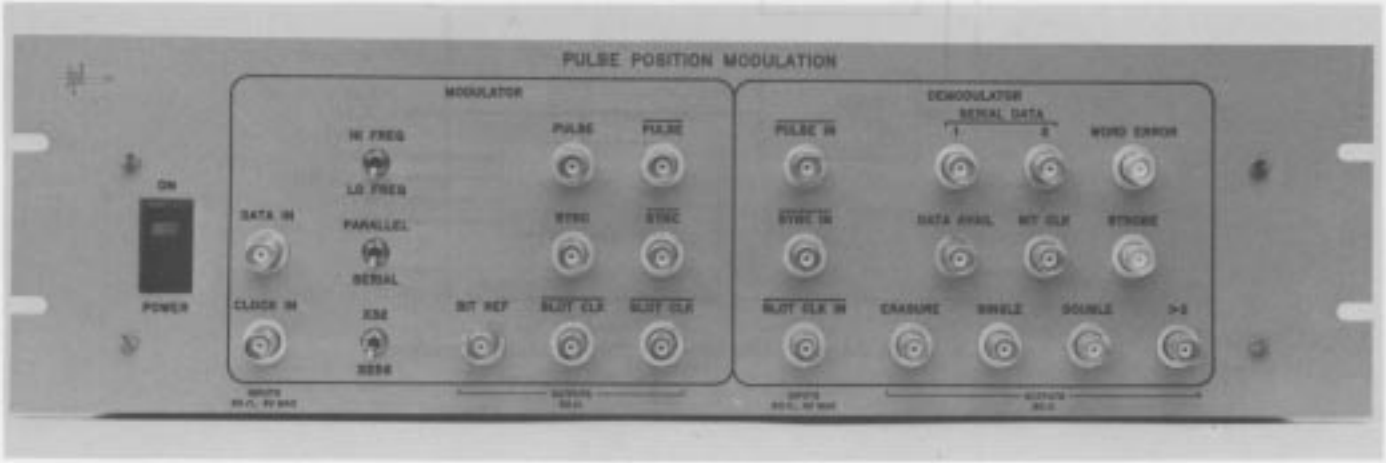

Fig. 3. Front panel of the PPM modulator and demodulator hardware

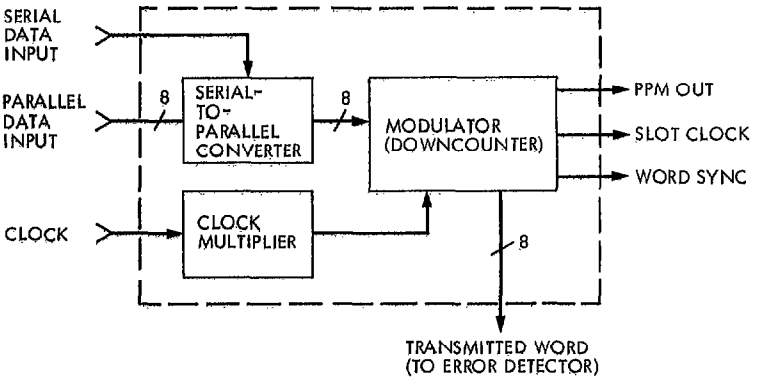

Fig. 4. Block diagram of the 256-ary PPM modulator

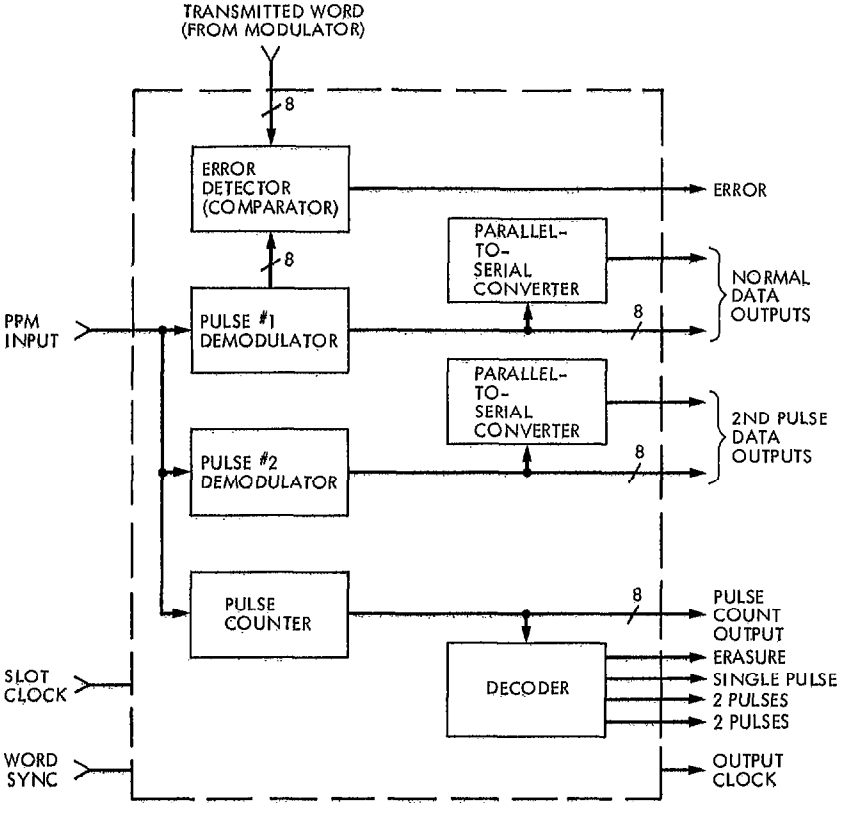

Fig. 5. Block diagram of the 256-ary PPM demodulator/analyzer