Polynomial Driven Time Base and PN Generator

S. S. Brokl
Communications Systems Research Section

In support of the planetary radar upgrade new hardware has been designed to increase resolution and take advantage of new technology. Included in this article is a description of the Polynomial Driven Time Base and PN Generator which is used for range gate coding in the planetary radar system.

I. Introduction

Digital data acquisition systems designed to receive data from artificial satellites and planetary objects encounter effects caused by the relative motion of these objects. The effects manifest themselves as a Doppler shift in the carrier frequency and a slight stretching or compressing of the information signal. The Doppler frequency shift is usually removed by heterodyning the incoming signal with a programmed local oscillator that removes the Doppler shift to the extent that it can be computed in advance of the observation. In many experiments, it is also desirable or essential to remove the effects of the time compression or expansion so that the signal samples remain in phase with the information baud rate. In the case of radar or pulsar astronomy, it is essential to perform this operation, since the non-deterministic signals are averaged over extended periods of time to reveal the statistical details of the signal. This article discusses the design and details of the operation of a new polynomial driven time base generator and PN generator. The PN generator is used in radar applications to form the original signal that is transmitted and to decode the received reflected signal. This particular design provides a timing precision of 20 ns over a period of one second. The time base system is designed to be updated at one second intervals from data computed from Chebyshev polynomials. During a given second, the time base is drifted linearly. Figure 1 is a block diagram of the planetary radar acquisition system that is currently being implemented. It shows how the Polynomial Driven Time Base and PN Generator fits into the system.

The Polynomial Driven Time Base and PN Generator (PDPG) is controlled by a VAX 11/780 computer via a Unibus DR11C interface. The PN generator runs at a 10 MHz chip rate derived from a 50 MHz clock and synchronized from a precision 1 second pulse (1PPS). PN coding is used as a form of pulse compression to give the best signal to noise ratio possible for planetary radar experiments.

Figure 2 is the block diagram of the Polynomial Driven Time Base and PN Generator. The PDPG consists of the following; a computer interface (via DEC DR11C Unibus interface), a precision programmed baud rate generator, a shift register with feedback, and a word detector with precision counter. The PDPG's primary function will be as the Radar Coder. The PN codes that were chosen are maximal length codes that yield an optimum correlation function with mini-

mum side lobes and give the lowest signal to clutter ratio. The coding allows precision range determination modulo for the duration of the code.

II. Computer Interface

The main interface to the VAX 11/780 computer for the Radar Coders is a Unibus DR11C (Ref. 1). The DR11C requires three address locations for operation on the Unibus. Address XXX0 is DRCSR (DR11C Control and Status Register). The second address location can be used as a read/write port and is being used for write only. The third address location is for read only and is being used for the purpose of reading back the coder internal registers.

Figures 3 and 4 are the formats and functions of the Coder Internal Control and Status Register (ICSR) and functional hold registers. The DR11C CSR bits CSR1 and CSR0 are used to control the mode of operation in read/write to DR11C addresses. With both CSR1 and CSR0 equal to zero, addresses 2 and 3 write or read from the ICSR in the coder. With CSR1 = 0 and CSR0 = 1, addresses 2 and 3 write and read from the registers pointed to by the ICSR. The register pointer within the ICSR can be set to auto increment on read or write.

The ICSR is common to all four coders. When writing or reading, all four coder ICSR registers respond. The interrupt mask bits 9, 10, 11, 12 are unique to each coder and use open collector output drivers to eliminate interference. The "Clear Interrupt" is decoded to clear only the interrupt pointed to by the coder select bits 6, 7. Interrupt A (INTA) on the DR11C is used by Request A (REQA) from the Coders. Because an interrupt could occur prior to enabling the interrupts, all interrupts should be cleared initially before enabling the interrupts on the DR11C interface (INT ENB A). The Word Counter is disabled after an interrupt and will not run until the next 1PPS. The interrupt should be cleared before the next 1PPS time.

As can be seen in Fig. 4, the coder has a number of internal registers for controlling the baud rate generator, setting the maximal length PN code, and controlling the word detect. The Word Counter keeps the time delay in clock pulses from the one second pulse until word detect. The word counter output is read on registers 6 and 7 which are read only types.

III. Precision Programmed Baud Rate Generator

The Baud Rate Generator is used to set precisely the shift rate (chip rate) of the PN code generator which follows. At the heart of this generator is a divide by 4, 5, 6 counter which generates a normal 10 MHz clock, plus or minus one clock per generator rate. The Pre-Range (PRN) and Pre-Range Complement (PRNC) registers hold values which, in conjunction with an adder and feedback register, act as a Number Controlled Oscillator that controls the number of deletions or additions per second of pulses obtained by the divide 4, 5, 6 counter. By picking the correct values for PRN and PRNC, a precise number of clocks can be generated during a one second interval. This slewed clock is used for tracking time shifts in the returned signal caused by the relative motion between the object and the earth observer. The PRN register holds the value of the increment and the PRNC register holds the 2's complement of the increment plus the clock frequency. The Number Controlled Oscillator works by initially loading the PRNC value at the 1PPS time and adding the PRNC to zero which is contained in the feedback register. At the first clock after the 1PPS time, the PRN value is presented to the adder and the value in the adder is loaded into the feedback register. From this point on, PRN plus the last value in the feedback register is continuously added with each clock pulse until A is greater than B in the comparator. The B side of the comparator is set with switches to a value equal to the clock frequency, i.e. 10 million. At that point PRNC is again presented to the adder and the cycle repeats continuously until the 1PPS time. At the 1PPS time the feedback register is again zeroed and a new value from PRNC and PRN is loaded.

The Word Counter is read to determine the phase of the PN Code Generator. A new value for PRN and PRNC can then be calculated and loaded at the next 1PPS time to correct the phase.

The divide by N and divide by M counters set the baud rate for the PN Generator. The SMPL signal is used by the Demodulators for over-sampling the incoming signals. The output of the divide by M counter is the shift clock to the PN generator. The values of N and M are program-selectable with the SPL and SPLB register.

IV. Pseudorandom Code Generator

The PN generator consists of a feedback shift register, a word comparator, and a phase counter. The basic PN generator is made from the shift register and parity feedback network. The feedback taps are selected by Programmable Read-Only Memory (PROM). Maximal length codes up to length 2^{24} can be selected by addressing the PROMs.

The word detector and counter are used to determine the precise time elapsed from the detection of an all 1's state within the coder following the 1PPS signal. The word length PROM stores the all 1's state and the shifted sequence just prior to

the all 1's for a maximal length code. Since the radar echoes are returning from planetary distances (i.e., Venus, Mars, etc.) with round trip light times of 8 minutes or more, it is important to know which echo is being received at any instant in time. Without precise timing, range information contained in the returned signal could not be extracted. The word counter holds the number of 50 MHz clocks which occurred between the 1PPS and the word detect. The word detect stops the counter and generates an interrupt so the value can be read by the computer.

V. Conclusion

The PDPG operates with two input clocks 10 MHz and 50 MHz and a 1PPS input signal, all coherent. Additionally it is programmable via a Unibus DR11C interface from a VAX 11/780 computer. The PDPG can operate with maximal length PN codes of 2 through 2^{24}. The time phase can be tracked to plus or minus 20 ns over the entire code length. Four PDPG modules are being built for the planetary radar system upgrade.

Acknowledgments

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References

1. *DR11C General Device Interface User's Manual* Digital Equipment Corp., Maynard, Mass., 1978.

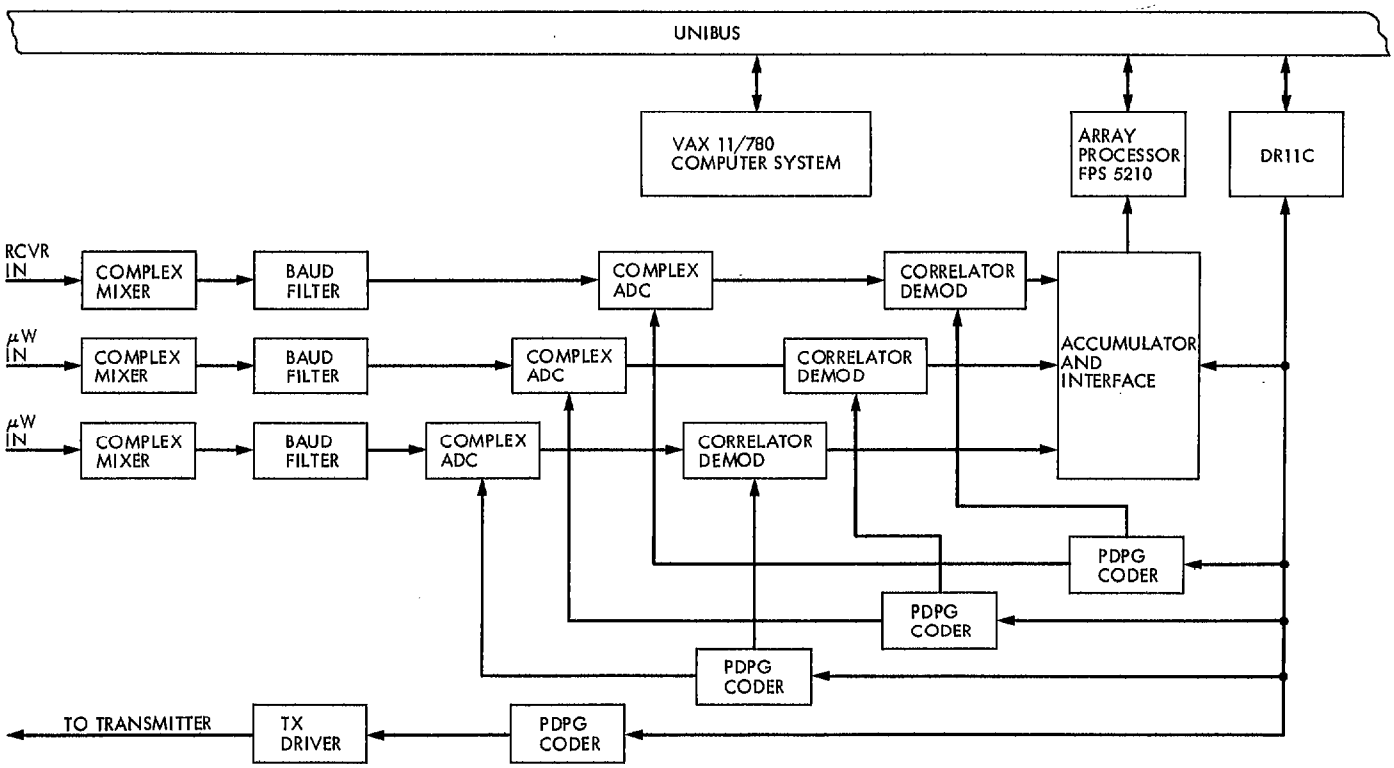

Fig. 1. High resolution radar system

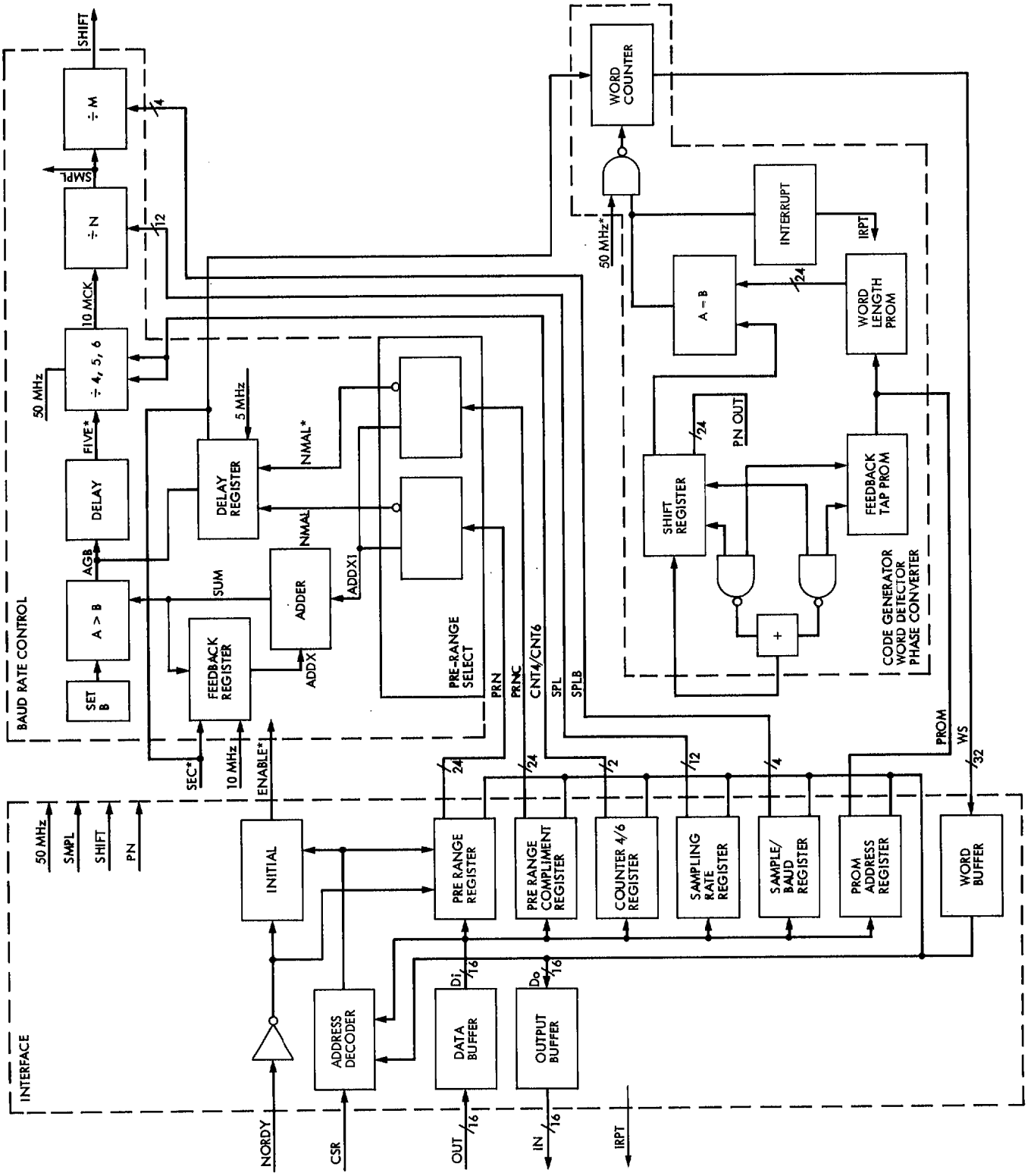

Fig. 2. Block diagram of the Polynomial Driven Time Base and PN Generator (PDPG)

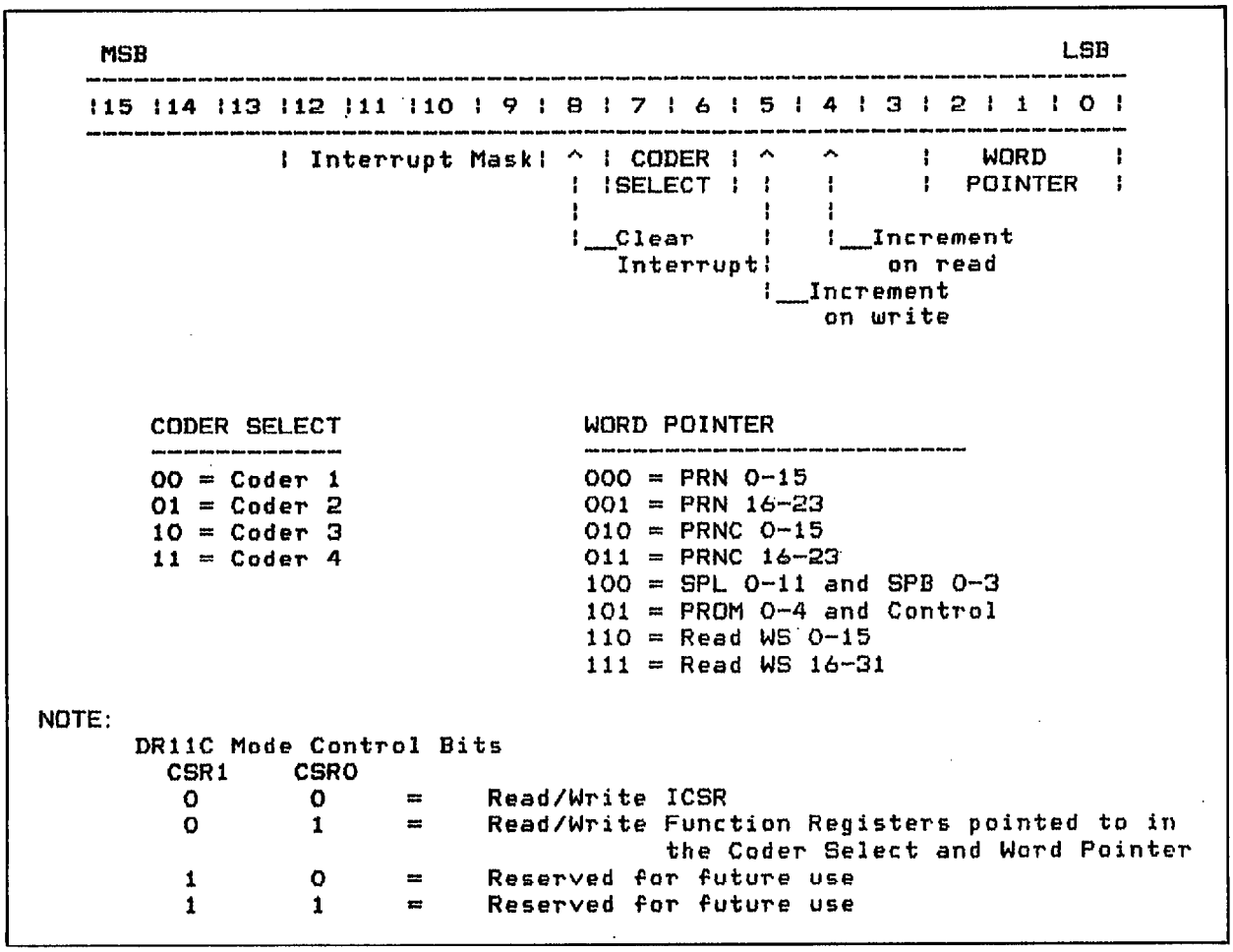

Fig. 3. Coder Internal Control and Status Register (ICSR)

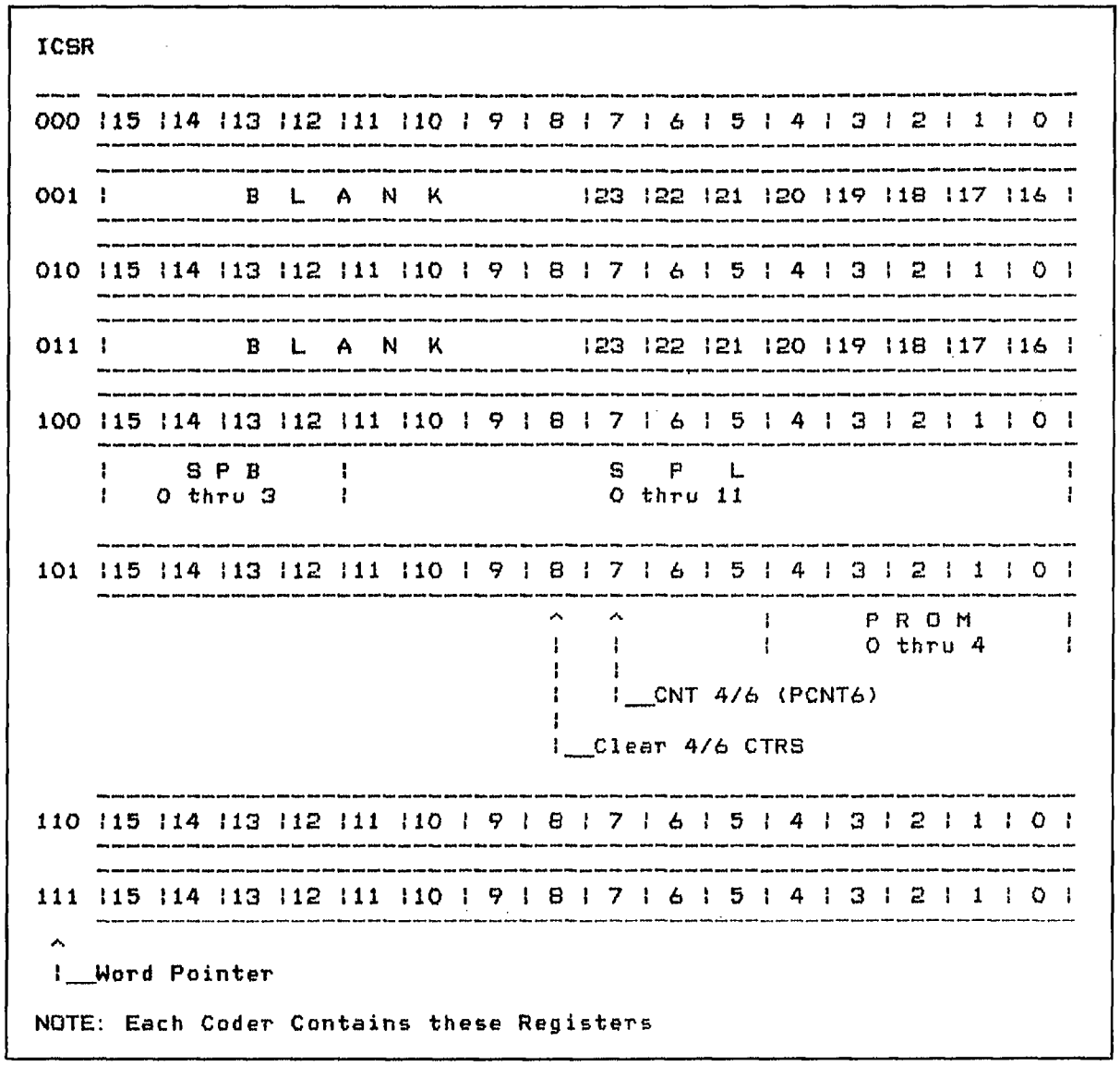

Fig. 4. Function register formats