Loop Gain and Circuit Parameters for Residual Carrier Tracking in the Advanced DSN Block V Receiver

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This article presents a circuit level analysis for residual carrier tracking of a deep space network signal by a proposed Block V receiver as conceived by the Receiver Advanced Development Team. The objective is to aid the circuit designer in selection of loop parameters to achieve the required performance objectives.

The topics specifically addressed are (1) loop stability and gain requirements, (2) loop component parametric equations, and (3) phase detector technology.

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The topics specifically addressed are as follows:

Loop Stability and Gain Requirements

- Oscillator Stability
- Loop Noise and Signal-to-Noise Ratio
- Doppler and Required Loop Gain
- Need for Coherent AGC and Gain Allowance

Loop Component Parametric Equations

- NCO (Frequency Synthesizer Method)
- Frequency Translation and Multiplication
- Phase Detector
- Analog-to-Digital Converter
- Digital Loop Filter
- Loop Compensation and Filter Frequency Response

Phase Detector Technology

Conclusions and Recommendations

The system analyzed is that of Fig. 1 which is believed to be the latest configuration for Block V.

I. Loop Stability and Gain Requirements

The loop gain requirements for a residual carrier tracking loop can be determined by analyzing the stability of the phase detector input signals. The carrier signal to be controlled is characterized by

$$S(t) = \sqrt{2P}\,[1 + \mathrm{a}(t)]\,\sin\,[\omega_o t + \psi(t) + d(t)] \qquad (1)$$

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where $a(t)$ represents amplitude noise. $\psi(t)$ includes phase and frequency noise of the received signal and 2.3 GHz L.O. (see Fig. 1) as well as modulation. In the last term, $d(t)$ represents doppler and other relatively long-term drifts such as circuit aging and temperature effects. The other input to the phase detector—the local reference signal—can be characterized similarly to Eq. (1) and includes noise and drifts of components within the hydrogen maser frequency standard and external multipliers.

A. Oscillator Stability

The problem of oscillator noise has been analyzed by Spilker (Ref. 1) for three sources: frequency flicker noise, white frequency noise, and white phase noise. The phase noise spectral densities were assumed to be K_a/f^3, k_b/f^2, and k_c, respectively, where the proportionality constants are specific to a particular oscillator technology.

For a linear model of the loop, the variance of the phase error is

$$\sigma_\epsilon^2 = \int_0^\infty \phi n(\omega) \mid 1 - H(j\omega) \mid^2 df$$

where $\phi n(\omega)$ is the spectral density of the noise and $1 - H(j\omega)$ gives the loop error function.

Based on the transfer function of a second-order PLL with damping $\zeta = 1/\sqrt{2}$ the residual phase variances

$$\sigma_{\epsilon_i}^2$$

are 8.71 $k_a/{b_n}^2$, 0.179 K_b/B_n and $K_c f_h$, respectively, where B_n is the one-sided loop noise bandwidth and $f_h >> B_n$ is the bandwidth limit imposed by IF filters.[2] Also quantization noise for the Numerically Controlled (digital) Oscillator must be included. The mean square noise for linear quantization is

$$\sigma_q^2 = \frac{q2}{12} \tag{2}$$

where q is the quantum step size. The noise contribution from each mechanism is summed to give a total phase error variance of

$$\sigma_\epsilon^2 = \sigma_a^2 + \sigma_b^2 + \sigma_c^2 + \sigma_q^2 \tag{3}$$

[2]For the DSN receiver this is the post phase-detector low pass filter of 15 MHz bandwidth.

The variance of the phase error is related to frequency variance by

$$\sigma_\epsilon^2 = (2\Pi)^2 \, T^2 \, \sigma_f^2 \text{ rad}^2 \tag{4}$$

where T is the measurement time period. The specified frequency stability $\Delta f/f$ will result in a frequency error of

$$\sigma_f^2 = \left[\frac{\Delta f}{f_o} (f_o)\right]^2$$

and, over time T, the variance of the phase error becomes

$$\sigma_\epsilon^2 = (2\Pi \Delta f T)^2 \tag{5}$$

B. Loop Noise and Signal-to-Noise Ratio

Receiver noise within the loop bandwidth B_n will contribute to uncertainty in the loop phase estimate. This can be viewed in terms of a noisy phase detector output voltage or in terms of the frequency uncertainty of the NCO output due to noise modulation.

The receiver noise in the tracking loop can be specified in terms of the carrier-to-noise power ratio, C/N. For a minimum carrier signal defined as that level for which $(C/N)_L$ = 10 dB in the two-sided loop noise bandwidth $2B_{L_o}$, then the worst case C/N at the analog-to-digital converters will be approximately

$$(C/N)_{ADC} = \frac{2B_{L_o}}{2B_{LPF}} (C/N)_L = \frac{0.1 \text{ Hz}}{2(15 \text{ MHz})} (10) \rightarrow -74.8 \text{ dB}$$

where B_{LPF} is the bandwidth of the phase detector output low-pass filter. This value ignores quantizing noise from the proposed 6-bit ADC's (see Eq. [2]) as well as other digital processing noise.

The phase detector input C/N corresponding to the above assumptions and ±250 MHz IF bandwidth would be $(C/N)_{PD}$ = (0.1 Hz) (10)/500 MHz = −87 dB. This IF bandwidth could be limited to, say, 40 MHz since the post detection bandwidth is 15 kHz or less. Then $(C/N)_{PD}$ = −76 dB. In any case, the phase detector will be expected to operate at signal-to-noise ratios substantially below what is conventionally considered to be a threshold value, about −30 dB (Ref. 2). This issue will be explored in a later section on phase detector technology.

C. Doppler and Required Loop Gain

The major determinant of loop gain is based on maintaining a loop phase error of less than 2° (1° goal) during maximum

doppler frequency shifts. Carrier frequency shifts of up to Δf_d = 100 kHz are expected but doppler dynamics are not expected to pose any problems for the tracking loop.

Based on a linearized loop model in which the static phase error θ_e is maintained at less than 0.1 radians (5.7°), the open loop gain (uncompensated loop) at ω = 1 rad/s is given by

$$K_v = \Delta\omega/\theta_e \tag{6}$$

In order to reduce the loop phase error to 1° (0.0175 rad) for a 100 kHz doppler frequency shift, the loop gain must exceed

$$K_v \geq 2\Pi\, \Delta f_d/\theta_e(\max)$$

$$= 35.9 \times 10^6 s^{-1}$$

$$= 151 \text{ dB at } \omega = 1 \text{ rad/s}$$

This value, of course, assumes a stand-alone loop with no external intervention.

D. Need for Coherent AGC and Gain Allowance

Equation (15) for phase detector gain (Section II.C) shows that the *PD* gain and therefore the system loop gain and bandwidth are proportional to the residual carrier power. This has a couple of consequences for the system design.

First, a low modulation index is required during the residual carrier tracking mode. For a peak phase deviation of θ_m = 1.57 radians with square-wave modulation, the carrier power is zero (see Eq. [14]). A reasonable upper bound might be $\theta_m \leq 1$ rad for which the residual carrier power will be only 5.3 dB less than the total received signal power.

A more important consideration, however, is that while limiters or noncoherent AGC can maintain the noise power into the phase detectors constant for ADC scaling, loop gain and bandwidth will vary with received signal dynamic range. Coherent AGC is required to maintain a constant *carrier* power at the phase detector input.

Since both in-phase and quadrature phase detectors are present in the advanced receiver design it is a simple matter to take the coherent AGC voltage from the inphase (I) detector which acts as a coherent full-wave rectifier (when θ_e = 0). Peak detection of the carrier is then attained by sampling and filtering the I-detector output.

The coherent amplitude detection characteristic of an in-phase phase detector with high input SNR[3] is proportional to

$$\sqrt{2P_c}\, \cos\theta_e \tag{7}$$

Consequently, increasing PLL phase error will cause a decrease in AGC loop gain given by (AGC Voltage Loss),

$$L = 20 \log \cos\theta_e \tag{8}$$

During doppler events the PLL phase error increases. If the dynamics of this process are ignored then we have only to insure that the loop gain is high enough to hold the receiver AGC within specifications.

If the AGC is allowed to vary by 0.5 dB, then the PLL static phase error can increase to $\theta_e = \cos^{-1}(10^{-L/20})$ = 0.336 rad (19.3°). For a worst case doppler of Δf_d = 100 kHz, loop gain (from Eq. [5]) will have to be at least $K_v \geq 2\Pi 10^5/0.336 \rightarrow 125$ dB. Of course, the designated loop gain of 151 dB (Section I.C) will insure that AGC variations due to PLL phase error (1° max) will be 19.3 times better than the specification limit.

II. Loop Component Parametric Equations

The simplified residual carrier tracking loop of Fig. 2 delineates loop components and their gain parameters. In this section a parametric expression is determined for each block's contribution to the PLL loop gain. This will allow for the calculation of the overall open loop gain as well as shedding light on the various parameter choices.

A. NCO, Frequency Synthesizer Method

The proposed Numerically Controlled Oscillator is illustrated in Fig. 3. Here, the value of the output frequency (unlocked PLL) or phase (PLL locked) is generated in the accumulator. The accumulator is updated periodically at a rate determined by the stable clock reference frequency f_{ck}. The numerical contents of the accumulator increase in the value for each cycle of the clock. The value of N determines the amount by which the numerical contents increase each clock as illustrated in Fig. 4.

The maximum numerical contents of the accumulator is $M = 2^b$ where b is the number of bits used. Therefore the accumulator will overflow and change output state each time

[3] In order to insure an AGC loop SNR > 10 dB this loop will have to be at least as narrow as B_{L_o} = 0.1 Hz.

M is exceeded. As seen in Fig. 4, the accumulator output frequency will be

$$f_A = \frac{N}{M} f_{ck} = \frac{N}{2^b} f_{ck} \tag{9}$$

which is linearly proportional to the input number N.

The loop gain parameter K_o (and resolution) for the NCO is determined as the frequency deviation Δf_o per change in input number N.

$$\Delta f_o = \frac{N}{2^b} f_{ck} - \frac{N \pm 1}{2^b} f_{ck} = \frac{\pm f_{ck}}{2^b} \tag{10}$$

Hence,

$$K_o \triangleq \frac{\Delta f_o}{N} = \frac{f_{ck}}{2^b} \tag{11}$$

As a typical example, a 32 bit accumulator and 10 MHz clock will give the NCO a sensitivity (and resolution) of $K_o = 10^7/2^{32} = 0.0023$ Hz/numerical value of N.

B. Frequency Translation and Multiplication

The NCO output frequency must be multiplied and translated up to a nominal frequency for the first mixer (2.3 GHz in this case). The translation component of this process will be performed by high-level mixing with an ultrastable reference frequency derived from the maser frequency standard. As such the effect on loop gain and stability will be possibly a multiplication of plus or minus one.

The times-M ($\times M$) multiplication component of this block is needed to increase the deviation sensitivity of the NCO thereby increasing the system open loop gain. The multiplication factor is the gain parameter for this circuit

$$K_m = M \tag{12}$$

M is usually determined after the other loop gain parameters are known since it is typically the most flexible and technologically achievable parameter. The major constraint on M is frequency stability.

As pointed out by Tam and Armstrong in a preliminary report entitled "Description of Block V Receiver Signal Processing Assembly with Technology Assessment" (personal communication), a commercial frequency multiplier with good thermal regulation has demonstrated "a stability of 3×10^{-16}, $\tau = 1000$ s."

C. Phase Detector

The phase detector seems at this point to be the weak link if not the Achilles' heel of the tracking loop. A search of the literature and data sheets (with telephone follow-up) indicates that there is not an off-the-shelf unit available which meets the specifications of 800 MHz ±40 MHz input with an output voltage range of ±2.5 V and 35-40 MHz bandwidth, not to mention output offset voltages of less than "a few tens of microvolts."

I have no doubt that a custom unit is quite feasible. It will be a single-balanced mixer design with an output balance potentiometer and approximately 1 KΩ output impedance. This issue is discussed in some detail later (Section III).

The analog phase detector of block diagram Fig. 2 has as inputs an 800 MHz IF signal including the phase estimate θ from the NCO-XM and an equal frequency reference signal f_{ref} derived from the maser frequency standard. The transfer function of the phase detector is

$$V_d = \sqrt{2P_c} \sin \theta_e \tag{13}$$

where P_c is the residual carrier power and θ_e is the loop phase error. The residual carrier power as a function of modulation index θ_m for a unit power squarewave modulation subcarrier is

$$P_c = P \cos^2 \theta_m \tag{14}$$

where P is the total power.

Since the loop will track the carrier with low phase error, the phase detector gain is just the slope of Eq. (13) at the origin. That is,

$$K_\Phi \triangleq \frac{dV_d}{d\theta_e} = \sqrt{2P_c} \text{ V/rad} \tag{15}$$

A typical value of phase detector sensitivity for high-level inputs is 0.5 rad/V. Unfortunately, most of the input in our application is noise so K_Φ will be low.

D. Analog-to-Digital Converter (ADC)

The ADC samples the phase detector output $V_d(t)$ and quantizes it into a numerical estimate $V_d(n)$. $V_d(n)$ is more commonly written as $X(n)$, X_n or X_k.

The output of the phase detector is essentially all noise with SNR = -75 dB (Section I.C) at the operating threshold defined as +10 dB SNR in $2B_{L_o}$ = 0.1 Hz. The $3\sigma_n$ noise peaks are scaled to ±2.5 V for input to the ADC and held constant by bandpass limiting or noncoherent AGC. If the number of bits used for linear quantizing in the ADC is a, then the ADC gain constant is

$$K_{\text{ADC}} \triangleq \frac{\Delta n}{\Delta V_d} = \frac{2^a}{6\sigma_n} \tag{16}$$

which for a = 6 bits and a full sampler input range of 5V pk-pk will be $2^6/5$ V = 12.8 numerical values per volt.

E. Digital Processing and Loop Filter

The phase detector output samples are taken at a very high rate (about 30M samples/s) compared to the expected tracking dynamics (kHz range). These noisy samples are accumulated (perhaps an Accumulate and Dump operation) and averaged to form a reduced rate sequence of numeric values which approximate the loop phase/frequency error. The static gain of this digital filter can be scaled to unity if desired so that it would have no effect on the loop gain computation.

Figure 5 is a block diagram of the second order loop filter implemented digitally. G_1 and G_2 are filter constants and the z-transform parameter z^{-1} indicates a 1-bit delay. For a third order loop an additional block is added (dashed) implementing $G_3/(1 - z^{-1})$.

For the purposes of computing the system parameter K_v ("velocity constant"), the static gain of the loop filter is G_1 and for the overall digital processing gain is K_F.

The loop filter output for updating the NCO phase/frequency is $z(n)$. As indicated in the system block diagram of Fig. 2, a numerical value N_o is set which establishes the center frequency of the NCO. This numerical value is incremented by the digitally processed numerical estimate of the phase and frequency error from the summing junction, $y(n)$. $y(n)$ is the sum of the Residual Carrier Error (RCE) and the Suppressed Carrier Error (SCE) where either may be zero depending on the data transmission mode.

More work needs to be done in the digital processing area to better define the parameters and their effects on loop gain and dynamics.

F. Loop Compensation and Loop-Filter Frequency Response

Tracking loops for receivers are usually compensated for damping factor ζ between 0.5 and 1.5 where $\zeta = 1/\sqrt{2}$ is most common. Lead-lag compensation allows for the independent setting of loop gain, bandwidth and damping.

For the advanced receiver design the digital loop filter will provide the loop compensation. Figure 6 illustrates the open loop frequency response where the simple pole at ω_p (= $1/\tau_1$) and zero at ω_z (= $1/\tau_2$) are set by the frequency response of the digital loop filter. For $\zeta = 1/\sqrt{2}$ and a desired one-sided loop bandwidth of B rads/s, the zero should be approximately one octave below B. That is,

$$\omega_z = B/2 \tag{17}$$

If the 40 dB/decade line ($1/s^2$) is projected from ω_z to the K_v = 1 axis, the intercept is at $B/\sqrt{2}$. Hence, the $\zeta = 1/\sqrt{2}$ compensated open-loop response between ω_p and ω_z is on a slope given by

$$40 \log \frac{B}{\sqrt{2}\,\omega} \tag{18}$$

The pole ω_p must be placed at that frequency for which the $1/s^2$ and K_v/s curves intersect. In log notation for Bode plotting, the K_v/s curve is given by

$$20 \log \frac{K_v}{\omega} \tag{19}$$

The solution for ω_p therefore is $B^2/2\omega_p^2 = K_v/\omega_p$, or

$$\omega_p = \frac{B^2}{2K_v} \tag{20}$$

The second order loop filter frequency response is equivalent to a lead-lag network with a pole and zero given approximately by Eqs. (17) and (20) respectively.

For the tracking loop with $\zeta = 1/\sqrt{2}$, B_{L_o} = 0.1 Hz, and K_v(dB) = 151 dB ($K_v = 35.9 \times 10^6$), the results are ω_p = 1.38×10^{-9} rad/s (0.22 nHz) and ω_z = 0.314 rad/s (0.05 Hz). For ζ = 1.5, ω_z is decreased by a factor of 1.65 and ω_p is decreased by 1.28.

The exact result relating damping factor, loop gain and compensation time-constants τ_1 and τ_2 is from Ref. 3, $\zeta = (1 + \tau_2/r\tau_1)\sqrt{r}/2 \approx \sqrt{r}/2$ where $r = AK\tau_2^2/\tau_1$. The approximation $\zeta \approx \sqrt{r}/2$ can be rewritten in my notation as $\zeta \approx \sqrt{K_v\ \omega_p}/2\omega_z$ which for $\zeta = 1/\sqrt{2}$ and $\omega_z = B/2$ yields Eq. (20). Failure to use the exact relationship of Ref. 3 for the high gain tracking loop will result in an error for the damping

factor of less than 9 parts per billion. The correction factors applied to ω_p and ω_z for $\zeta_x \neq 1/\sqrt{2}$ are computed from

$$x = (2\zeta_x^2)^{1/3} \tag{21}$$

where

$$\omega_p(\zeta_x) = \sqrt{x}\ \omega_p \text{ and } \omega_z(\zeta_x) = x\omega_z \tag{22}$$

III. Phase Detector Technology

The concerns of phase detector DC offset are explored in this section.

Commercially available phase detectors produced by mixer manufacturers come in two circuit configurations, i.e., the double-balanced mixer (DBM) of Fig. 7(a) and the single-balanced mixer (SBM) of Fig. 7(b). In addition, for completeness, Fig. 7(c) illustrates a second form of the SBM.

As analyzed in Ref. 4, circuit C can be dismissed immediately because of poor dc balance, low gain (about 9.9 dB less than circuit B), and limited output range because the transfer characteristic has flat tops for $V_d > V_D$ due to the discharge of the output capacitor C. Circuit B is a more conventional version of the SBM phase detector for which Eqs. (12) and (14) give the transfer function and gain assuming that the reference input $V_{ref} \gg \sqrt{2P_c}$. The analysis of Ref. 4 indicates best linearity and dc balance when the reference and input signals are equal. However, the circuit sensitivity will suffer by $\sqrt{2}$ as the transfer function becomes

$$V_d = \sqrt{P_c}\left[\sqrt{1+\sin\theta_e} - \sqrt{1-\sin\theta_e}\right] \tag{23}$$

which is a nearly triangular version of the sinusoidal characteristic of Eq. (12). Also, noise was not considered in the analysis although a reference oscillator or the VCO of a narrow bandwidth PLL will be expected to be relatively noiseless compared to the signal input. Consequently one would not expect a thresholding effect as exhibited in discriminators. The nearly triangular characteristic when operating with equal level inputs is advantageous for demodulator applications *and* where the nonlinearity of the sin θ_e detector becomes a problem in high-level input applications. The block V receiver qualifies on both counts.

The Varil PD 100 and PD 101 DBMs are redesigned version of the standard DBM. The redesign takes advantage of the sensible notion that developing a reasonably high output voltage requires using more than a 50 Ω load resistance. The PD 100-101 is designed for an output load of 500 Ω. As might be expected the dc offset is worse with the higher impedance. Indeed the equation from Ref. 5 (p. 83) must be modified to include $R_L \neq 50\ \Omega$. Also this equation, derived in Ref. 5, is already in error by $\sqrt{2}$ because in Eq. (19) (p. 83), $V_{IF} = \sqrt{50\ P_{IF}}$ gives the rms voltage whereas the $2V_{IF}/\Pi$ relationship for the full-wave rectifying due to poor isolation (IS) requires the *peak* V_{IF}. The modified and corrected expression is

$$V_{\text{offset}} = 6.4\ \sqrt{R_L/50}\ 10^{\alpha}$$

or

$$= 0.9\ \sqrt{R_L}\ 10^{\alpha} \tag{24}$$

where

$$\alpha = (\text{LO} - \text{IS} - 30)/20$$

and LO power is in dBm with isolation in dB.

As stated in Ref. 5, DBM's often have better isolation than SBM's and they always are superior with respect to third-order (and higher) intermodulation products which produce dc offset. However, SBM's are simpler; it's easier to match diodes and to maintain the match[4]. Also the dc offset voltage due to noise can easily be zeroed. Such a circuit is illustrated in Fig. 8. One such unit (PD 100-101) is guaranteed only to 500 MHz with a 1.5 MHz baseband width having ±2 V output range into 1 kΩ (+17 dBm RF input). While these specs don't match our application, it should be noted that they are guaranteed over a temperature range of -54°C to 100°C, and custom designs with reduced temperature requirements may achieve our specifications.

The double-balanced mixer approach is available from another manufacturer, Mini-Circuits. This unit is designed specifically for phase detector applications and isolation is greater than 50 dB. The dc offset is 200 μV typical (1 mV, max). The available unit is rated only to 100 MHz with a ±1 V output range into 500 Ω (+7 dBm input) but the baseband width is 50 MHz. DC balance zeroing is not practical with four-diode DBM's.

The SBM and DBM units available as phase detectors designed for relatively high impedance loads have absolute maximum input power ratings of +20 and +17 dBm, respec-

[4]This is especially important in high-level detectors because they may have more than one diode/branch (leg) or a diode and series resistor in order to reduce dissipation or breakdown effects.

tively. Indeed the high level mixers available from Avantek and Watkins-Johnson (Relcom Division) are rated to +27 dBm of LO input power. None of these devices can be driven with one Watt (+30 dBm).

IV. Conclusions and Recommendations

An analysis of the requirements for residual carrier tracking for the advanced DSN receiver indicates a minimum loop gain of 151 dB be used. This is based on maintaining a maximum loop phase error of 1 deg without external intervention.

The contribution to system loop gain for each loop component has been assessed and a parametric equation determined. This will aid the receiver designer in making the tradeoffs necessary to achieve the required loop gain.

Coherent AGC will be required in order to maintain loop gain and bandwidth over a large received signal dynamic range.

Concerns over phase detector thresholding effects due to large negative SNR's and dc voltage offset have been addressed. The findings suggest a custom design incorporating the single-balanced mixer configuration of Fig. 8. The suggested chopped reference solution can be used if necessary to further reduce the dc offsets. Indeed, since this is a technique similar to the chopped amplifier solution to dc stability, it suggests the use of an ac-coupled amplifier at the chopped phase detector output to obviate the question of obtaining ±2.5 V peak on noise.

As it is, attaining the required loop gain appears to pose a substantial challenge as the following calculation will attest:

$$K_v = K_\Phi K_{ADC} K_F K_o M \tag{25}$$

If the representative loop component gain values calculated in the text are used then K_v = 151 dB = 35.9 × 10^6 and the multiplication factor in the frequency translation section becomes $M \geqslant 35.9 \times 10^6/(\sqrt{2P_c} \times 12.8 \times K_F \times 0.0023 \times 2\Pi) = 137 \times 10^6/K_F \sqrt{P_c}$. Because of the negative SNR's, the carrier signal into the phase detector will be $\sqrt{2P_c} \ll 2.5\ V_{pk}$ and therefore the digital processing will be required to provide a considerable processing gain.

On the other hand the 151 dB of loop gain is based on requiring the loop to reduce, *without external intervention*, the loop phase error to 1 deg during a 100 kHz doppler frequency shift. External methods for reducing loop stress will be very important.

More work is needed to be done to better define the digital processing area of the tracking loop for better definition of the parameters which affect the loop gain and dynamics and some to overcome the lack of published research on microwave phase detectors.

References

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4. Ohm, G. and Alberty, M. "Microwave Phase Detectors for PSK Demodulators," *IEEE Transactions on MTT*, Vol. MTT-29, No. 7, July 1981, p. 724-731.
5. Kurtz, S. R., "Specifying Mixers as Phase Detectors," *Microwaves*, Vol. 17, No. 1, pp.80-89, Jan. 1978.

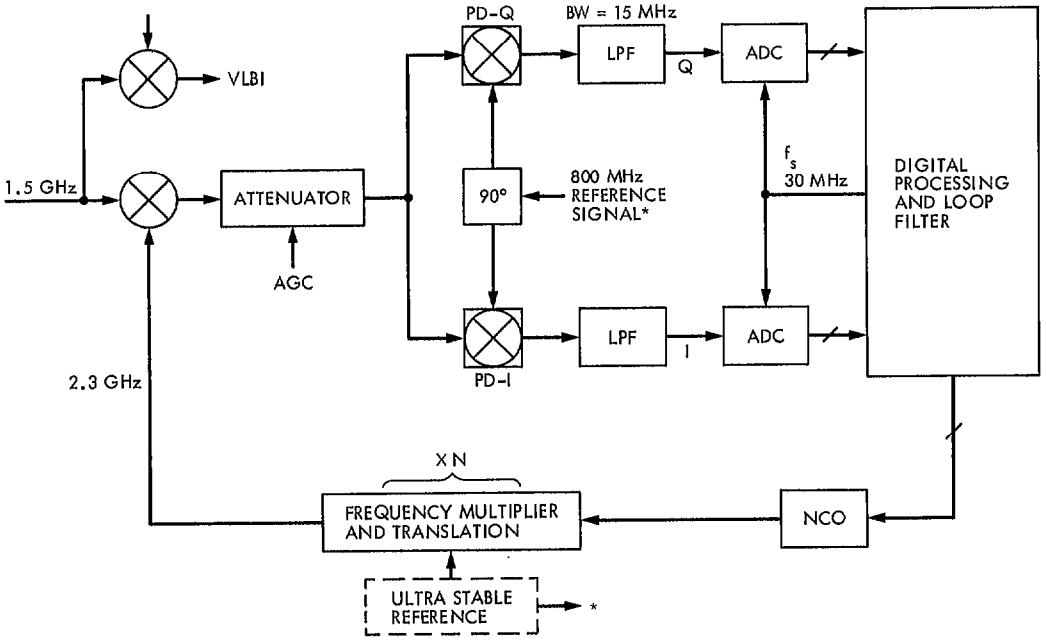

Fig. 1. Basic block diagram for the carrier tracking loop

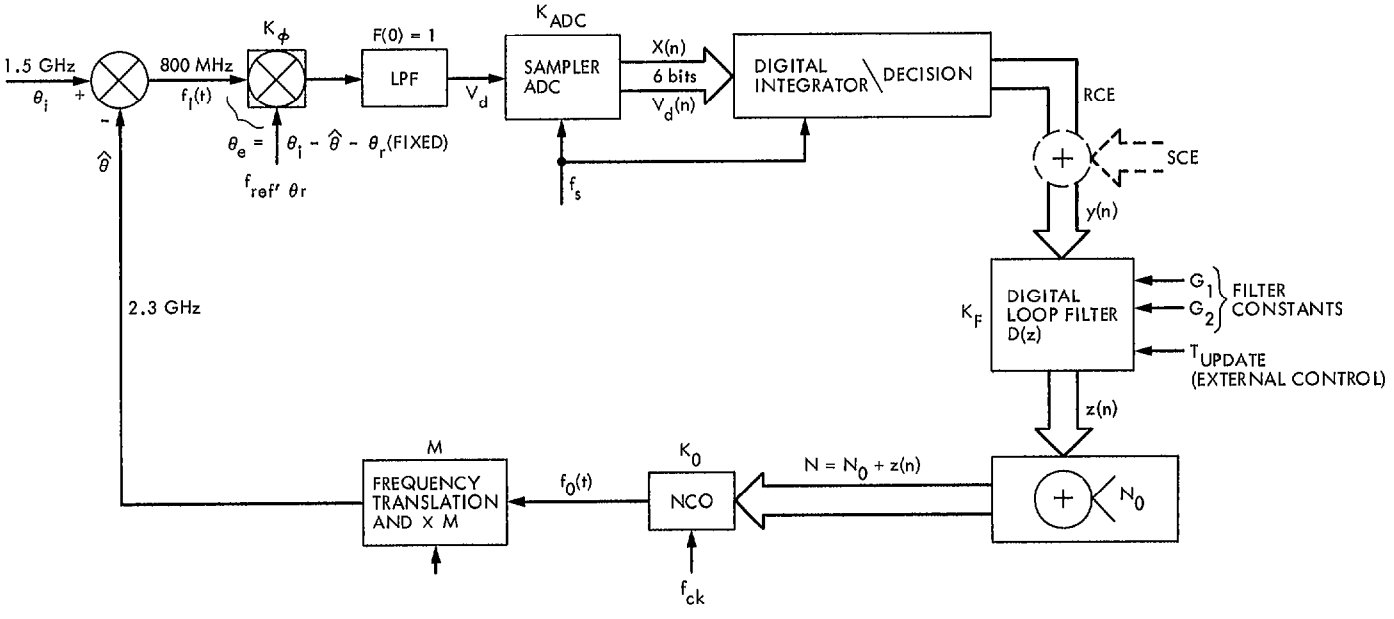

Fig. 2. Simplified residual carrier tracking loop

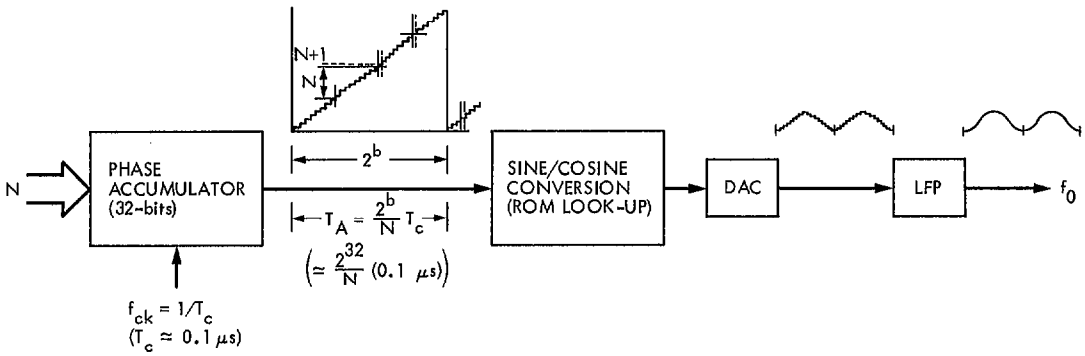

Fig. 3. Numerically controlled oscillator (frequency synthesizer)

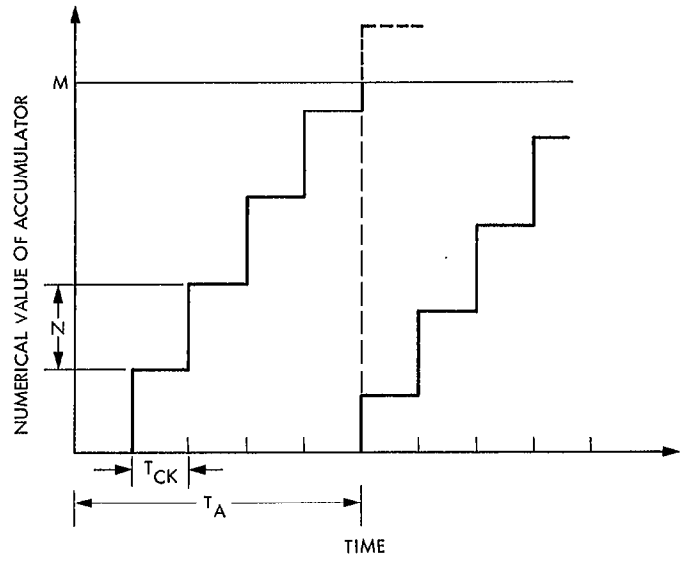

Fig. 4. Numerical value of accumulator as a function of time

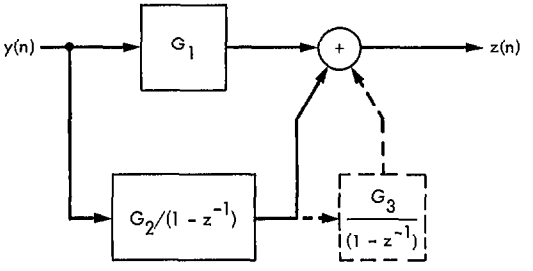

Fig. 5. Digital loop filter

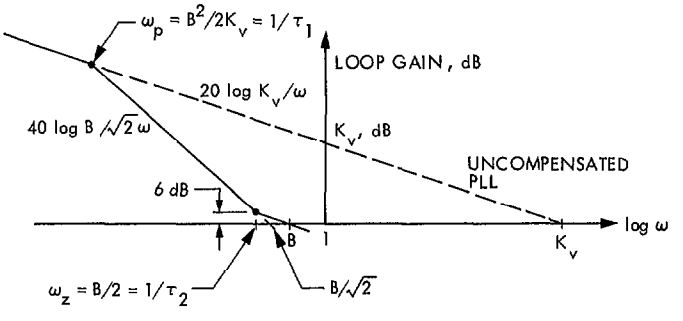

Fig. 6. Open loop gain versus frequency

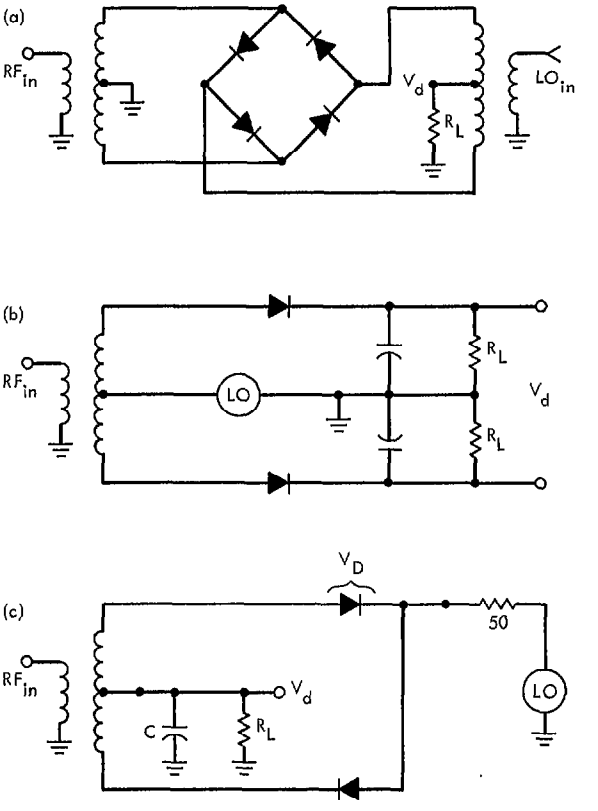

Fig. 7. Typical phase detector circuits

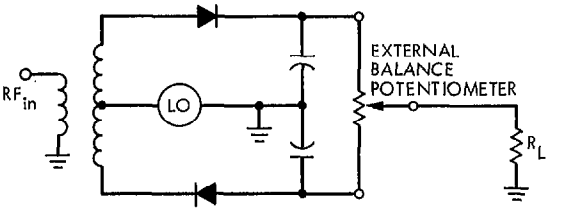

Fig. 8. Improved single-balanced phase detector