Telemetry Simulation Assembly Implementation in the DSN

M. E. Alberda

DSN Data Systems Section

An improved telemetry simulation capability is being implemented, starting in 1983, as part of the Mark IV A Network Implementation Project. The Telemetry Simulation Assembly (TSA) is replacing the Simulation Conversion Assembly (SCA) throughout the DSN. The development of the TSA is discussed, and the design is described to the block diagram level. The testing and evaluation completed so far are summarized.

I. Introduction

Beginning in late 1983, a new telemetry simulation capability is being implemented as a part of the Mark IV A Network Implementation Project throughout the Deep Space Network (DSN). The Telemetry Simulation Assembly (TSA) is a major assembly within the DSN Test Support Subsystem (DTS), and it is required to support testing requirements associated with an expanded set of spacecraft missions.

The design implemented provides simulated spacecraft and related reference telemetry test signals that are routed to other DSN subsystems, as shown in Fig. 1.

The TSA is a computer controlled data generation and transmission system that is based on the Modular Computer Systems Classic 7845 minicomputer. Also included are various peripheral equipment and the JPL designed Signal Generation Assembly (SGA) equipment. The SGA equipment consists of large plug-in circuit boards, an output amplifier unit, a power supply, a cable interface panel, and multiple external function generators.

The TSA was developed to replace the existing Simulation Conversion Assembly (SCA) currently in use throughout the DSN.. The SCA contains a limited capability computer (XDS-910) that is virtually obsolete based on today's technology. The TSA provides for very much higher data and symbol rates, more extensive encoding capability, and greatly increased storage and memory capacity, including disc and random access memory (RAM).

Following an in-house prototype fabrication and evaluation effort, a production contract was awarded to an electronics manufacturer in 1982 covering four systems of SGA equipment plus extensive spares and documentation. This equipment was successfully completed and acceptance tested in 1983. Then two complete systems were delivered to the DSN Systems Integration Facility (SIF) where systems integration and testing are in progress. The balance of two systems plus all spares will be delivered to the SIF in early 1984.

This report describes the equipment built and summarizes the testing completed to date. Lab and acceptance testing have

been done by utilizing a test program developed for this purpose. The test program is loaded into the computer from disc, and operator commands are entered from a local terminal. This terminal is provided for lab use only and has not been provided for use in the operational mode, where control will be remote, from another subsystem.

A TSA operational program is under development and is currently in the development test phase. A description of this program is not included in this report.

II. Functional Characteristics

The missions supported are listed in Table 1, along with the telemetry characteristics associated with each mission. However, significantly higher capability was incorporated in the new TSA above that needed for the new mission set, including added output channels and delay sections; much higher data and symbol rate capability (up to 2 M b/s or 4 M s/s) was also incorporated. This was done to satisfy anticipated requirements associated with potential new missions, such as Venus Radar Mapper (VRM).

The TSA was designed to be remotely operated and monitored, with local operation to be done only for checkout and maintenance. The remote operation is accomplished from a manual console, which is a part of the Link Monitor and Control Subsystem (LMC). This unit also contains an MC7845 minicomputer which is linked with several other subsystem minicomputers via a Local Area Network (LAN). These subsystems are located in a Signal Processing Center (SPC), which is part of a Deep Space Communications Complex (DSCC). Three DSCC's are contained within the DSN, one at Goldstone, California, one in Spain, and one in Australia.

Six independent data output channels have been provided, all operating simultaneously. Each channel can operate in either of two modes — a computer data source mode or a self-contained data generation mode. Each channel provides data formatting (NRZ-L, NRZ-M, or Biphase-L), data encoding (either long- or short-constraint length codes), and frame-length counting with coder-reset capability.

Six delay sections have been provided in order to support antenna array testing. In the DSN, either a single antenna or a group (two or more) of arrayed antennas can be used to track one spacecraft. Arraying provides a significant gain in signal-to-noise ratio (SNR) over that available from a single antenna. If arrayed, a signal reaches each antenna at a slightly different time due to the physical distance between antennas. The TSA generates and sends a test-signal stream to the Test Transmitter (TT) associated with each antenna; the test-signal stream is delayed a different magnitude for each antenna

in order to simulate the difference in arrival time of a signal at each antenna. A fixed spacecraft position is assumed for each array test, and a delay resolution down to 0.1 μs is provided by each delay.

III. Detailed Hardware Design Description

A brief summary of the subsystem design is presented below.

A. Subsystem Block Diagram

The interfaces to other subsystems are shown in Fig. 2. These consist of the following:

(1) Local Area Network (LAN) ties in with other computers, e.g., the Link Monitor (LMC) and the Complex Monitor (CMC). Data, command, and status transfers are transmitted between selected computers on the bus, as required.

(2) The TSA receives multiple inputs of a 10 MHz precision reference from the Frequency and Timing Subsystem (FTS). These references are routed to each one of the 12 function generators and also to the SGA planes containing the digital channels and the delay sections. Also received from the FTS are 1, 10, 100, and 1000 pulses/s timing signals that are used by the computer for real-time interrupt generation, as required.

(3) The TSA provides up to seven independent output baseband signals, one signal to each Test Transmitter (or Test Translator) via an Exciter, contained within a Receiver-Exciter subsystem associated with each antenna (see Fig. 1). Each TSA signal consists of a square wave subcarrier onto which data (or symbols) have been bi-phase modulated. The subcarrier is also amplitude controlled to represent a desired mod index attenuation for a given test.

(4) The TSA provides multiple reference output signals (symbols, symbol clock, data, and modulated subcarrier) to telemetry link assemblies where error rates are determined. These are Baseband Assembly (BBA), Subcarrier Demodulator Assembly (SDA), Symbol Synchronizer Assembly (SSA), and Telemetry Processor Assembly (TPA).

The subassembly units contained within the TSA consist of the 7845 computer with peripherals, the SGA circuit planes which plug into a Peripheral Controller Enclosure (PCE) associated with the computer, a removable cartridge disc, an output amplifier unit (OAU), twelve function generators, and a power

supply. This equipment is contained in four racks as shown in Fig. 3.

B. TSA Internal Organization

The computer is used to remotely control and monitor all equipment within the TSA, as shown in Fig. 4. The function generators (FGs) are remotely controlled and monitored via an IEEE-488 bus driven from a controller card located in the IOIS section of the computer. Waveform (square wave), frequency, phase angle, amplitude, and DC offset are set by computer commands. Self-test of each FG can also be commanded, and the result is fed back to the computer via the bus.

Control words are sent out from the computer and loaded into holding registers that provide groups of control bits, as required, to control all operating features of each digital channel, delay section, and modulator-output amplifier section, including signal routing in and/or out of each of those circuits.

Long-loop simulation capability is provided for data rates up to 30 Kb/s. Data are received at an SPC via a ground communications link and sent to the TSA via the LAN. The TSA stores, formats, and sends the data to the SGA where the modulated signal is used to test the end-to-end Telemetry System.

The computer and its I/O configuration are shown in Fig. 5, where each line represents a plug-in circuit board. An I/O Processor, called the internal IOP, is provided on the CPU board. Another IOP, called the external IOP, is provided on a separate board. A separate bus is provided for each of these IOPs, and maximum data transfer rates are as shown. The SGA planes are loaded from the external IOP when operating one (or more) digital channels in the computer mode. An aggregate digital channel output rate of 6 Mb/s has been demonstrated, i.e., 1 channel at 6 Mb/s or 2 channels at 3 Mb/s each, etc., using test software. The SGA planes have been built from partially populated circuit planes, called General Purpose Interface Controllers, with custom circuitry (about 400 ICs) added on each plane.

C. Digital Channel Description

Six digital channels are provided, three on each of two SGA-1 type boards. Fig. 6 shows the functions and data flow, in block diagram form, for a typical channel. In the computer mode, each of two FIFO memory buffers is alternately loaded from the computer in a burst mode, up to 64 16-bit words per FIFO. Each FIFO is alternately emptied into a parallel-to-serial converter, where a continuous serial data bit stream is generated. When one FIFO is empty, data are obtained from the other FIFO, while at the same time a Data Request is sent

to the computer to refill the empty FIFO. In the other data source mode, simulated data are generated by hardware contained within each channel. Any one of the following data forms is available: square wave (1, 0, 1, 0, . . .), all 1's, all 0's, a repetitive pseudo-noise (PN) sequence 2^{11} −1 bits long, or an operator-selected repetitive pattern up to 6-bytes long. Then the serial data stream, selected from any of the desired sources, is routed to a data format generator (NRZ-L, NRZ-M, or bi-phase L) and then to a selected encoder, if coding is required, where symbol bits (symbols) are generated. A separate FG provides the clock input for each channel, from which symbol and data clocks are derived. A frame counter is also provided that generates a signal to reset the encoder shift register at the end of each frame, if required by the selected code. The outputs of each digital channel are data, symbols, data clock, and symbol clock.

The outputs from any one digital channel can be routed to any one (or more) delay section by computer control of the multiplexer switching circuitry provided.

D. Delay Section Description

As mentioned previously, the sole purpose for the delay sections (Fig. 7) is to support arrayed antenna testing. When non-arrayed tests are conducted, the delay sections serve no function. However, the digital channel outputs are routed through the delay section anyway enroute to the modulator-amplifier and reference output sections, with essentially zero delay introduced (nominally 0.4 μs maximum).

For array testing, outputs from only one digital channel are routed to multiple delay sections (one delay section per arrayed antenna), and different magnitude delay intervals are generated by each delay section, depending on the assumed spacecraft position and the known physical location of each antenna. Delay interval D1 is provided to simulate the delay in arrival time of a spacecraft signal to an antenna which is farther away from the spacecraft than is the antenna in the array group nearest to the spacecraft. Delay D2 is provided to simulate the time delay required for the signal transmission delay through the cable from an antenna to the Signal Processing Center (SPC). Delay D3 is provided to simulate the processing time required for the Baseband Assembly (BBA) to combine its multiple baseband inputs and develop its single improved SNR output signal to the TPA.

Within each delay section, FIFO buffer memories are provided that store symbols and data for the required delay intervals. Symbol-clock and data-clock signals are also regenerated to simulate the required delays. One output from a delay section is a symbol (data) stream occurring after D1, which is routed to the modulator-amplifier section. The other outputs

from a delay section are reference outputs, occurring after D2 + D3, that are routed to the reference output section. The required delay intervals are developed within each delay section by counting down, at a 10 MHz rate, counters that have been initially loaded from the computer with a binary number corresponding to the desired delay interval. The reference outputs from only one delay section within an array group are used and routed to the other assemblies in a telemetry link, i.e., from the delay section with the longest total delay interval, DT. There are five variable and one fixed delay sections provided, totaling six.

E. Modulator-Amplifier Section

There are six bi-phase modulator (mod) sections provided. Each mod has two inputs, a symbol (data) stream from one of the six delay sections and a simulated subcarrier input from one of six FGs. The FG signal is fed to both positive and negative inputs of a high-speed operational amplifier (op amp) through high-speed switching transistors (FETs). One FET is conducting while the other is not. Thus, the op amp output is either inverted or noninverted, depending on which FET is turned on. One FET is controlled by noninverted symbols while the other FET is controlled by inverted symbols, derived from the same symbol stream. Thus, the op amp output provides the desired bi-phase modulation. The simulated subcarrier input amplitude is set, at the FG, to provide an output amplitude proportional to the desired mod-index value. Subcarrier phase is also set at the FG to simulate the desired D1 delay.

Each mod output is connected to one of seven output amplifier units through an 8-to-1 analog multiplexer switch. Each output amplifier is a high-speed, high-power hybrid op amp coaxial cable driver whose output is connected to an assigned Test Transmitter (TT), or Test Translator, in a Receiver-Exciter Subsystem. Sufficient speed and power are available from these amplifiers so that an excellent square wave shape is preserved and delivered to a TT up to a frequency of 5 MHz, through a 50 ohm coaxial cable up to 75 m long.

The analog multiplexer switches are provided to achieve overall improved availability so that any digital channel and any delay section can drive a specified TT without requiring any manual cable switching.

All modulators, analog switch multiplexers, and output amplifiers are contained on one large printed circuit board mounted in the Output Amplifier Unit (OAU).

F. Reference Output Section

The reference outputs from any one delay section can be routed, through digital multiplexer switching, to any one of

four telemetry links in the SPC. There are two types of links utilized, one containing a dual channel BBA and a dual channel TPA, and the other type containing two SDAs, two SSAs and a dual channel TPA.

The reference outputs provided from a delay section are

(1) Modulated subcarrier (fixed level) to an SDA

(2) Symbols to an SSA

(3) Symbols, symbol clock, and modulated subcarrier (fixed level) to a BBA

(4) Data to a TPA

Three delay sections, a fixed delay section, a control register section, and the Reference output section are contained on an SGA-2 type circuit board.

G. Power Supply

The power supply unit provides + and − 5V and + and − 15V power to the OAU and + and − 15V power to the SGA boards, as required.

H. Overall Performance Characteristics

The variable ranges and resolution of the signals from digital channel and delay sections are indicated in Table 2.

The wave shape observed at the load end of a coaxial cable to a TT shows rise and fall times of about 10 to 15 ns.

IV. Testing and Evaluation

A. Acceptance Testing

The TSA Test Program was developed to support TSA testing both for individual subassemblies and for the complete system, operating in a typical telemetry link environment. For both types of testing, a Classic 7845 computer is assumed available to run the test program. A CRT terminal (VT100) is used for both types of testing, for manual entries and message display.

The test program provides a menu of commands that allows for selection and control of all operating features of each digital channel, delay section, function generator, and signal routing between all sections.

A prototype TSA system, located in a development laboratory, was used for initial checkout and acceptance testing of all SGA-1 and SGA-2 circuit boards as well as all power supply and output amplifier units. The Acceptance Test Procedure

(ATP) and test data sheets are included within the Operation and Maintenance Manual (JPL TM 08301).

The final portion of the ATP was completed, for each TSA system, using equipment located in the Verification Test Facility, where TSA system inputs and outputs were verified using telemetry-link equipment.

The prototype system has been used for TSA operational program development and testing, in addition to its use for hardware checkout and testing.

B. System Integration Facility (SIF) Testing

After all parts of the ATP were successfully completed, the TSA systems were delivered to the SIF where integration testing with other subsystems was completed. Two TSA systems have been delivered to the SIF so far, and one system to the VTF, which meets project schedules. The remaining system is fully tested and will be delivered in the near future, along with the spare subassemblies scheduled for delivery to each of three DSCCs and to the VTF.

C. First Installation Testing

After testing was completed at the SIF, the first TSA system was delivered to the Goldstone DSCC (SPC-10), along with the other subsystems that are parts of the Mark IV A project. After installation here, extensive TSA testing and evaluation will be performed while using the other required subsystems, including calibration procedures as required, for operating the TSA delay sections to support array testing.

V. Conclusion

The prototype development phase and the production fabrication and test phases of the TSA project have proceeded in an orderly fashion with relatively few changes being required. The effort has closely followed the original development plan, including cost, schedule, and the meeting of performance requirements.

Table 1. Telemetry characteristics

Mission Data Channel		PCM Type	Coding Characteristics	Data Rates, bits per sec	Subcarrier, kHz	Mod Index 0°	RF Band	Frame Size	Frame Sync
PIONEER 10/11									
	1	NRZL	Uncoded	8-2048	32.768	66	S	192 or 384	
	1	NRZL	Conv. K=32; R=1/2	8-2048	32.768	66	S	192 or 384	
PN-Venus									
	1	NRZL	Uncoded	8-4096	16	37, 67	S		
	1	NRZL	Conv. K=32; R=1/2	8-2048	16		S	512	F8549(16)
Space Telescope	Biφ-L			4000					
Voyager 2 Uranus	1	NRZL	Conv. K=7, R=1/2	10-29, 900	360	70	X	1792	
	2	NRZL	Uncoded	40	360	55	X	2200	03915ED3(16)
	2	NRZL	Uncoded	40	22.5	55	S		
Galileo									
	1	NRZL	Conv. K=7, R=1/2	7,680-134,400	360		X	5120, 1120	
	1	NRZL	Conv. K=7, R=1/2	Up to 40,000	22.5/360	20 to 88	S	1920, 4480	03915ED3(16)
	2	NRZL	Uncoded	40	22.5		S	7680	
ISEE-C									
	1	NRZL	Conv. K=24, R=1/2	64	1.024	40	S	1024	FAF320(16)
	1	Biφ-L	Conv. K=24, R=1/2	512-2048	N/A	63	S		EC819FBE
ISPM-ESA	1	NRZL	Conv. K=7; R=1/2	1024-8192	131.072	32	X	1024	EB90(16)
AMPTE-CCE									
	1	Biφ-L	Conv. K=7, R=1/2	101,000	NA		S		
	2	NRZL	Uncoded	3300	16		S		
AMPTE-IRM									
	1	Biφ-L	Conv. K=7, R=1/2	1000-8000	NA	74	S		
	1	NRZL	Conv. K=7, R=1/2	2048, 4096, 8192	131.072		S		
AMPTE-UKS									
	1	Biφ-L	Conv. K=7, R=1/2	1000-32000	NA				
GIOTTO		NRZL	Conv. K=7, R=1/2	20000	327.7				

Table 2. SGA performance characteristics

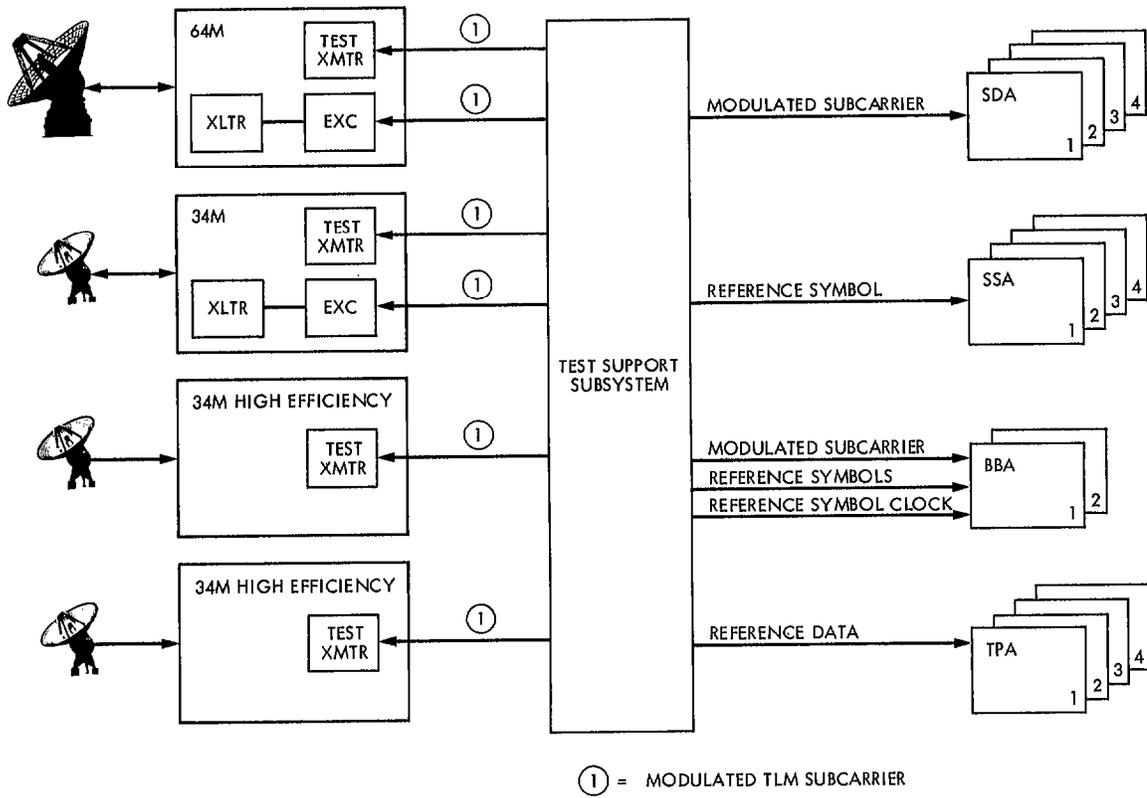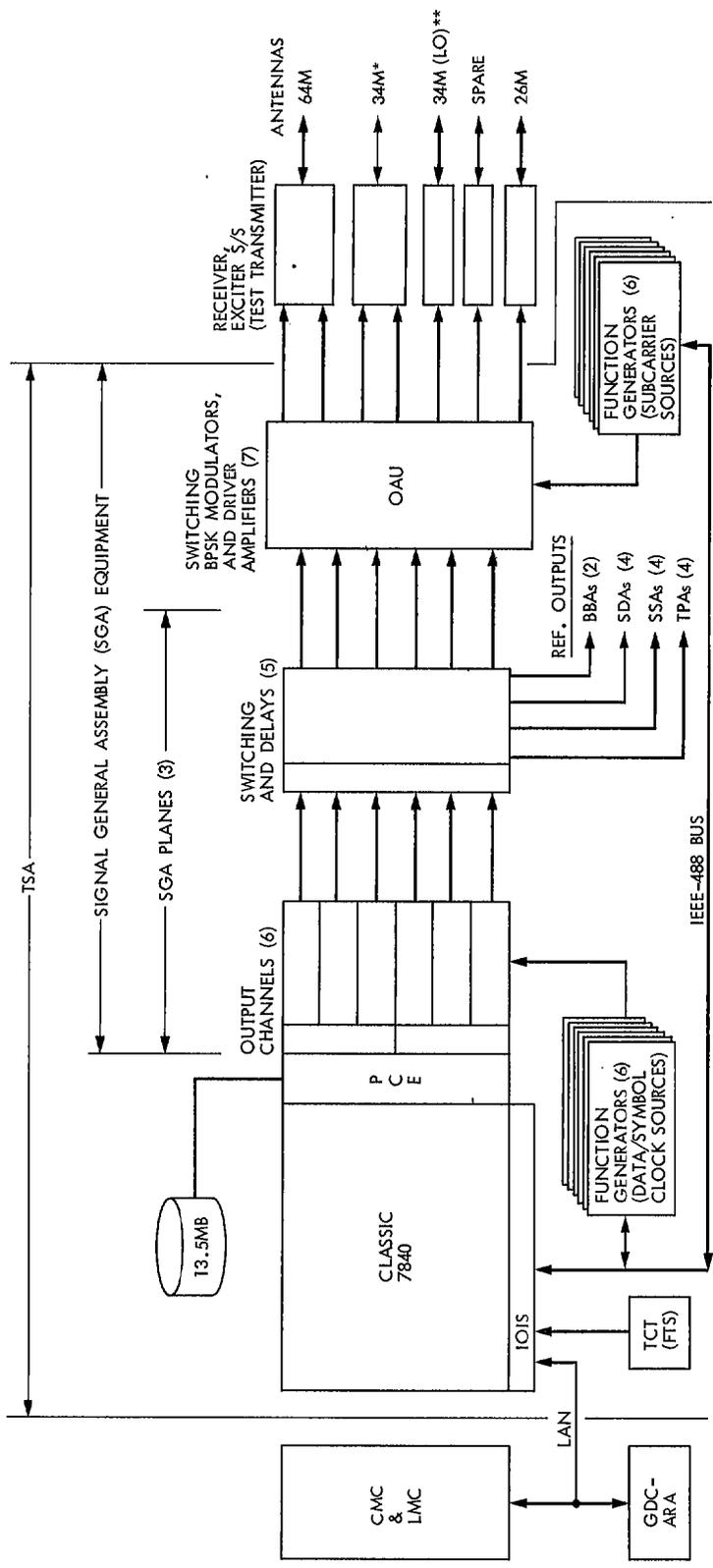| Parameter	Range	Resolution
Delays	1.0 – 537.6 μs	0.1 μs
Subcarrier	50 Hz – 5 MHz	0.01 Hz
Symbol rate (NRZ WO S/C)	6 SPS – 5 MSPS	0.01 Hz
Symbol rate (NRZ W S/S)	4 SPS – 5 MSPS	0.01 Hz
Symbol rate (BIO-L)	100 SPS – 5 MSPS	0.01 Hz
Data rate (7-1/2, 7-1/3 CR)	10 BPS – 1.7 MBPS	0.01 Hz
Data rate (24-1/2, 32-1/2 CR)	8 BPS – 2 MBPS	0.01 Hz

Fig. 1. Test signal distribution

Fig. 2. TSA subsystem block diagram

* DSS12, VIA MICROWAVE
** GOLDSTONE, AUSTRALIA; PLANNED LATER FOR SPAIN

CABINET 4

| A1 FUNCTION GENERATOR HP3325A | A2 | A3 | A4 | A5 FUNCTION GENERATOR HP3325A | A6 BLANK | BLANK | BLANK | BLANK | BLANK |

CABINET 3

| A1 FUNCTION GENERATOR HP3325A | A2 | A3 | A4 | A5 FUNCTION GENERATOR HP3325A | A6 BLANK | A7 OUTPUT AMPLIFIER ASSY | BLANK | A9 POWER SUPPLY ASSY | BLANK |

CABINET 1

| A1 IOIS P/S | A2 IOIS FILE 1199-1 | BLOWER | A3 CLII/45-2 CONTROL PANEL +5V | A4 CPU FILE | A25 FTS-TCT 1 | A5 CPU CONN PANEL | A6 AC PANEL |

CABINET 2

| A2 PCE #1 4911-1 #1 | A3 PCE #1 P/S +5V | A4 PCE #1 CONN PANEL | A5 13.5 MB DRIVE 4181-1 | A6 PCE #2 4911-1 #2 | A7 PCE #2 P/S +5V | A8 PCE #2 CONN PANEL | A26 NIU | A5 AC PANEL |

Fig. 3. TSA rack configuration
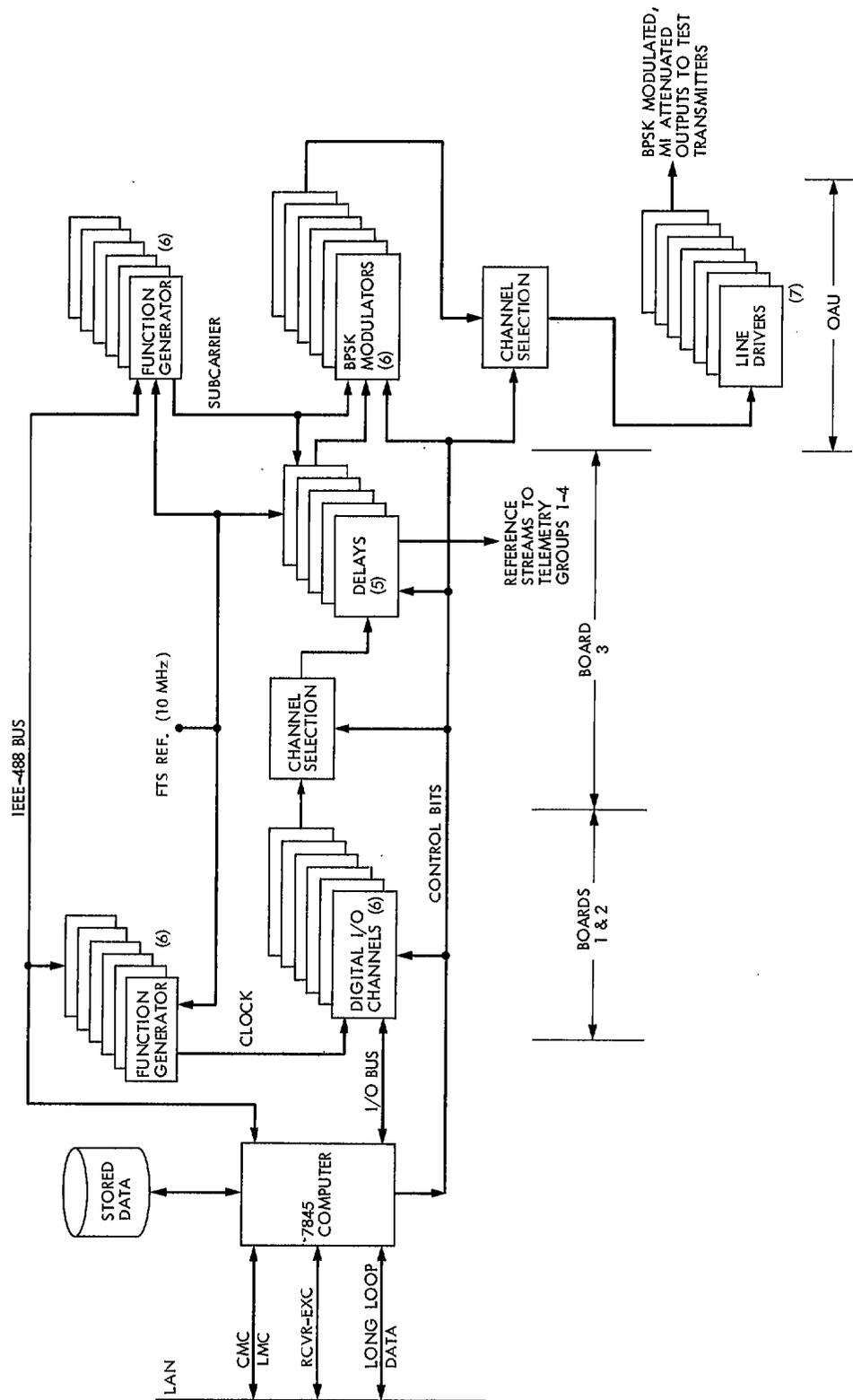
Fig. 4. TSA hardware configuration

(CLASSIC 7845 – BLOCK DIAGRAM)
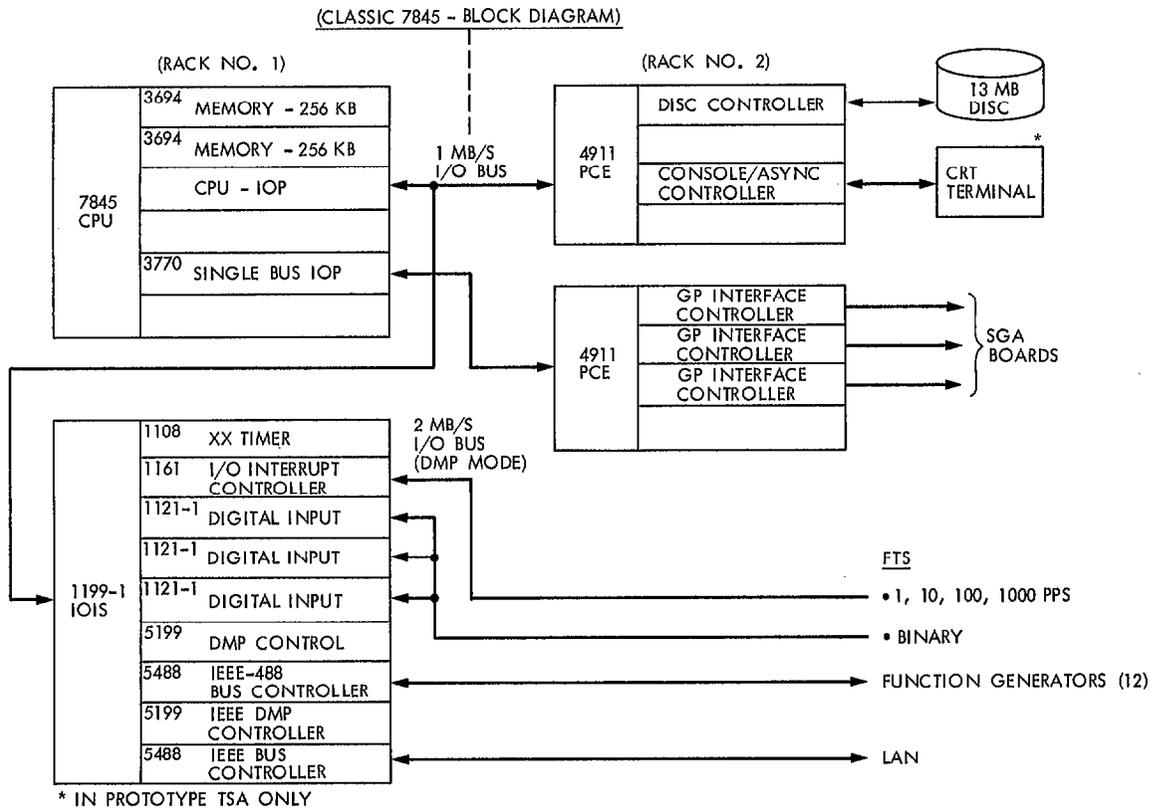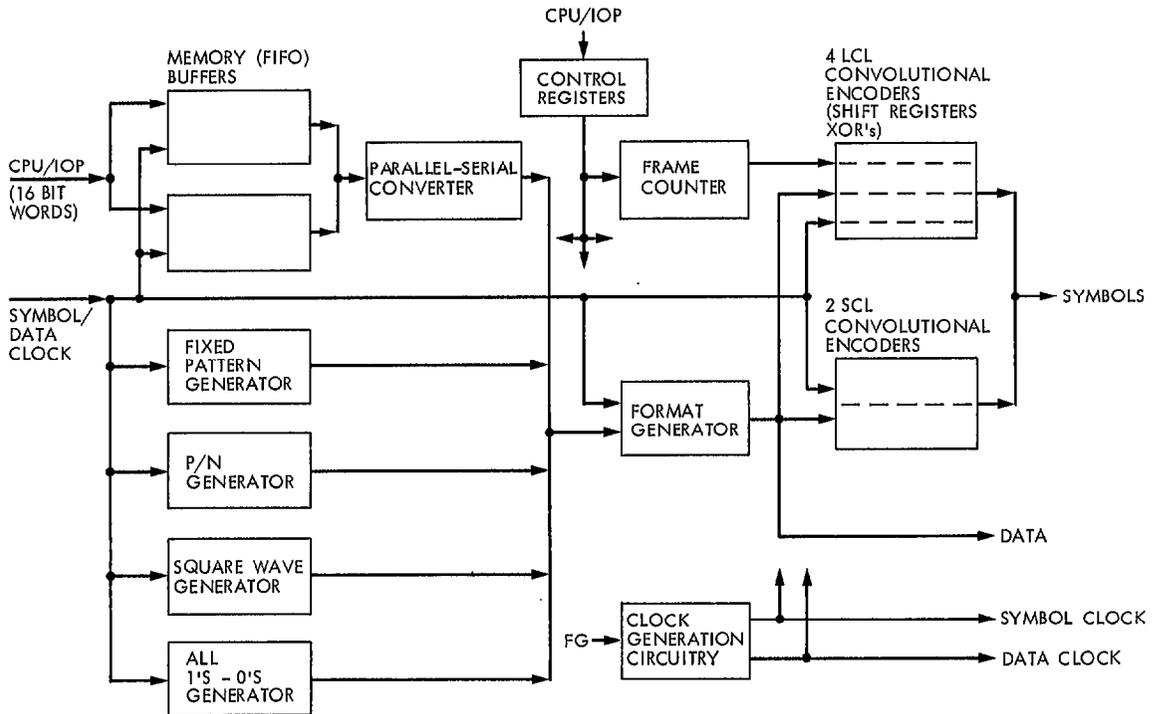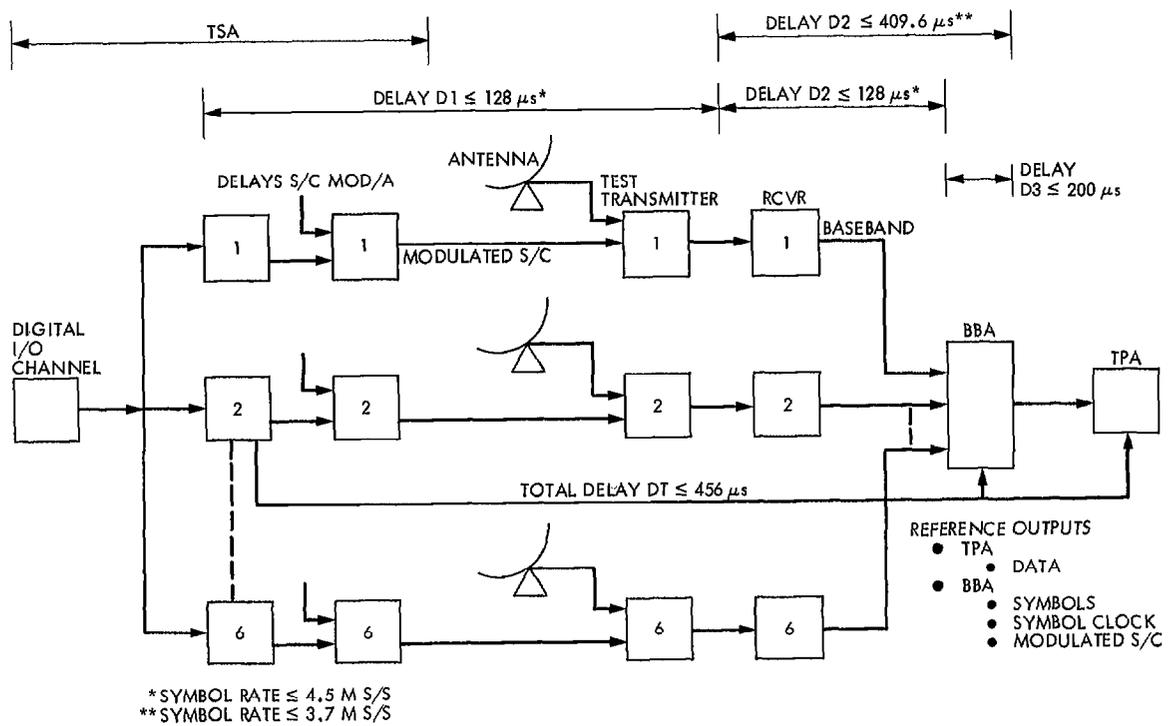
Fig. 5. TSA computer configuration

Fig. 6. Digital channel configuration

Fig. 7. Antenna array block diagram