The Goldstone R/D High Speed Data Acquisition System

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A digital data acquisition system that meets the requirements of several users (initially the planetary radar program) is planned for general use at Deep Space Station 14 (DSS 14). The system, now partially complete, is controlled by a Digital Equipment Corporation (DEC) VAX 11/780 computer that is programmed in high level languages. A DEC Data Controller is included for moderate-speed data acquisition, low speed data display, and for a digital interface to special user-provided devices. The high-speed data acquisition is performed in devices that are being designed and built at JPL. Analog IF signals are converted to a digitized 50 MHz real signal. This signal is filtered and mixed digitally to baseband after which its phase code (a PN sequence in the case of planetary radar) is removed. It may then be accumulated (or averaged) and fed into the VAX through an FPS 5210 array processor. Further data processing before entering the VAX is thus possible (computation and accumulation of the power spectra, for example). The system will be located in the research and development pedestal at DSS 14 so easy access by researchers in radio astronomy as well as telemetry processing and antenna arraying is anticipated.

I. Overview

A High Speed Data Acquisition System is being constructed for research and development (R/D) use in the Deep Space Network (DSN). This system will, when completed, be a subsystem of the DSN Ground-Based Planetary Radar System. Its primary purpose will be to collect the 15 MHz bandwidth RF signal from the DSN Radar Receivers and perform all necessary data rate compression (filtering, phase correction, and correlating) to get radar data on a general purpose computer for further processing. This function is currently performed by an array of hardware devices that are, for the most part, inadequate for the type of high bandwidth radar experiments that will be performed over the next decade. A good idea of the capabilities of the current system can be seen in Refs. 1 and 2. This article provides a system level understanding of the new system.

The High Speed Data Acquisition System is a collection of advanced digital signal processing devices that are connected to a host minicomputer. The system will be configured to operate in a wide range of modes, allowing a user to interconnect these devices and control them completely under software control. The set of processing devices that will be available to users enables many types of radar experiments as well as pulsar observations, general radio astronomy, and some telemetry demodulation and decoding capabilities.

A Digital Equipment Corporation (DEC) VAX 11/780 computer is the heart of the system. The standard DEC operating system (VMS) will be used to run the machine while all of the general purpose peripheral devices will be connected to the VAX through conventional VMS driver routines. Consequently, nearly all data acquisition programs (i.e., software for

the control of experiments) may be written in high level languages such as FORTRAN or Pascal. This design philosophy provides a means for low cost data collection and ease of documentation. It will also enable more people to operate the system with only a small amount of specialized training.

The configuration of the High Speed Data Acquisition System at completion is shown in Fig. 1. The top part of the figure represents the VAX computer and its peripherals while the bottom part shows the special purpose devices that will be built.

The VAX 11/780 computer is also configured with all the necessary peripherals for program development and testing. In addition there are commercial peripherals that are essential to the radar program, including a high resolution color video monitor for real time image display and a high resolution graphics printer for data monitoring during experiments. Data will be collected and saved on a 500 Mbyte Winchester disk or on two high speed magnetic tape drives. The storage capability on this system will be nearly a factor of ten better than that of the current radar system.

In order to process the high rate data imposed by anticipated signal bandwidths, special purpose devices are also required. These high speed digital signal processing devices will be connected to the VAX through a Floating Point Systems (FPS) array processor. Subsequently, the data may be further reduced and processed before being transferred to the VAX. This will relieve the typical throughput problems that one encounters when using a host computer to collect and process real time data.

In addition, there will be low rate data input and output available on the VAX by means of a set of standard DEC analog-to-digital and digital-to-analog converters. Data collected in this manner by the VAX can be transferred to the array processor for processing and then back to the VAX for handling or storage. The digital-to-analog converters can be used to drive instruments or real time displays in order to enhance certain experiments.

The radar correlator assembly consists of a block of sixteen correlator modules that will run at a clock rate of 10 MHz. Each module will be capable of performing 256 delay lags in a one by four bit correlation function in a continuous stream. Each individual module will be able to operate in a cross- or auto-correlation mode. The selection of input signals, reference signals, and interconnection of the modules will be under complete control by the host VAX. This means that a user can reconfigure the correlator assembly to suit the needs of each individual experiment, or change their function during an experiment in a controlled manner, all from software written in a high level language.

The radar system typically uses up to three complex input channels. However, a fourth complex channel is included in the new system. This extra channel provides for expansion as well as a hardware backup.

Since some radar experiments will require pulsed or spread spectrum radar as well as CW radar, pseudonoise (PN) sequence generators must also be part of the High Speed Data Acquisition System. One generator is required for each channel. The output of these generators will be supplied to the correlator assembly, the IF processing devices, and the transmitter driver. These PN generators are programmable (from the VAX) so that a large set of PN codes of various lengths can be used for different experiments.

A unique feature of the new system is the IF processor hardware. Input signals are sampled directly at the output of the IF amplifier which is centered at 7.5 MHz. With this center frequency, a channel bandwidth of 15 MHz is available. Thus, a sample rate of at least 30 MHz will be needed to handle the information band. A sampling rate of about 50 MHz will be used to digitize the IF signal as the input to the system. All signal conditioning and processing following this will thus be accomplished digitally. The conditioning processes will consist of antidispersion filters, baseband mixers, and baud integrators. The resulting baseband signal will then be fed to a set of signal multiplexers that will be used to distribute the various signals to the correlator assembly.

A wide range of preprocessing can be achieved, ranges from none to the full capability of filtering, correlating, and transforming. For this reason, it is better to view the High Speed Data Acquisition System as a four channel digital receiver system. Among the nonradar applications that this system will be capable of supporting are general radio astronomy, SETI (Search for Extra-Terrestrial Intelligence), and telemetry reception. These applications are addressed in more detail in the following section.

II. Applications

The primary mode of operation of the High Speed Data Acquisition system is the collection and processing of radar data. Since the system was designed with this purpose in mind, it will do this job particularly well. The system will support CW, pulsed, and spread spectrum radar experiments, and thus it will support experiments targeted at the outer planets as well as the terrestrial planets. A number of radar experiments anticipated over the next five years are listed below along with

their system requirements. Figure 2 shows a time table of the various experiments.

Mars. This will be the first experiment that will use the High Speed Data Acquisition System. The observations are planned for June and July of 1984. Only one station (DSS 14) will be used. This experiment does not require the IF processor portion of the system. It will require at least one quarter of the correlator assembly, a PN sequence generator, and all of the computing facility. In addition, a baseband mixer and sampler assembly must be fabricated (mostly out of existing parts) to interface the system to the IF output of the radar receiver.

Mercury. Mercury can be observed several times each year. This work will require either a dual polarization receiver or the use of two stations operating at different polarizations. In either case, at least two channels of the IF processor must be in place. Mercury will be observed with both CW and spread spectrum radar.

Venus. Venus will be observed in the first six months of 1985. These observations require three stations. The entire IF processor must be working by this time. Also, the full capability of the correlator assembly will be needed.

Asteroids. These observations will be made on a semiregular basis. CW radar with frequency hopping and a dual-polarized receiver will be used.

Comets. These observations are similar to those of asteroids. Of particular note are the proposed observations of Halley in early 1986.

Moons of Jupiter. These observations will resume in April of 1985. They will also use CW radar with frequency hopping and dual-polarization.

Rings of Saturn. The first observation will be in May of 1985. CW radar with frequency hopping and dual-polarized signals will be used.

The High Speed Data Acquisition System will also be a useful tool in general Radio astronomy. It could be used to measure Stokes parameters (polarization parameters) and average the results in real time. It will also be possible to run the system as a real time interferometer by using the multiple channels in the IF processor.

The flexibility that is being designed into the High Speed Data Acquisition System will make it a useful tool in DSN receiver development. It will be the first system at a DSN site to have a fully digital IF processor. Since all aspects of this IF processor are to be programmable from the VAX computer, it can be used to experiment with new types of mixing and filtering techniques for telemetry and radiometric reception. It will be possible to control the loop filters dynamically during reception to provide improved receiver performance. The four channels in the IF processor can be used to perform real-time arraying of up to four antennas as well as carrier arraying for telemetry reception. The correlator assembly could also be used to demodulate a subcarrier and track data in a telemetry signal. Telemetry decoding could then be done on the VAX if the data rates are low enough. If the system were to be used for extensive high rate telemetry experiments, then a Viterbi decoder (MCD) could be attached to the VAX as another high speed peripheral.

The extreme flexibility in the High Speed Data Acquisition System and the ability to control this flexibility from simple high level programming languages is certain to make the system a major research tool for many projects well into the future.

III. Computer Facility

The High Speed Data Acquisition System is based on a Digital Equipment Corporation VAX 11/780 computer. This computer was chosen to meet the need for high-performance real time data collection, data processing, and program development. This machine, and all its associated peripherals and hardware add-ons, will be located at the Goldstone facility in the pedestal of DSS-14.

The VAX computer uses a 32-bit architecture that is based on the PDP-11 family of 16-bit minicomputers. Although the VAX uses addressing modes and stack structures that are similar to those on PDP machines, the VAX provides 32-bit addressing. This is enough to access a four gigabyte program address space. The 32-bit data paths in the VAX also offer increased processing speed and accuracy over the PDPs. The VAX processor hardware and instruction set were specifically designed to support high-level programming and still produce efficient machine code. The VAX also has a floating point processor that augments the primary processor by performing floating point operations with a substantial performance improvement. There is also a high speed memory cache that provides a large reduction in memory access time. The VAX main memory uses error correcting codes to correct single bit errors and detect double bit errors in each byte.

The VAX operating system, VAX/VMS (or simply VMS) is a multi-user virtual memory system that supports an easy-to-use interactive command interface. The virtual memory feature allows the execution of programs that can be larger than the physical memory allocated to them. Virtual memory

paging (the operation that swaps memory and disk space to allow this feature) is handled automatically by VMS. Consequently, the programmer need not be concerned with the working details of memory management. Memory management facilities can be controlled by the user in the event that such control is necessary to optimize the real-time performance of a particular program.

There are two hardware buses on the VAX backplane to which peripherals may be attached. One of these is the MASS Bus. It is capable of high throughput communications. The second, the UNIBUS, provides a standard interface that can be used with a large set of peripherals. Figure 3 shows the configuration of the High Speed Data Acquisition VAX. The blocks that have shaded corners represent equipment that is already installed and working in a JPL Laboratory. The peripherals that will be attached to the VAX are listed below (but do not include the special purpose hardware devices that will be described in the following sections):

2 RK07 28 Megabyte Disk Drives. These drives use removable hard disk cartridges. These are useful for storing the operating system and most user software. Since they are removable, they provide a fast method for transporting software or performing backups.

1 RP07 500 Megabyte Disk Drive. This device, which is to be attached to the MASS bus, will be a principal storage area for collected data.

2 TU78 Magnetic Tape Drives. These are high speed (1600 or 6250 bpi at 125 ips) tape drives that can be used in real time data acquisition or high speed data transfers.

1 DR780 High Speed 32-bit Parallel Interface. This device is a 32-bit parallel interface that is capable of transferring data at rates up to two megabytes per second. The DR780 uses separate data paths for control information and data. The control path is 8-bit and bidirectional. The data path provides a synchronous 32-bit transfer which may be clocked by either an LPA11-K clock or by a clock provided by an external device.

1 LPA11-K Analog/Digital Data Controller. This device is an intelligent controller that transfers data between the VAX computer and a set of interface modules. These modules include analog-to-digital and digital-to-analog converters and a high speed 16-bit parallel interface (see Section IV). The LPA11-K subsystem uses silo buffers and direct-memory-access data transfers to allow real-time data acquisition with a very limited interrupt load and very limited burden in the VAX itself. The LPA11-K is implemented using two microprocessors, and it contains its own programmable real-time clock. The VAX can initiate a chain of data transfers through the LPA11-K with only a single I/O request. This silo structure allows data to be transferred continuously regardless of the status of the UNIBUS or system software latencies. Data rates up to 15,000 samples per second can be handled by the LPA11-K. There is also a mode where the LPA11-K services only the analog-to-digital converter and can handle 150,000 samples per second.

6 DR11-C 16-bit Parallel Interfaces. These will be used to provide control to the various special purpose hardware that will be described in Section IV.

2 VT100 CRT Terminals. These will be the primary user interface with the VAX for both program development and experiment control.

1 AED512 Color Graphics Terminal. This will be used as a real time high resolution display for monitoring experiments and reviewing collected data. The AED512 provides a 512 X 512 pixel display with 8-bit resolution in each of the three primary colors for a total for 24 bits for each pixel.

1 LA120 Operator Console. This device will be used to monitor the VAX itself and keep hardcopy logs of system performance. Hardware problems will be reported to the console so that the operator may act upon them when necessary.

1 LXY12 Printer/Plotter. This device will be the primary hardcopy output generator. It will be used to examine quick-look data analysis and to aid in software development.

1 FPS-5210 Array Processor. This device is equipped with a programmable I/O processor (GPIOP) that can be used to collect data from an external device and pass it through the array processor independently of the VAX. Maximum data rate through the GPIOP is three million 38-bit words per second. The FPS 5210 is rated at 30 million floating point operations per second. It will be used to format and process incoming data before it is sent to the VAX.

1 DEC PDS Power Distribution System. The PDS will provide filtered and regulated power to all the VAX peripherals.

The VAX provides the High Speed Data Acquisition with the required flexibility and expandability that are needed to support experimental work at Goldstone well into the future.

IV. General Purpose Acquisition Hardware

The High Speed Data Acquisition System will have a set of peripheral devices that perform conventional data acquisition functions. These functions include digital-to-analog conver-

sion, analog-to-digital conversion, and high throughput digital-to-digital interfaces. These can be used to interface the system with existing data acquisition hardware, laboratory instruments, or specialized display devices. They will also be instrumental in the testing of the system itself.

The general purpose acquisition hardware will reside on its own dedicated bus so that a continuous data flow may be achieved regardless of the status of the buses on the VAX itself. This bus will be attached to the VAX through the LPA11-K Analog/Digital Data Controller that was described in Section III. Figure 4 shows the configuration of this part of the system. The shaded boxes, once again, represent hardware that is already installed in the laboratory.

There will be four modules attached to this LPA11-K bus that will comprise the general purpose acquisition hardware. These are described below:

AA11-K 4-Channel D/A and Display Control. This device provides four independently buffered digital-to-analog converters. Each of these has 12-bit accuracy and a slew rate of 5V/s. In addition the AA11-K includes a display control driver that supports a 4096 X 4096 dot array display. This can be used to drive a high-resolution graphics CRT or an oscilloscope.

AD11-K Analog to Digital Converter. The AA11-K contains a high speed 12-bit analog-to-digital converter and an associated multiplexer. The multiplexer can be used to support 8 full channels or 16 single-ended channels of input. The timing for the conversions can be provided in one of three ways: under software control, from a real-time clock, or from an external input. A multichannel throughput rate of 50 KHz will be possible.

DR11-K Interface. This is general purpose 16-bit parallel interface for interconnection with other digital devices.

KW11-K Dual Programmable Real Time Clock. This module provides two real-time clocks that will be used to control data flow in and out of the LPA11 subsystem and provide accurate time tagging. Each clock is independently programmable and may operate at several different clock frequencies, as may be required for various applications.

These devices, together with the LPA11-K controller, will constitute a subsystem of the High Speed Data Acquisition System that will provide a general compatibility with other data acquisition and data processing hardware without disturbing the other portions of the system. The inclusion of this subsystem will make it easier to append hardware devices to the system when such devices are needed without having to install these permanently.

V. High Speed Data Acquisition Hardware

In addition to the computing facility and the general purpose data acquisition hardware, the High Speed Data Acquisition System will include special purpose hardware that will enable it to collect and process data directly from the IF portion of the radar receiver. This same hardware could be used to interface with other receivers as well. Figure 5 shows the special purpose hardware and its relationship to the computing facility. Most of this special purpose hardware is not available commercially and hence it must be designed and built in-house. The hardware with shaded boxes in the figure has been fabricated and tested.

The high speed data acquisition hardware comprises three subsystems. These are the IF processor subsystem, the correlator assembly, and the PDPG coders (PN sequence generators). Figure 5 shows these subsystems and their relationship to the High Speed Data Acquisition System computing facility.

The IF processor will serve as the principal path for input data in the completed system. It will be designed to accept, as input, an analog IF signal with a carrier of 7.5 MHz and a two sided bandwidth of 15 MHz. Thus the analog-to-digital converters (A/Ds) must sample at no less than 30 MHz and will do so with four-bit accuracy. However, in order to assure that there is a sufficient rejection of frequencies outside of this bandwidth, the converters will actually be capable of a 50 MHz sampling rate.

The outputs from the converters will be passed through Anti-Dispersion Filters (ADFs) before mixing so that phase corrections can be made on a controlled basis. These filters will be programmable from the VAX.

The Digital Complex Mixers (DCMs) will be high speed (50 MHz) digital multipliers, which will heterodyne the IF signal down to baseband. The reference frequency for the conversion can come from the VAX (predictions stored in memory and sent to a PLO) or from feedback within the system.

The signal will then be passed through Complex Baud Filters (CBFs). These devices will serve two purposes. They will act as loop filters that can be controlled by the VAX. In addition, they will smooth the signal so that it may be sampled at a lower rate for subsequent processing.

The correlator assembly consists of a baseband signal multiplexer, correlator-accumulator modules, and a device for data formatting and interfacing to the array processor.

The baseband multiplexer will allow the baseband signals from the four complex channels of the IF processor to be

routed to any combination of correlator-accumulator modules. This function will be under the control of the VAX. In this way, the correlator assembly can be configured many ways, depending on the needs of a particular experiment. The correlators can have a variable number of lags (selectable under computer control) and operate as cross- or auto-correlators.

Each correlator-accumulator module will include a complete 4-by-1 256 lag correlator and a pipelined adder that will produce a 12-bit output. These will operate at a clock rate of 10 MHz. The accumulators will be capable of summing the correlator outputs for up to one full second. The output of each module will be a 28-bit word.

The Interface and Data Formatting will collect the output from the correlator-accumulator modules and feed that data through the General-Purpose Input/Output Port (GPIOP) of the array processor. This collecting function will also be under the direct control of the VAX.

The PN sequences that will be used for spread-spectrum radar work will be supplied by the polynomial driven PN Generators (PDPGs). Each of these will run at a 10 MHz chip rate that will be synchronized with an accurate reference clock. The PDPGs will also provide time domain compensation for the Doppler effects caused by the relative motion of the observer and the target. The PDPGs will be controlled by the VAX and will be capable of generating a large range of PN sequences from a single pulse to a sequence $2^{24} - 1$ bits long.

This special purpose hardware will compose the first high-speed digital IF receiver to be installed at Goldstone. It will be capable of serving as a test bed for digital receiver work as well as radar and radio astronomy work.

VI. Interfacing to the Remainder of the Radar System

In order to perform the experiments that were described in Section II, the High Speed Data Acquisition System must interface with other DSN systems, including transmitters, receivers, communication links, and frequency reference generators. These systems are also undergoing fabrication or upgrading. It is essential that they are operating at the time that they are needed for the various experiments. We describe here the major requirements that the High Speed Data Acquisition System will put on these other systems:

(a) Radar experiments must be performed with transmitters and receivers that operate on the same frequencies. Both S- and X-band signals will be required.

(b) The bandwidth of the transmitter, receiver, and antenna systems must be adequate to pass a 2 MHz PN phase code without a serious degradation of shape for any length $2^N - 1$ where $1 \leqslant N \leqslant 30$.

(c) The X-band bandwidth must also support the Rings of Saturn experiment. At least 10 MHz must be passed for this.

The receiver must provide both orthogonal-circular polarizations simultaneously at X-band. Two identical channels are required, each having a 10 MHz bandwidth centered on a frequency of 8495 MHz. A system noise temperature of less than 20 K is preferable for this work. A similar S-band capability should also exist although it is not mandatory for the proposed radar experiments.

Some experiments require that stations other than DSS-14 be used during an observation. To this end, interstation links must exist between DSS-14 and both DSS-12 and DSS-13. These links must be capable of supporting the PN signal described above.

Accurate timing signals must be provided to the acquisition system. Most of the work can be supported by rubidium clocks. However, any observations that will use more than a single station will require hydrogen clocks.

VII. Conclusion

The High Speed Data Acquisition System will serve the needs of the DSN's Planetary Radar Program at the Goldstone facility over the next decade. The system will be useful in other areas of research including radio astronomy, SETI, and real time antenna arraying. The ability to control the system in a high level software language will enable it to be used by a larger group of people than the current system, and this flexibility will also facilitate its use as a tool for advanced receiver and demodulator development.

References

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3. S. S. Brokl, "Polynomial Driven Time Base and PN Generator," *TDA Progress Report 42-75*, 1983, pp. 84-90.

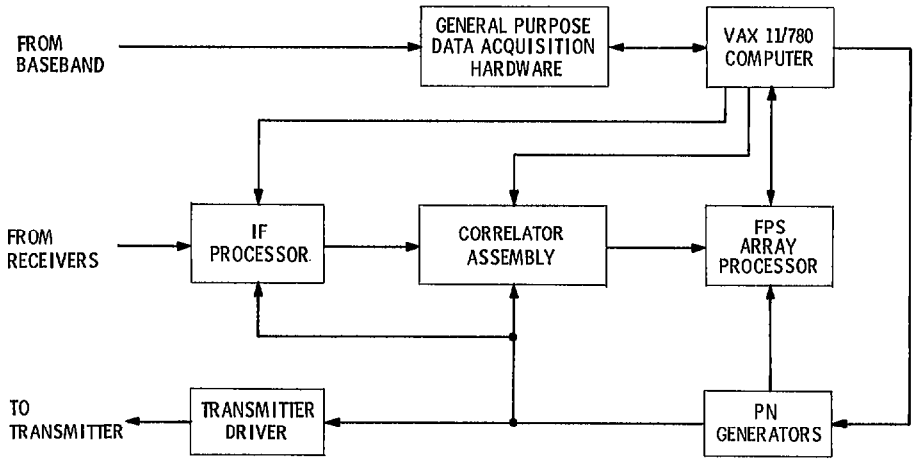

Fig. 1. High Speed Data Acquisition System overall block diagram

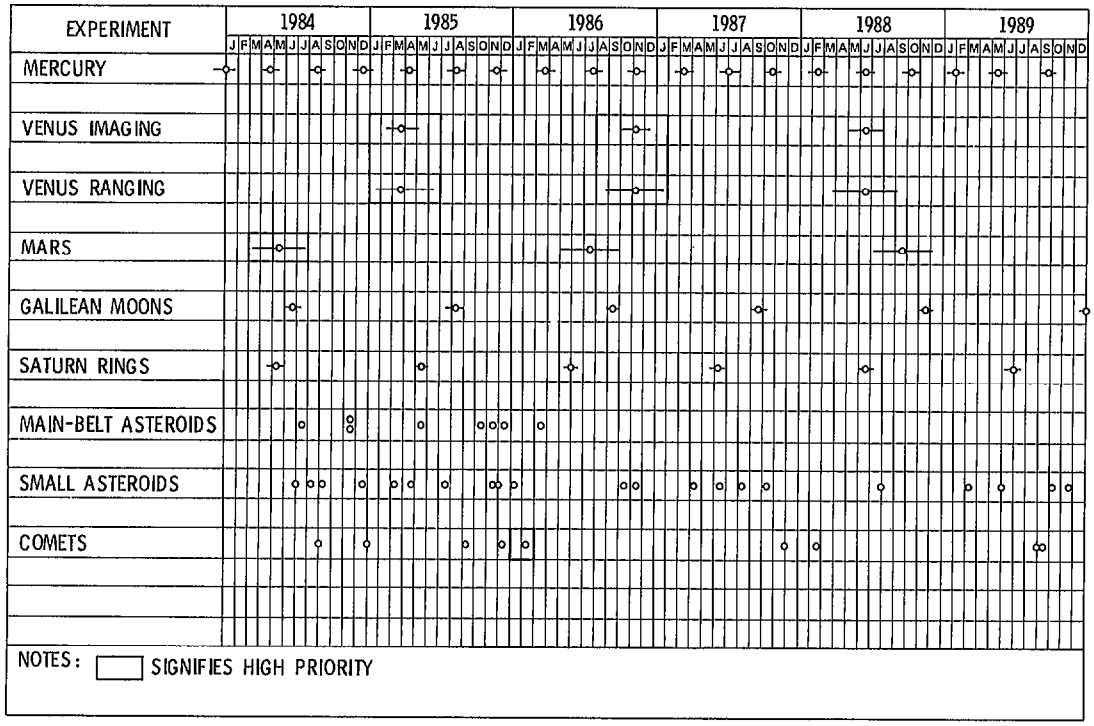

Fig. 2. Time table of anticipated radar experiments

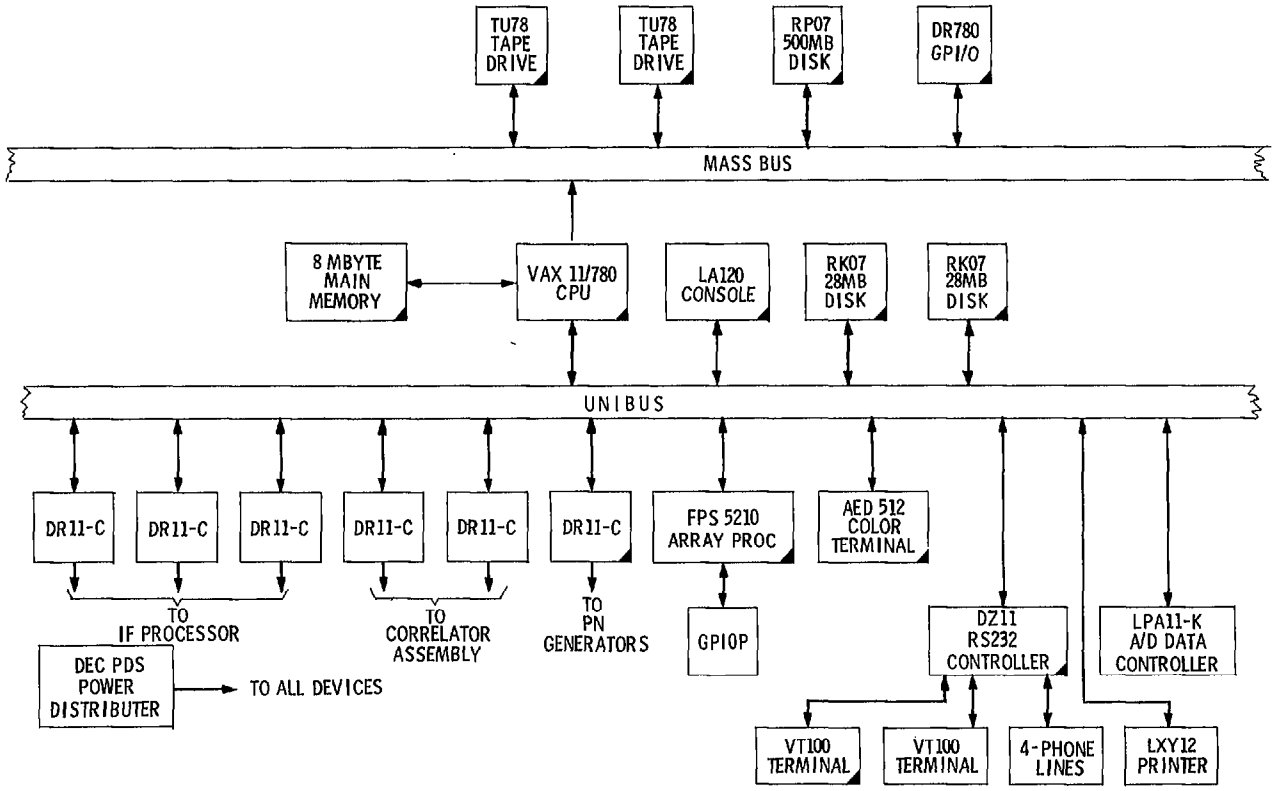

Fig. 3. The VAX 11/780 configuration for the HSDAS. Shaded corners represent equipment that is installed and working at JPL.

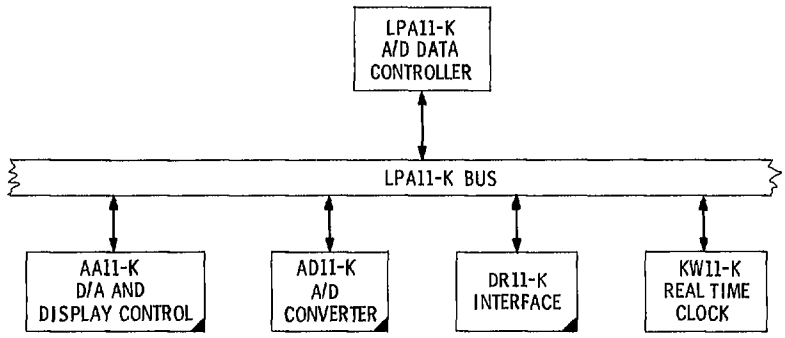

Fig. 4. General purpose data acquisition hardware for the HSDAS. Shaded corners represent hardware that is already installed.

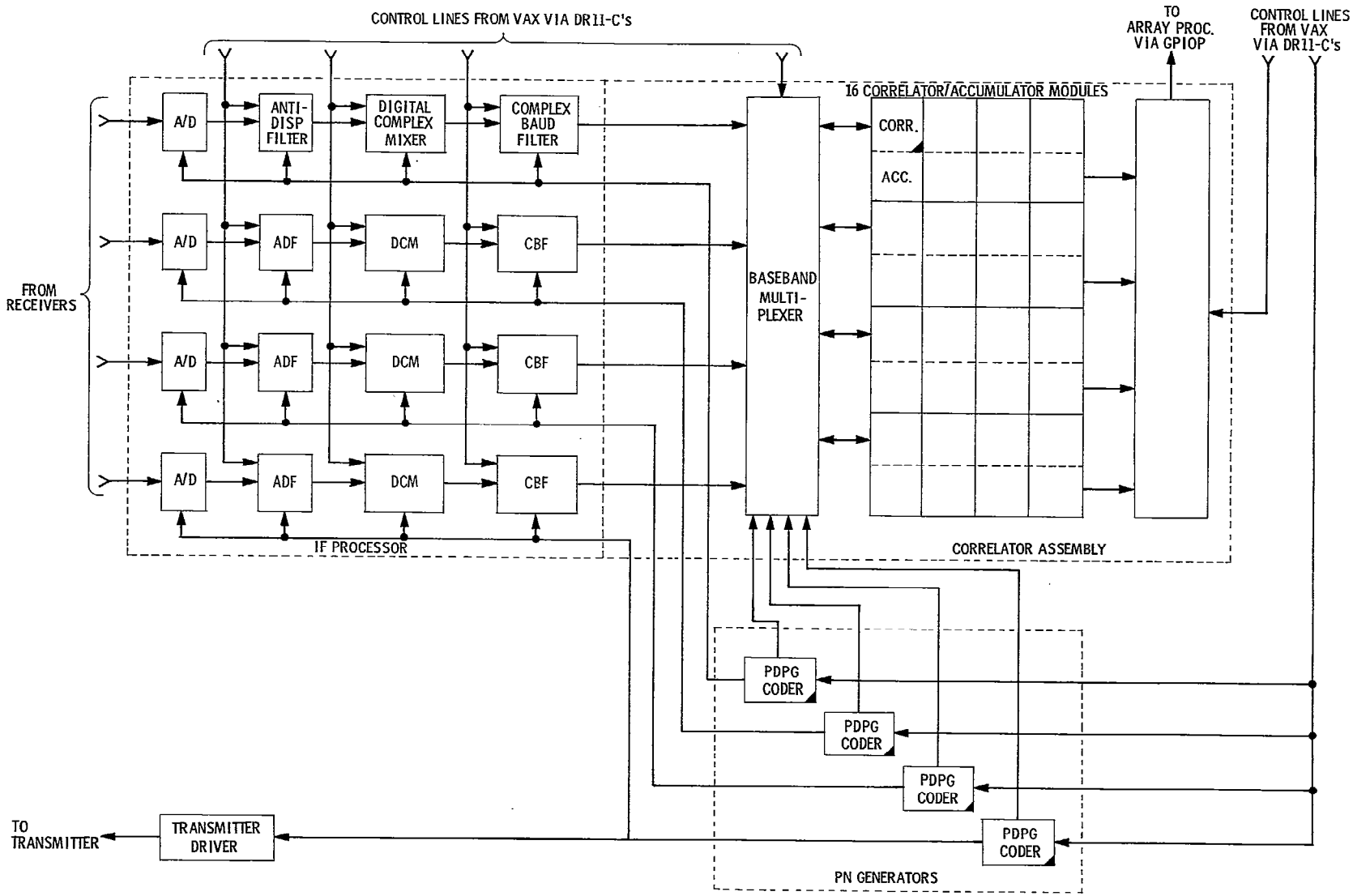

Fig. 5. Special purpose data acquisition hardware. Hardware with shaded boxes has been fabricated and tested.