Demodulator and Accumulator for the High-Speed Data Acquisition System

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In support of nonflight project data acquisition, a new High-Speed Data Acquisition System was designed. The demodulator and accumulator modules are at the heart of this new system and are described in this document.

I. Introduction

The High-Speed Data Acquisition System (HSDAS) is currently being implemented principally to support the DSN Planetary Radar Program (Ref. 1). In the HSDAS, the Polynomial-Driven PN Generators (Ref. 2) will be used to bounce a coded waveform off the radar target. The demodulator and accumulator subsystems are to be used to detect the reflected signals and produce ranging information for further processing.

Each demodulator consists of 16 TRW TCC1023J digital correlator chips configured as 4 by 1 bit auto or cross correlators, with 256 lags. Included on the module is all of the logic and adders required to represent the 256 lag data as a 12 bit offset binary number.

The accumulator module follows the demodulator and allows accumulations of 12 bit offset binary numbers from each lag to a maximum 28 bit number. Each accumulator module supports two demodulators. For the final system there will be 16 demodulator and 8 accumulator modules.

II. The Demodulator

Figure 1 is a block diagram for the demodulator. There are 16 TRW TCC1023J correlators which are configured as 4X1 auto or cross correlators. The autocorrelation function is:

$$C_{(n)} = \sum_{\ell=0}^{256} C_\ell \left[G_{\ell+n}\right]$$

where G_ℓ is a one bit representation of the original data, $G_{\ell+n}$ is a four bit representation of the original data time-shifted, and ℓ is the lag number.

The cross-correlation function is:

$$C_{(n)} = \sum_{\ell=0}^{256} G_\ell \left[H_{\ell+n}\right]$$

where G_ℓ is a binary signal, $H_{\ell+n}$ is a four bit representation of the returned signal time-shifted, and ℓ is the lag number.

The normal modes of operation for the demodulator in the radar acquisition system will be as a cross correlator, when doing delay Doppler gating using the Polynomial Driven PN Generator, or as an autocorrelator when doing continuous wave (CW) detection or radio astronomy.

It will be possible to configure several of the modules within the system to run as a 512 lag or 1024 lag correlator, with both real and imaginary channels. It may even be possible to run 8 by 1 bit correlations.

The correlator chips accomplish the multiply with exclusive-nor logic (Ref. 3). The truth table is shown below.

A	B	$\overline{A \quad B}$
0	0	1
0	1	0
1	0	0
1	1	1

This can be thought of as a multiplier if one replaces 0 by -1 and 1 by +1. This implies that the A/D converter data input to the demodulator should be expressed in offset binary. A conversion table for a four bit 2's complement to offset binary number is shown in Table 1. As can be seen, the transformation only requires toggling the sign bit.

In the demodulator Fig. 1 there are 16 correlator chips broken into 4 groups of 4 chips each. The adder tree that follows sums the results of the correlators into a 12 bit number representing a running total of correlations for four bits over 256 lags.

The correlators also have a mask input so that any number of bits may be masked off and will not be used as part of the total output calculation. This is extremely useful when running short codes since it prevents the multiple copies of unused lags from being summed.

The demodulator uses one master clock which can run as high as 20 MHz. The code, mask, and signal have their own enable inputs to the module. This allows the clock to bring the data as required.

The correlator chips contain two shift-register chains with one isolated from the exclusive-nor logic by a register which can be parallel loaded with the 64 bit serial bit stream in one of the shift-register chains. The signal LDR into the demodulator does this function for 256 lags. This allows a new 256 bit code string to be serially loaded while correlating the first stream, which is being held in the registers.

Figure 2 is a photograph of the demodulator module. The modules for the radar system have been built and tested. They have also been operated successfully in a system test with the Polynomial Driven PN Generators.

III. The Accumulator

Figure 3 is a block diagram of one half of the accumulator module. Each module contains two complete 28-bit wide accumulators. Each accumulator has two buffer memories (double buffered), so that one memory may be unloaded by the computer while the other memory is accumulating data. The accumulation function is:

$$A_{(\ell)} = \sum_{m=1}^{M} C_{(\ell,m)}$$

where $\ell = 1,256$ is the lag number and M is the number of accumulations. M is programmable from 1 to 2^{16}.

The purpose of the accumulator is to allow a correlated signal to be integrated for a period m times longer than the storage length of the correlator.

The control of the accumulator is derived in the computer interface and formating module which is being designed. The accumulator is designed with Fairchild FAST tm logic and 30 ns access time memories. The accumulator will run with a maximum clock rate of 10 MHz.

Figure 4 is a photograph of the accumulator module. The design and construction are complete.

IV. Conclusion

The demodulator and accumulator modules perform the detection and prefiltering of data which will be further processed by a Floating Point Systems FPS 5210 Array Processor. The array processor is also used to form the complete sums when multiple units are used to extend the number of lags or the number of bits in the product table. The High-Speed Data Acquisition System was designed for High Resolution Radar Astronomy. The system has applications in astronomy and possible application for the Search for Extraterrestial Intelligence (SETI) and perhaps RFI monitoring.

References

1. L. J. Deutsch, R. F. Jurgens, S. S. Brokl, "The Goldstone R/D High Speed Data Acquisition System," *Telecommunications and Data Acquisition Progress Report 42-77*, January-March 1984, Jet Propulsion Laboratory, Pasadena, CA.

2. S. S. Brokl, "Polynomial Driven Time Base and PN Generator," *Telecommunications and Data Acquisition Progress Report 42-75*, July-September 1983, Jet Propulsion Laboratory, Pasadena, CA, pp. 84-90.

3. John Eldon, "Correlation . . . A Powerful Technique for Digital Signal Processing," *LSI Publication TP17B-4/81*, TRW LSI Products, TRW Inc., 1981.

Table 1. Conversion table for a four bit 2's complement to offset binary number

Range	2's Complement	Offset Binary
+MAX	0 1 1 1	1 1 1 1
	0 1 1 0	1 1 1 0
	0 1 0 1	1 1 0 1
	0 1 0 0	1 1 0 1
	0 0 1 1	1 0 1 1
	0 0 1 0	1 0 1 0
	0 0 0 1	1 0 0 1
0	0 0 0 0	1 0 0 0
	1 1 1 1	0 1 1 1
	1 1 1 0	0 1 1 0
	1 1 0 0	0 1 0 0
	1 0 1 1	0 0 1 1
	1 0 1 0	0 0 1 0
	1 0 0 1	0 0 0 1
-MAX	1 0 0 0	0 0 0 0

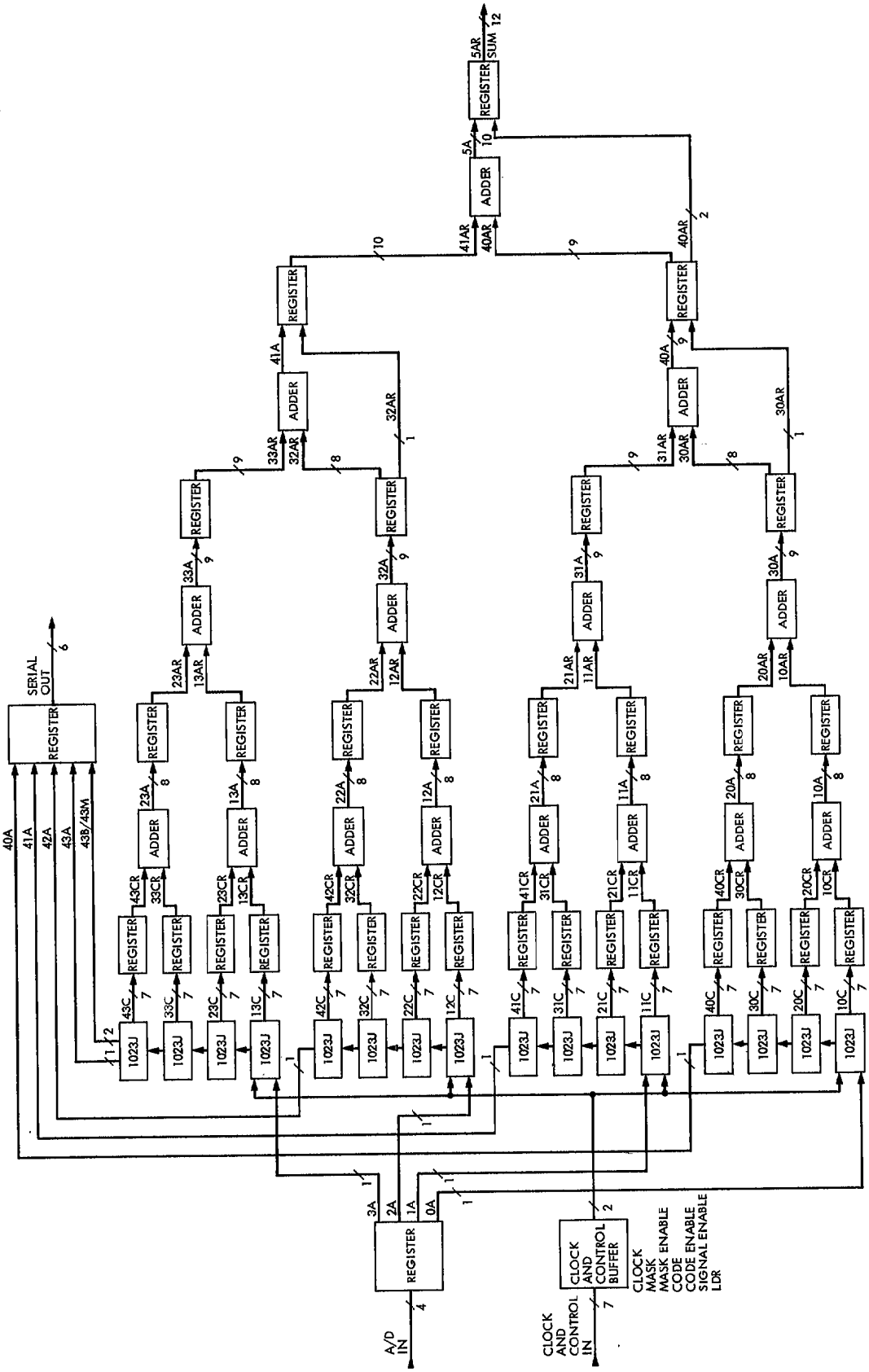

Fig. 1. Demodulator block diagram

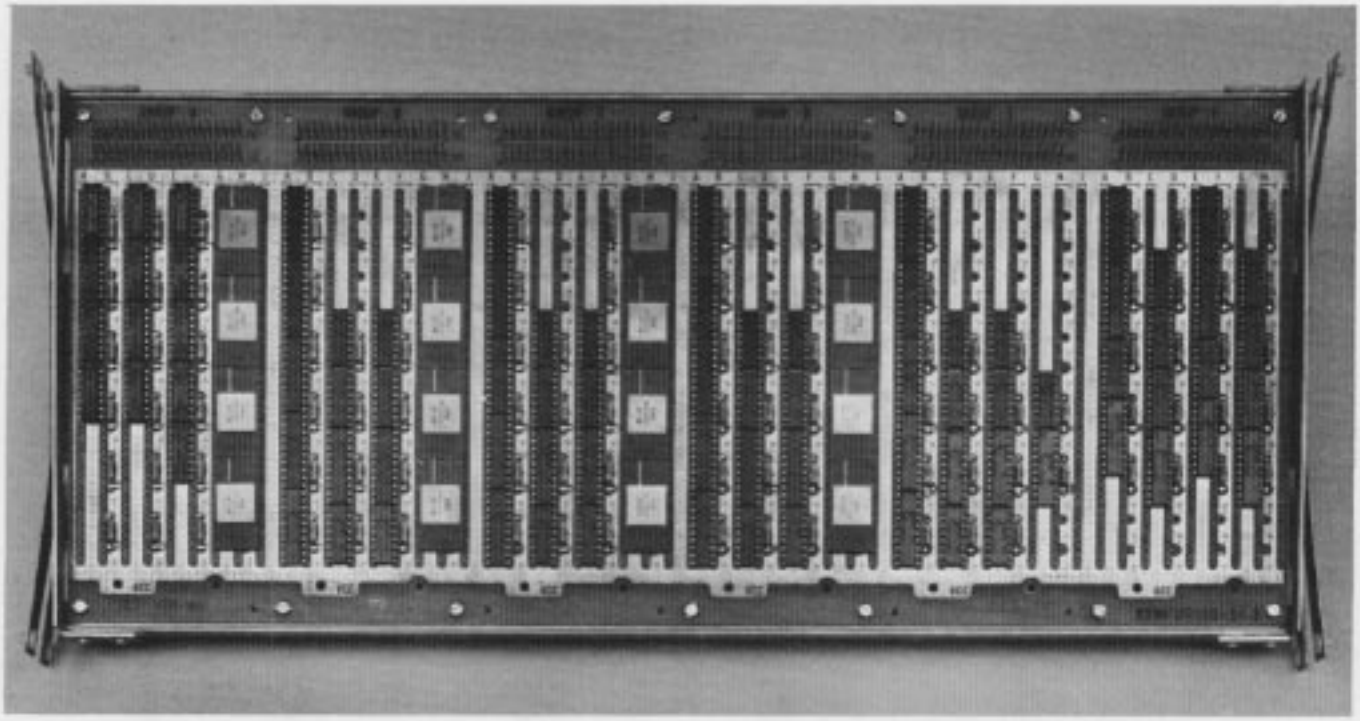

Fig. 2. Demodulator module

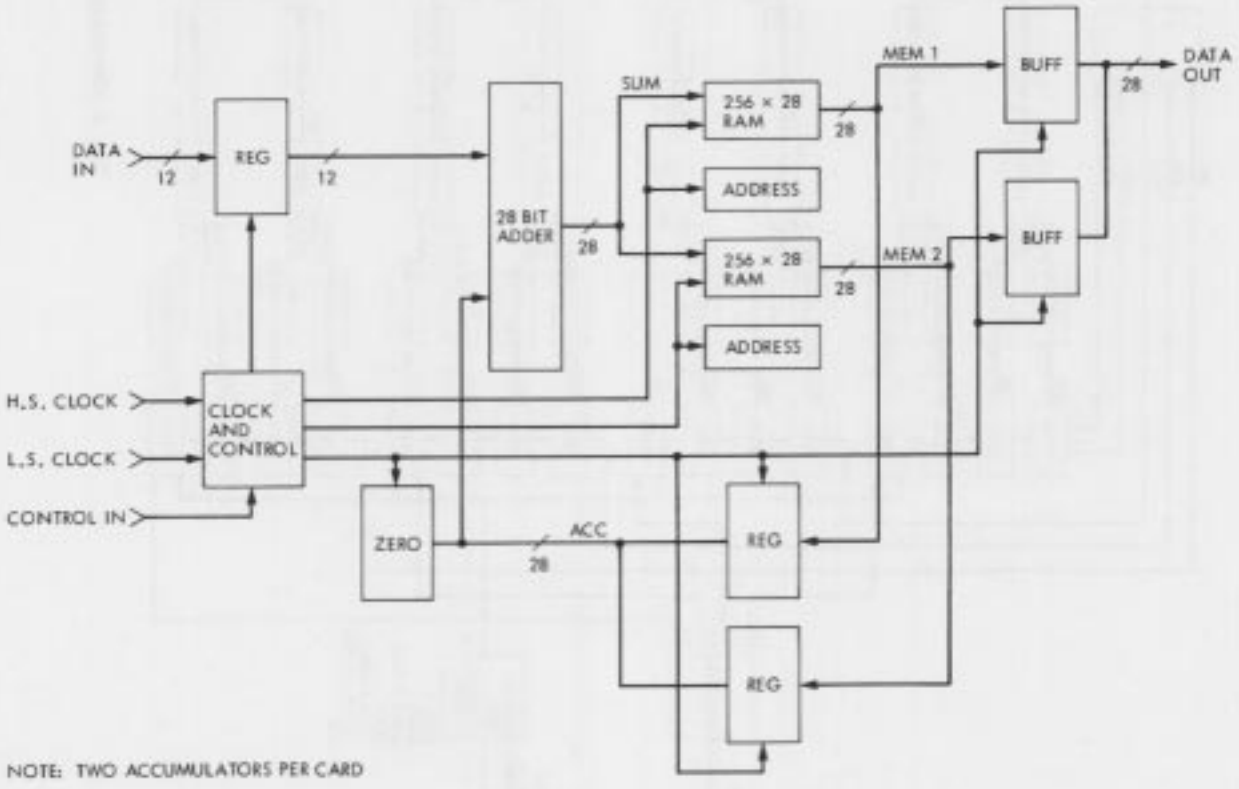

Fig. 3. Accumulator block diagram

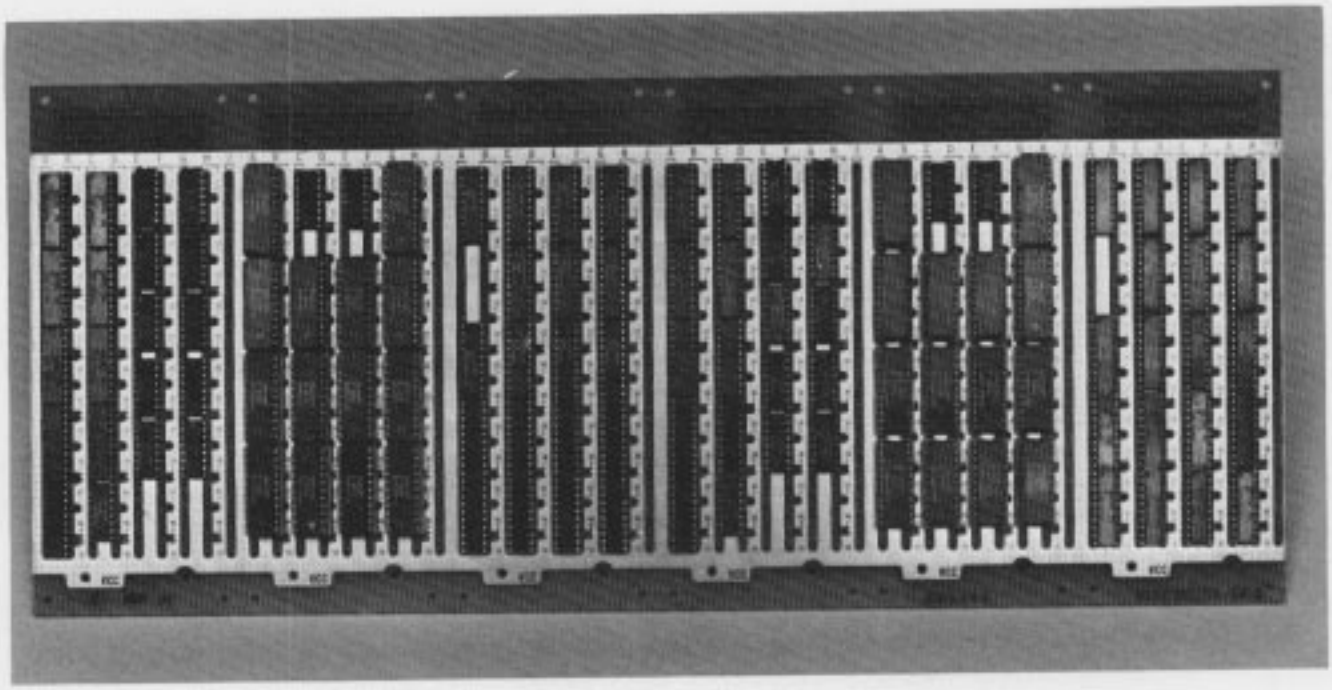

Fig. 4. Accumulator module