A High-Performance Hybrid RF Isolation Amplifier

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A high-performance hybrid RF Isolation Amplifier (Iso-Amp) has been developed at JPL. The circuit exhibits a unique combination of RF characteristics at performance levels exceeding those of any commercially available device. Recent improvements in the design have resulted in significantly higher reverse isolation, a four-fold increase in bandwidth and improved reliability. These devices are very useful in RF and IF signal conditioners, instrumentation, and signal generation and distribution equipment. These Iso-Amps should find wide application in future DSN and R&D RF systems.

I. Introduction

In 1976 a two-stage RF amplifier exhibiting very high reverse isolation and well-controlled impedance levels was designed at JPL.[1] The circuit was hybridized and several hundred of these hybrid Iso-Amps were used in JPL R&D systems including delay-stabilized microwave links for reference frequency distribution and various multiple output distribution amplifiers.

Recently, an additional sixty Iso-Amps were used in an Allan variance frequency stability analyzer where the high reverse isolation of this circuit was needed. Unfortunately, this group of devices, built under contract to JPL, had an unacceptably high failure rate. Within the first few months of operation, four of the sixty hybrid Iso-Amps had catastrophically failed and others were suspected of intermittent bursts of noisy operation. Failure analysis of these four Iso-Amps indicated that the failures were due to poor construction techniques, sloppy component mounting and wire bonding, and little or no quality control. A decision was made to replace all sixty hybrids in the frequency stability analyzer. The replacement parts would have to be built by a firm whose workmanship and quality assurance standards were better than those of the previous supplier.

Prior to interviewing manufacturers of RF hybrid circuits it was decided to see if it might be possible to extend the RF performance of the circuit. The result of this effort was a modified circuit with 10 dB higher reverse isolation and with the upper frequency range extended from 100 MHz to 400 MHz.

After interviewing several leading manufacturers of thick- and thin-film RF amplifiers, a fixed-price contract was let to a corporation in Florida to hybridize the modified Iso-Amp design and produce 300 units. Monitoring of the contractor was provided during the engineering and manufacturing phases by JPL engineering and quality assurance personnel.

[1] By J. MacConnell in JPL's Communication Systems Research Section.

Approximately 100 of the new hybrid Iso-Amps have been installed in the frequency stability analyzer and other R&D systems. No failures have occurred with these units and the improved performance provided by the modified design will benefit future DSN and R&D systems.

II. Functional Description and Applications

There are dozens of companies within the U.S. and abroad which manufacture monolithic and hybrid RF amplifiers. Hundreds of off-the-shelf devices are available which provide the RF engineer with a wide selection of easy to use gain blocks sporting various combinations of gain, bandwidth, noise figure, input and output standing wave ratio (SWR), and output compression level. Packaging options include flat packs, dual in-line devices, transistor outline (TO) cans, and connectorized modules. Recently, a number of wide bandwidth, monolithic silicon RF amplifiers have been introduced which are housed in tiny, 70 mil microwave transistor packages.

With this vast selection of commercially available devices, why would we want to design another RF amplifier? Could our requirements be so different than those of other RF engineers to justify the expense of designing and hybridizing a custom part? In what ways does the performance of the Iso-Amp excel over the commercially available parts?

The hybrid Iso-Amp was designed to have the following characteristics:

(1) Very high reverse isolation (greater than 50 dB at 400 MHz)

(2) Very good input impedance match in 50 ohm systems (input SWR less than 1.10:1)

(3) Output power level capability of at least +16 dBm

(4) Gain of approximately 7 dB

(5) Wide band operation (0.4 to 400 MHz)

(6) Single supply voltage operation with low power consumption (+15V at 45 mA).

(7) Easily inserted package for 50 ohm microstrip systems

(8) Exceptional RF performance at a moderate cost

High reverse isolation and accurate input impedance control were the primary Iso-Amp design goals. Wide bandwidth, large signal handling capability, single supply operation with low power dissipation, and moderate cost extend the usefulness of the part to a broad spectrum of applications.

Reverse isolation is a term describing the reverse transmission loss through a device. It is a measure of the "reverse leakage" of a signal applied at the output of the device and measured at its input. Although the RF designer is normally concerned with signals flowing unidirectionally from inputs toward outpus, there are numerous RF design situations requiring amplifiers which can effectively block those "wrong way" signals.

Multiple-output distribution amplifiers (DAs) accept a single RF or IF input which is amplified and then split to provide several identical outputs. These devices are used in situations where there are multiple users of a single signal. DAs are used, for example, in DSN tracking stations to supply reference frequency signals (originating in a single atomic frequency standard) to many separate pieces of equipment and systems. It is very desirable for the DA to have high isolation between its output ports. This will insure clean, stable outputs on all ports even if one output is corrupted by an unstable terminating impedance, or by signals or noise emanating from poorly designed or faulty equipment. An Iso-Amp placed in series with each of the DA's outputs will provide very high isolation between these ports.

Another application which sometimes requires high reverse isolation is in receiver or instrumentation IF strips. Local oscillator leakage through a mixer may contaminate the preceding RF or IF stages, adversely affecting other users of that signal. An Iso-Amp placed ahead of the mixer will block the LO leakage and maintain the purity of the input signal.

The use of high-isolation buffers is often necessary where RF signals must enter an exceptionally noisy environment. An example of this occurs in frequency-multiplying phase locked loops, where a sample of the voltage controlled oscillator's (VCO's) output signal must be supplied to a digital frequency counter. Switching transients and noise from the digital logic will not only add to the output of the VCO but may modulate the signal as well. This spectral contamination can be avoided by isolating the output of the VCO from the noisy digital circuitry.

Accurately controlled input impedance was also an important design goal in the development of the hybrid Iso-Amp. The Iso-Amp was designed to operate in 50 ohm systems and its input provides an exceptionally good terminating impedance over a wide bandwidth. This characteristic is useful when working with devices whose RF performance is sensitive to impedance levels, such as mixers, reactive filters, equalizers, directional couplers, power splitters, bridges, and transmission lines.

The versatility of the hybrid Iso-Amp stems from its unique combination of RF characteristics. There are, of course, alternate solutions to design problems requiring high isolation, excellent impedance matching, and high output level capability.

High reverse isolation can be achieved by using a cascade of several general purpose RF amplifiers with suitable interstage pads to control the overall gain. Care must be exercised during the design to insure an acceptable noise figure and dynamic range. With proper design, packaging, and construction, high isolation will be realized from the chain of devices. Compared to using a single device, the concatenation will occupy more board space and require more construction time. It will likely consume more power from DC power supplies, dissipate more heat, and have a higher overall parts cost.

Applications requiring a broadband RF amplifier with low input SWR can be satisfied by placing a fixed pad between the signal source and a high-SWR amplifier. If the required input SWR is very low, the pad's value may be large. The overall noise figure of the pad/amplifier combination is increased by the pad's value, and similarly, the gain is reduced by that amount. An additional stage of gain may be necessary to compensate for the lossy, impedance-matching pad. Again, the costs of using this approach include higher circuit complexity and increased design effort.

III. Circuit Description

A schematic diagram of the modified Iso-Amp circuit is shown in Figure 1. The circuit employs two complementary stages to achieve its high reverse isolation, good impedance matching, and large signal handling capability. Recent modifications to the circuit include:

(1) Frequency compensation (resulting in quadrupled bandwidth)

(2) Better transistors (resulting in higher reverse isolation and improved reliability)

(3) Changes in the output biasing (to eliminate a possible source of noise)

(4) Additional power supply decoupling (for improved isolation)

The input stage was designed to provide a good impedance match in 50 ohm systems and to exhibit very high reverse isolation. A pair of bipolar microwave transistors are connected in a common-base, complementary circuit. The input signal is fed through a 44 ohm resistor (R1) to both emitters. With a collector current of 10 mA, the AC impedance looking into the parallel emitters is 6 ohms. The total input impedance is

$$Z_{in} = 44 + 6 = 50 \text{ ohms}$$

DC bias voltages for the input transistor bases are derived from the voltage divider consisting of R3 through R6. The collector current of 10 mA is then established by the emitter resistors (R7 and R8) of 150 ohms each. R9 is the collector load resistor for the first stage. The total AC load presented to the first stage is the parallel combination of this resistor and the input impedance of the output amplifier. The net collector load impedance is 40 ohms and the common-base configuration of the circuit establishes a current gain of unity. This results in a voltage gain of approximately 0.8 (or about −2 dB) for the input stage.

PNP and NPN transistors are used in complementary configurations in both stages of the Iso-Amp. This allows the Iso-Amp to handle large RF signals with good linearity while consuming a modest current from its power supply.

The output structure developed for the Iso-Amp is best described by using separate DC and AC models.

In terms of DC biasing, transistor Q3 and its associated circuitry operate as a current source. Resistors R11 and R12 form a voltage divider across the supply voltage, holding Q3's base at about +11.5 volts. Approximately 2.75 volts appear across the series combination of R16 (68 ohms) and R17 (20 ohms) resulting in an emitter (and collector) current of 31 mA. This DC bias current is fed to the collector circuit of transistor Q4.

Approximately 5 mA of this current are diverted through the resistive divider consisting of R13 (390 ohms), R14 (820 ohms), and R15 (300 ohms). The DC voltage seen by the base of Q4 is proportional to the voltage appearing on its collector. In operation, the voltage at Q4's collector will rise to a level sufficiently high that its base voltage overcomes the base-emitter drop of 0.8 volts. At this point, Q4's increasing conduction slows the rise of collector voltage. Bias equilibrium is attained when the collector voltage reaches +7.5 volts. This circuit creates a "stiff" voltage source and the final collector voltage is quite insensitive to bias current changes.

The biasing arrangement of the output stage is, then, a current source driving a voltage source. This leads to a very stable DC operating point for the transistors. Collector current and collector voltage are independently controlled with this arrangement and each is accurately maintained over normal variations of power supply voltage and temperature.

Consider the AC model of the output stage. The two transistors operate in parallel. Examination of the schematic reveals that, for AC signals, both transistor bases are tied together, as are the emitters and collectors. The output stage can therefore be analyzed as if it were a single transistor amplifier employing emitter degeneration and collector voltage feedback. The voltage gain of this stage is given by:

$$A_v = \frac{-R_c}{R_e}$$

where

R_c = the collector load impedance

and

R_e = the total emitter impedance

The input impedance of this stage is

$$Z_{in} = \frac{R_f}{1 + A_v}$$

where

R_f = the unbypassed feedback resistance

and

A_v = the voltage gain of the stage

With the component values shown in Fig. 1, the second stage input impedance is 68 ohms (including the loading caused by bias resistors) and its gain is approximately -2.8 V/V, or 9 dB.

The net gain of the complete, two stage Iso-Amp is

$$G_{\text{Iso-Amp}} = -2 \text{ dB} + 9 \text{ dB} = +7 \text{ dB}$$

IV. Breadboard Activities

Several changes in the Iso-Amp design were introduced during the recent modifications which resulted in improved RF performance. A number of breadboard circuits were built and tested during this activity. The first breadboards were built on copper-clad substrates using leaded components. Component leads and interconnecting wires were kept as short as possible to minimize signal radiation and parasitic inductance.

Once a candidate design was obtained, it was clear that a better breadboarding technique would have to be employed during the final circuit refinements and RF performance verification. The deleterious effects of component leads and the layout restrictions imposed by using packaged devices were clearly affecting the circuit's RF performance at frequencies beyond about 250 MHz. A better breadboarding technique was also desired to simplify replication of the circuit. Several identical breadboards had to be built and tested to determine the repeatability of the design's RF performance.

A two-sided printed circuit board was designed for the final breadboarding activities. Chip capacitors, 1/8 watt carbon composition resistors, and microwave transistors were surface mounted on the 4.0 × 2.8 cm (1.6 × 1.1 inch) boards. Plated through holes provide low inductance connections to the solid ground plane on the back of the boards. Several of these final breadboards were built and tested, confirming the repeatability of the modified design's RF performance. One of these breadboards is shown in Fig. 2.

V. Hybrid Circuit Implementation

The internal circuitry of one of the new hybrid Iso-Amps is shown in Fig. 3. The metal cap which would normally be welded in place over the circuitry was left off of this sample part. A 12-lead, circular TO-8 hybrid package measuring 1.52 cm (0.600 inch) in diameter provides the hermetically sealed environment for the thick film circuit.

All circuit elements within the hybrid circuit are either printed on or mounted on an alumina substrate measuring approximately 0.91 × 0.91 × 0.038 cm (0.36 × 0.36 × 0.015 inch). Initial processing of the substrates is performed on arrays of 9 or more substrates. Conductive circuit traces are added by the thick film process wherein gold-bearing ink is screened onto the substrate arrays in a pattern matching the desired metalization. Volatile solvents are subsequently removed in a drying process. The arrays are then fired at high temperature in an inert atmosphere, fusing the gold alloy conductors to the alumina substrates.

Thirteen of the nineteen resistors in the circuit are thick film and the balance are thin film devices. The thick film resistors are printed on the arrays with resistive inks. The ends of each resistor overlay the edges of conductors establishing the circuit connections. The substrate arrays are again dried and fired in a process similar to the one used for the circuit conductors. Initial resistance values are intentionally made slightly lower than desired since the thick film resistors are subsequently laser trimmed to their final values.

Chip capacitors, thin film resistor networks, and transistor dice are bonded to the substrate arrays with electrically conductive epoxy. The arrays are separated into individual substrates which are then bonded to the metal headers of the hybrid packages. Additional circuit connections are added with gold wirebonding. Due to the very small wirebond pads on the microwave transistors, 0.0018 cm (0.0007 inch) diameter gold bond wire is used to make base and emitter connections on all transistors. Other wirebonding, including connections to the header's base and pins, is performed with 0.0025 cm (0.001 inch) diameter gold wire.

Following inspection and initial electrical testing, the hybrid circuits enter an oxygen free environment where the metal covers are electrically welded to the headers, hermetically sealing the integrated circuit. Final electrical testing and case labeling are the last steps in the manufacturing process.

VI. Electrical Performance

Table 1 shows the typical RF performance of the hybrid Iso-Amps. Differences between the breadboard and hybrid Iso-Amps are insignificant with the notable exception of the reverse isolation. The reverse isolation of the hybrids is typically three or four dB lower than the performance obtained with the breadboard circuits. This may be due to slightly better grounding in the breadboards or it may be a consequence of shrinking the size of the circuit to a tenth of a square inch and mounting it in a package whose input and output pins are separated by only 1.0 cm (0.4 inch). A stray coupling capacity of only 0.05 picofarads between the RF input and output pins would, in fact, limit the device's isolation to about 62 dB at 100 MHz (a typical value for these hybrid Iso-Amps).

The two port scattering parameters of a typical hybrid Iso-Amp are given in Table 2.

VII. Applications Considerations

Since the hybrid Iso-Amp was designed to operate with relatively low power consumption, heat sinking is generally not a problem. In most applications the hybrid is soldered into a microstrip circuit board, with the base (header) of the circuit in intimate contact with a copper clad ground plane. This mounting configuration provides adequate heat sinking for the circuit without resorting to metal clamps or special heat sinks sometimes required with higher dissipation devices. Thermal resistance at the case/ground plane junction can be further reduced by adding a small amount of heat sink grease at this point when mounting the circuit. This precaution protects the Iso-Amps when they are operated in high temperature environments.

Some applications require higher reverse isolation than a single Iso-Amp can supply. Simply cascading a pair of these devices on a microstrip board does not double the reverse isolation. Signal leakage between output and input microstrip traces limits the isolation. Imperfect grounding and insufficient power supply decoupling can also adversely affect the cascade's ultimate isolation. Careful design, layout, and shielding can, however, yield Iso-Amp cascades with very high isolation.

Shown in Fig. 4 is an isolation amplifier module developed for the Allan Variance Frequency Stability Analyzer. Contained within this module are two independent cascades consisting of a concatenated pair of the hybrids with an interstage pad to control the overall gain. Careful attention to grounding, power supply decoupling and shielding (including beryllium-copper finger stock shields) was necessary to achieve reverse isolations in excess of 110 dB at 100 MHz.

VIII. Conclusion

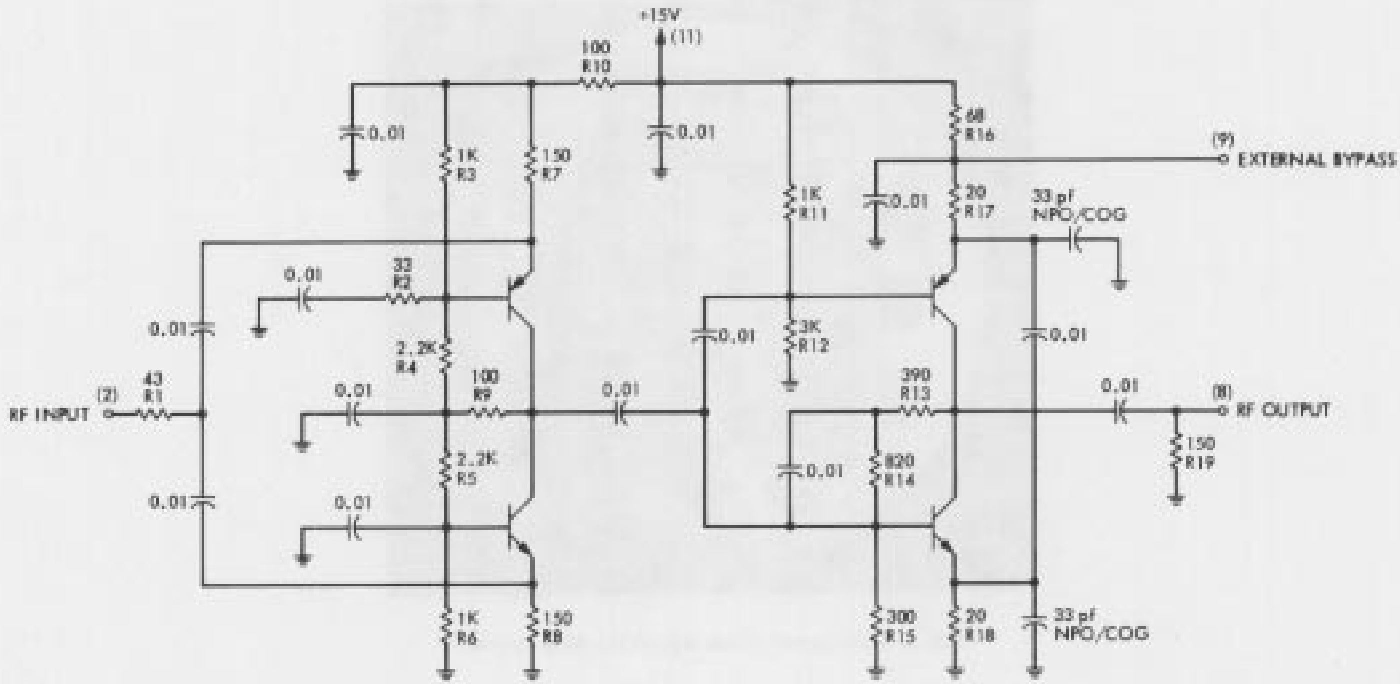
The hybrid RF isolation amplifier described in this article exhibits a unique combination of RF characteristics in a single easy to use package. This circuit provides an economical solution to many RF design problems requiring high reverse isolation, good impedance matching and high output level capability. Useful over a frequency range spanning ten octaves, these hybrid amplifiers should find wide application in future DSN and R&D RF systems.

Table 1. Hybrid Iso-Amp typical RF performance

Gain	7 dB
Frequency Response	Flat to within 0.5 dB from 2.0 to to 350 MHz -1.0 dB at 1.3 and 400 MHz -1.0 dB at 0.4 MHz with external 0.1 microfarad bypass capacitor from pin 9 to ground
Reverse Isolation	85 dB at 3 MHz 62 dB at 100 MHz 51 dB at 400 MHz
Input SWR	Less than 1.1 from 3 to 400 MHz
Output SWR	Less than 1.75 from 3 to 100 MHz
1 dB Output Compression Level	Greater than +16 dBm
Third Order Intercept Point	+27 dBm
Noise Figure	12.5 dB
DC Power	+15 V at 45 mA (Dissipation = 675 mW)
Package	1.52 cm (0.6 in.) diameter, 12 lead, hermetic TO-8

Table 2. Typical hybrid Iso-Amp scattering parameters

Frequency,	Input Return (S11)		Forward Gain (S21)		Reverse Isolation (S12)		Output Return (S22)	
MHz	dB	Angle	dB	Angle	dB	Angle	dB	Angle
3	-28.0	-138	7.06	-176	-87.3	16	-27.6	-145
20	-30.6	-178	7.00	175	-76.0	58	-27.5	-142
100	-31.1	146	7.29	155	-62.4	69	-17.5	-133
200	-31.0	117	7.56	129	-56.7	62	-12.5	-155
300	-30.2	96	7.46	100	-54.4	53	-10.3	178



NOTES: NUMBERS IN PARENTHESES ARE PACKAGE PIN NUMBERS
CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE NOTED
PNP TRANSISTORS ARE TYPE NEC 88900 (CHIP)
NPN TRANSISTORS ARE TYPE NEC 02100 (CHIP)
HYBRID PACKAGE IS 1.52 cm (0.600 inch) DIAMETER, 12 LEAD, HERMETIC TO-8
GROUND = PINS 1, 3, 4, 5, 6, 7, 10, 12, AND CASE
ALL HYBRID GROUND PINS SHOULD BE CONNECTED TO GROUND PLANE

Fig. 1. RF Iso-Amp schematic diagram

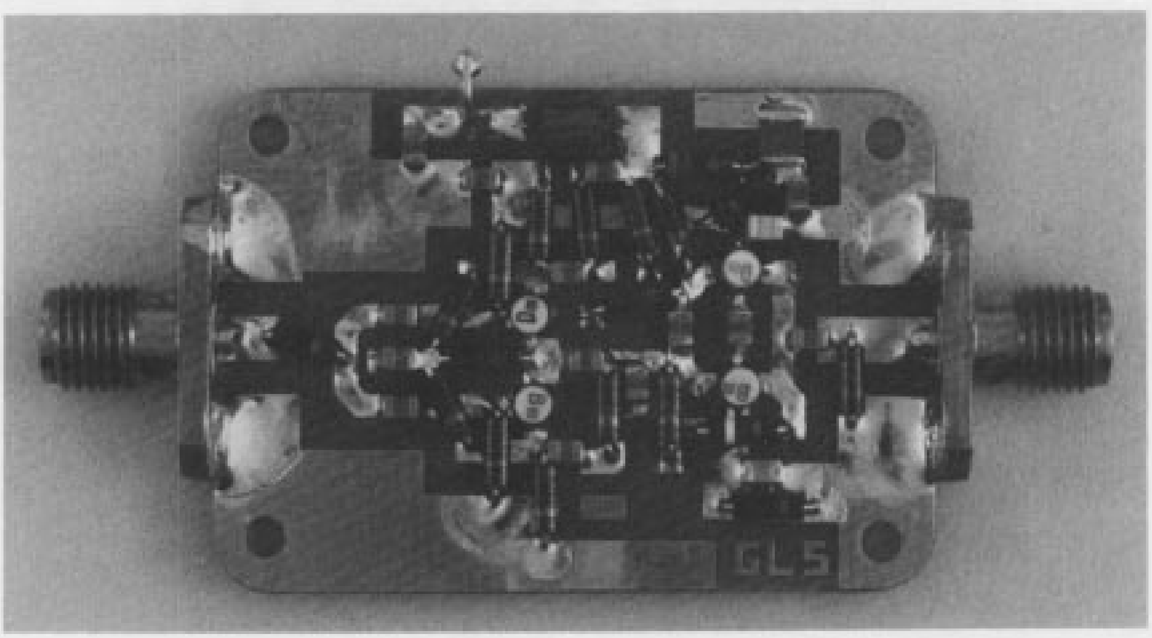


Fig. 2. RF Iso-Amp breadboard

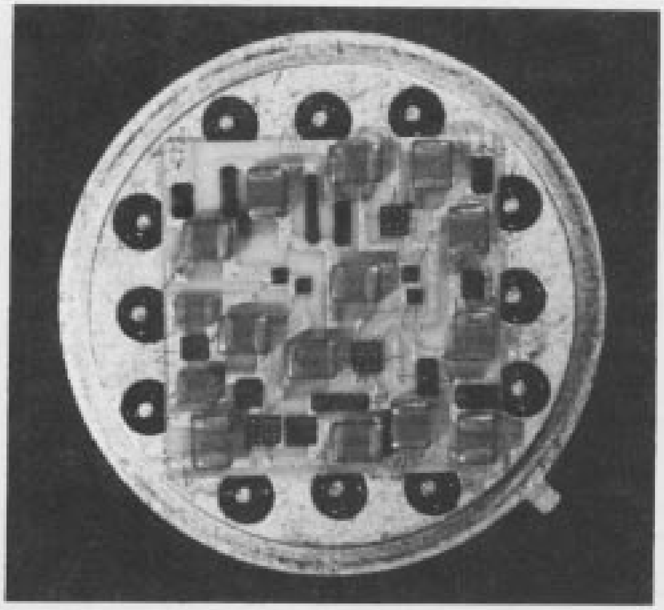


Fig. 3. Photograph of the hybrid Iso-Amp circuitry

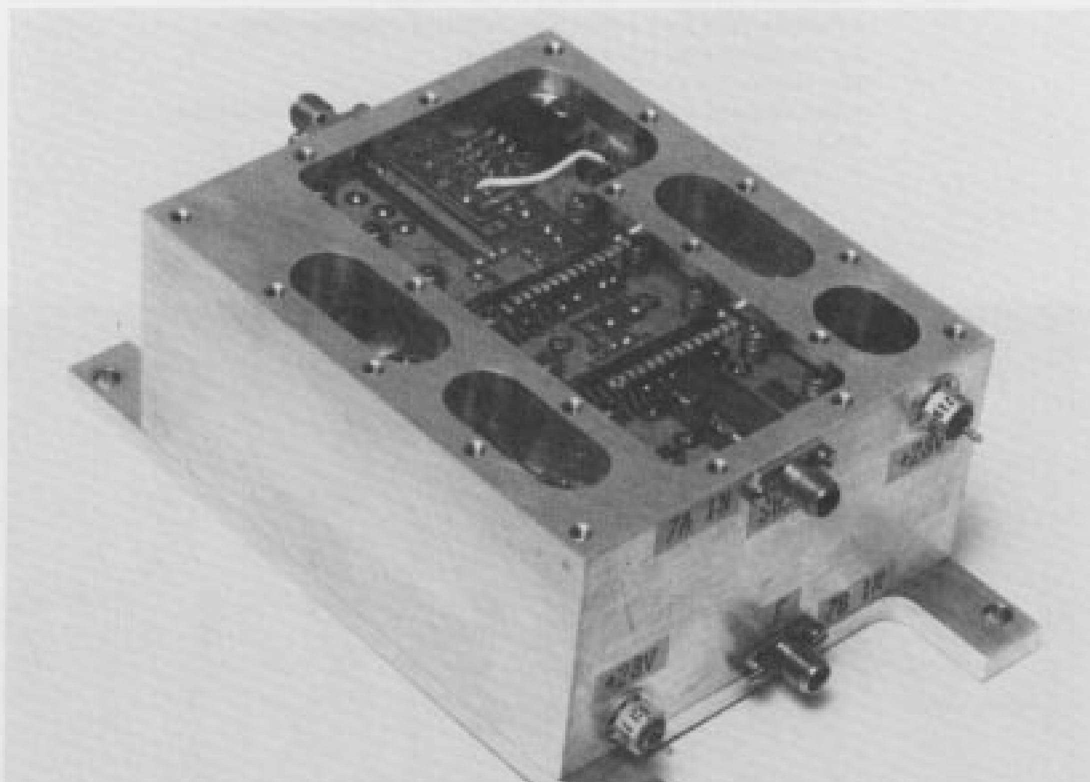


Fig. 4. Isolation Amplifier module for the Allan Variance Frequency Stability Analyzer