Symbol-Stream Combiner: Description and Demonstration Plans

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A system is described and demonstration plans presented for antenna arraying by Symbol Stream Combining. This system can be used to enhance the signal-to-noise ratio of spacecraft signals by combining the detected symbol streams from two or more receiving stations. Symbol Stream Combining has both cost and performance advantages over other arraying methods. Demonstrations are planned on Voyager II both prior to and during Uranus encounter. Operational use is possible for Interagency Arraying of non-DSN stations at Neptune encounter.

I. Introduction

Symbol-Stream Combining (SSC) is a method of combining the received signals from two or more antenna-receiver systems in order to achieve a signal-to-noise ratio (SNR) which is approximately equal to the sum of the signal-to-noise ratios at each antenna-receiver. The primary motivation for SSC is interagency arraying of non-DSN and DSN stations for the Voyager Neptune encounter.

This article describes the symbol-stream combining system concept, the hardware and software implementation, and the preliminary demonstration plans.

In Symbol-Stream Combining, the received signals at each antenna station are processed through symbol detection. Then the detected symbols from the two or more stations are brought together, aligned, and combined with proper weighting. This is as opposed to Baseband Combining (BBC), in which the signals are brought together, aligned, and combined as broadband baseband signals prior to subcarrier demodulation.

Symbol-Stream Combining has three major advantages over Baseband Combining. First, the ground communication bandwidth for SSC is less than one-tenth of that for BBC. This is a major cost reduction, especially when international satellite links are required. Second, the SSC combining and backup recording equipment is less complicated and less expensive. Third, the SNR performance is approximately 0.35 dB better for SSC than for BBC, as shown by Divsalar (Ref. 1). The main disadvantage of SSC is that the subcarrier demodulators and symbol synchronizers must operate at lower SNRs than for BBC; this disadvantage will be overcome by use of synchronization techniques being developed for the DSN Advanced Receiver (Ref. 2).

Figure 1 shows the planned configuration for the first demonstration of SSC, using DSS-13 and DSS-14. Voyager 2 will be tracked by both stations. The symbol-stream combiner will be located at DSS-14. The signal at DSS-14 will be processed by a standard telemetry stream through symbol detection. Then the detected symbol stream will be input to the Symbol-Stream Combiner (SSC). The signal at DSS-13

will be synchronized and the symbols detected using a partial breadboard of the Advanced Receiver signal processing unit. These detected symbols will be transmitted to DSS-14 on the existing microwave link and input to the SSC. The combined symbols at the output of the SSC will be input to a decoder, and the symbol stream from DSS-14 only will also be decoded. Either two decoders will be used simultaneously, or one will be time shared. The decoder performance will be monitored to establish the SNR improvement achieved by SSC.

II. System Description

One of the main advantages to the symbol stream combining method of antenna arraying is the simplicity of the hardware necessary for the implementation of the system. Because SSC is performed on the quantized symbols after subcarrier demodulation and symbol synchronization, the data rate into the SSC is equal to the symbol rate, which is under 60 kHz for Voyager Uranus encounter. This is much lower than the 15 MHz sampling rate of the Baseband Assembly (BBA), which implements Baseband Combining. Thus, functions performed in hardware in the BBA can be done in software in the SSC. These software functions include cross correlation for alignment and SNR estimation. The SSC also performs SNR estimation, in software, on the input symbol streams to determine the weighting constants to be used in the hardware for the combining.

The basic functions that must be carried out in SSC are alignment of the quantized symbol streams, weighting of each symbol, and combining or summing the weighted symbols. The combining function is as follows:

$$Z(n) = a_0 X_0(n) + a_1 X_1(n+k)$$

where

0, 1 = station index

X_i = symbols from station i

Z = combined symbols

n = time index for nth symbol

k = delay to station 1 from station 0

a_i = weighting constant for station i

The weighting constant is computed in the SSC using the algorithms analyzed by Q. D. Vo (Ref. 3). The above relation is implemented in hardware with software control and computation of values for a_0, a_1, and k. Alignment is accomplished by delaying the $X_1(n)$ stream by k samples with respect to the $X_0(n)$ stream. The value of k is determined by software cross correlation of the two streams and by utilizing delay calculations based on antenna pointing predicts and knowledge of the vector baseline between the antennas. Once the value of k is determined, weighting and combining is performed in special purpose hardware.

III. Hardware Description

The special hardware is a multibus board which was developed for the BBA for the combining and weighting of sampled data and a special delay card developed for this project. A block diagram of the hardware configuration is shown in Fig. 2. The hardware consists of a multibus card cage with seven standard and two special purpose cards, two disk drives, two function generators, and an interface assembly. The standard cards are:

1 INTEL SBC-86/14 Single Board Computer with an 8087 Multimodule

1 Chrislin Industries CI-8086 512 KByte Dynamic RAM Card

1 National Semiconductor 8222 Disk Controller

1 INTEL SBC-534 I/O Expansion Card

2 SBX-488 Multimodule interface cards for controlling the function generators

1 Digital Pathways TCU-410 Clock Calendar Card

The two special multibus cards are a Programmable Digital Delay Card and a Multiplier-Adder Board for combining. Two eight-inch Shugart Disk Drives are used also.

A custom interface assembly to interface to the microwave link at the stations and generate test sequences for system self-test is also shown. The two function generators supply clock signals. One supplies a times-four clock, phase locked to the channel-0 symbol clock. The other supplies a test signal clock for channel 1 during self-test.

A. Delay Card

The function of the Delay Card is to input two symbol streams, buffer them, delay one stream with respect to the other so as to align the corresponding symbols from the two sources, and to output the two aligned symbol streams to the Multiplier-Adder Board.

A diagram of Delay Card signal flow is shown in Fig. 3. The card consists of two independent channels so two streams can be delayed simultaneously. Each channel has a first-in-first-out (FIFO) circular buffer memory, a read address

counter and a write address counter. Channel 0 is set at a fixed delay of k_0 symbols, depending on the particular stations being arrayed. This fixed delay is greater than the maximum allowance (negative k) for the baseline. The channel-1 data are delayed $k_0 + k$, which is always positive. The differential delay is k, as required.

The main complexity in the Delay Card arises because the symbol rates from the two stations are slightly different due to Doppler shift. This Doppler shift or changing delay is caused by Earth rotation. The differential fractional Doppler between stations is on the order of 10^{-9} for two Goldstone stations, and up to 2×10^{-6} for widely separated stations. Thus, the delay changes by one symbol time in 10^6 to 10^9 or more symbols. In each channel-0 symbol time, there is almost always one channel-1 symbol, but occasionally there are zero or two channel-1 symbols.

The Delay Card operates synchronously with the symbol-stream clock from channel-0. A clock at four times the symbol-0 clock is input to the Delay Card. This clock is divided into four phases, a read phase, two write phases (W0 and W1), and a do-nothing phase.

The operation for channel-0 symbols is straightforward. During each channel-0 symbol time, the newly arriving symbol is written into the buffer on write phase W0, and one symbol is read out on the read cycle.

The situation for channel-1 input is more complicated. The channel-1 symbols arrive asynchronously to the times-four clock. They are first synchronized to that clock using a shift register. As the channel-1 symbols are synchronized, a Data-Ready signal is generated for each symbol. Then, on the next write phase, either W0 or W1, the symbol is written into the channel-1 buffer and the Data-Ready signal is turned off. Thus, there are two opportunities to write into the channel-1 buffer during each channel-0 symbol time, but 0, 1, or 2 writes occur depending on the number of channel-1 symbols arriving.

One symbol is read out of the channel-1 buffer on each read phase, i.e., at the same instant as the corresponding channel-0 symbol is read. The synchronization delay for channel-1 is denoted by ϵ. The FIFO buffer delay is $k_0 + k - \epsilon$. Finally, the differential delay between the two channels is k, as desired.

B. Multiplier–Adder Board

The Multiplier-Adder Board performs the weighting of the symbol streams and summation of the weighted streams to produce the combined output. This card is similar to the BBA Multiplier-Adder Board (MAB), with a minor modification to enable 8086 addressing rather than 8080 addressing. The MAB can combine up to four symbol streams and can be used with an additional MAB to combine up to eight streams. The card performs 8-bit multiplication on input data streams with weighting function values input from the 8086 over the multibus. The card then performs sums on these data to produce the combined results. In addition, the MAB provides circuitry for capturing either input data to the card or data at a selected point in the computation and transferring these data over the multibus to the computer. This enables the software to acquire the symbols for use in the cross correlation and SNR estimation computations. The weighting coefficients are returned to the MAB from the software.

C. Interface Assembly

The interface assembly provides two interfaces between the SSC Delay Card and the microwave link or a local symbol synchronizer assembly (SSA). The interface assemblies also generate psuedorandom test patterns for self-test of the data paths, under computer control.

For flexibility and reliability, both interfaces can input either SSA or microwave link data. The interfaces use Zilog Z8530 Serial Communication Controllers for parallel-to-serial and serial-to-parallel conversion, and Computrol modems for FSK modulation and demodulation of the microwave link signal. The Z8530 is used to send and receive the streams using a standard SDLC protocol.

IV. Software Description

The SSC software is composed of modules that perform operator interfacing, calculation, and control functions. The software organization is shown in Fig. 4.

The operator communicates with the system through a series of menus and prompts. After the operator has made the necessary key-ins and has selected the option to align the incoming data streams, the program takes over. First, the SNR Estimation Module computes SNR estimates and combiner weight values. Next, the Delay Calculation Module computes delay values from the input antenna predict information. These values are used to initialize the boards. Then control passes to the Alignment Module, which consists of the Correlation and Control Submodules. Control passes between these submodules until the streams are aligned or the operator intervenes. During the alignment process, operator displays including SNR estimates, correlation values, and delay estimates are constantly updated.

A. Environment

The program operates under the CP/M-86 operating system. As much software as possible is written in Pascal MT+86, with low-level interface routines written in 8086 assembly language. In critical areas where bottlenecks might occur, assembly language is used for speed.

B. Operator Interface

The operator has the option of using built-in default values or entering his own values for most system variables. Variables such as SNR estimates or antenna pointing predicts can be entered through the keyboard or from a data file that the operator specifies. Upon power up, the operator can enter either a test mode or the Real Time Combiner (RTC) mode. From the main menu the operator can also display system date and time. The SNR Estimation and Delay Calculation Modules can also be run individually with results displayed to the operator, for testing. Operator displays take the form of changing real time displays that can be viewed during the test mode or the RTC mode. Operator control is maintained via the keyboard.

The ability to write test data to disk is available in either the test mode or the RTC mode. Data written to disk consist of system variables, raw data, combined data, computed results, time, date, test identification, such as test name or number, and a small field for comments.

C. Mathematical Modules

There are three mathematical modules, the Delay Calculation Module, the SNR Estimation Module, and the Alignment Module.

1. Delay Calculation Module. Due to the geographical separation of the receiving stations, spacecraft signals arrive at one station later than the other. That delay and the delay associated with transmitting the received data stream from one station to the station at which the SSC equipment is located require that one stream be delayed to allow proper alignment with the other stream. The Delay Calculation Module takes as input two DSS station names and antenna pointing predicts associated with each station. The geometrical delay is calculated using the predicts and the baseline vector between the two stations. It is necessary to perform this calculation only for acquisition because the hardware maintains delay synchronization after acquisition. Transmission delay time between stations and cabling delay times for each station are also accounted for. A database containing this information is maintained on disk.

2. SNR Estimation Module. The SNR Estimation Module computes an estimate of SNR for each incoming data stream. Using a number of raw data samples from the MAB, it computes an estimated SNR and then weighting constants for each data stream. It also computes the output SNR. The algorithms used are those developed by Q. D. Vo (Ref. 3).

3. Alignment Module. The Alignment Module consists of the Correlation Module and the Control Module that aligns the data streams. It accepts delay estimates from the Delay Calculation Module for initial alignment. It then uses the Correlation Module to determine the exact delay, which will be close to the delay input from the Delay Calculation Module, and aligns the symbol streams accordingly.

The Correlation Module reads the two symbol streams from the MAB, correlates them, and decides if the streams are aligned. This decision is based on a correlation threshold value which can be changed by the operator. If the streams are aligned, then this program is left and the tracking/combining mode is entered. If the streams are not aligned, then the delay is changed by a software algorithm, and the process is repeated until alignment is achieved.

The Control Module takes delay values from the Correlation Module and computes values for the read and write counters for the registers on the Delay Card. It stops the delay function on the card, resets the counters to the desired values, restarts the delay function on the card, and returns to the Correlation Module. It also accepts new weight values from the Correlation Module and loads them to the MAB. During the alignment process, this module forms the one control point for access to both the MAB and the delay card.

D. Interface Modules

The two main interface modules are the modules that communicate with the MAB and the Delay Card. They perform the low-level control functions to pass data and commands between the high-level PASCAL software and the hardware. The MAB can operate in a test mode or a combiner mode. In its test mode, outputs to the board consist of start and stop test commands and values for the on-board test and weight registers. Input from the MAB in its test mode consists of intermediate and final results from the adder trees and status information. Output in the combiner mode to the board consists of multiplier constants for the weight registers, and input consists of the raw data symbols, intermediate adder tree results, and combined data symbols.

The Delay Card is controlled by outputs to the card consisting of values loaded into the read and write counters for each delay buffer and commands to enable or disable the delaying function of the card.

Testing of both the interface modules and the cards themselves is controlled by low-level menus built into the software

modules. The Delay Card test menu allows the operator to load the read and write counters for each channel directly and to enable or disable the delaying function for each channel. The MAB has the circuitry on board to generate its own input to the adder tree. A static test or a dynamic test can be conducted. Intermediate results can be read from seven different points in the adder tree.

There are two other smaller hardware interface modules. One allows the operator to view and change the system date and time which are maintained on the Timing and Control Unit (TCU) board. The other interfaces the two HP 3314 Function Generators via two SBX488 GPIB modules. This allows the function generators to be under program control.

V. Preliminary Demonstration Plans

Initial demonstration of SSC is planned for the first quarter of calendar year 1985, using DSS-13 and DSS-14. Prior to the first combining demonstration, the SSC will be laboratory-tested, and the microwave link interfaces and other station interfaces will be checked out. Several SSC demonstrations are planned for the first half of 1985.

The desired operating conditions are that the symbol SNR at DSS-14 be approximately -2 to +3 dB, and that the symbol SNR at DSS-13 be approximately -10 to -5 dB. Thus, the breadboard of the advanced receiver telemetry processor is required at DSS-13 in order to achieve subcarrier and symbol synchronization at low SNR with low degradation. If the advanced telemetry processor breadboard is not ready when desired, an alternate configuration using DSS-12 and its standard telemetry processing system will be used for a first demonstration. This would demonstrate the SSC technique, but not the ability to use a very low SNR station. The low SNR capability would be demonstrated when the advanced telemetry processor breadboard becomes available.

Tentative plans are being developed to use the SCC during Voyager Uranus encounter in January, 1986. This usage could be in a backup mode to BBC between Goldstone stations or could be to array Owens Valley Radio Observatory or DSS-13 into the Goldstone array. Either configuration would be on a nonoperational basis.

A major goal of these demonstrations is to make symbol-stream combining a viable option for implementation of Interagency Arraying for the Voyager Neptune encounter.

References

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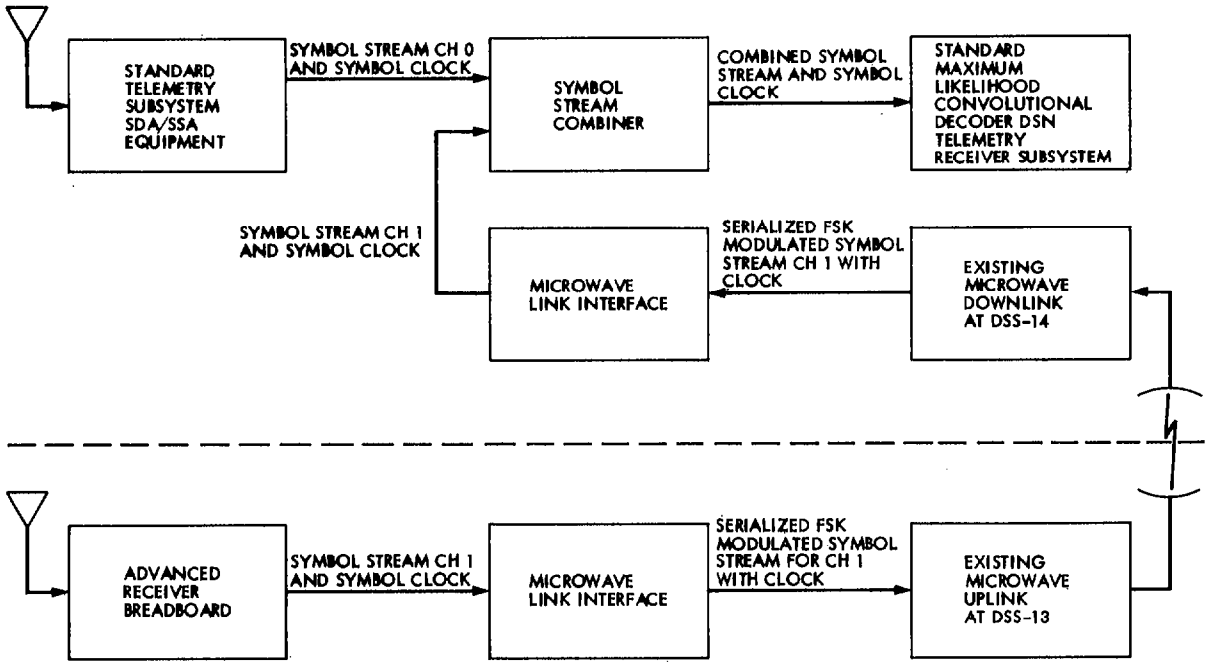

Fig. 1. Symbol-stream combiner demonstration station configuration block diagram for DSS-14 and DSS-13

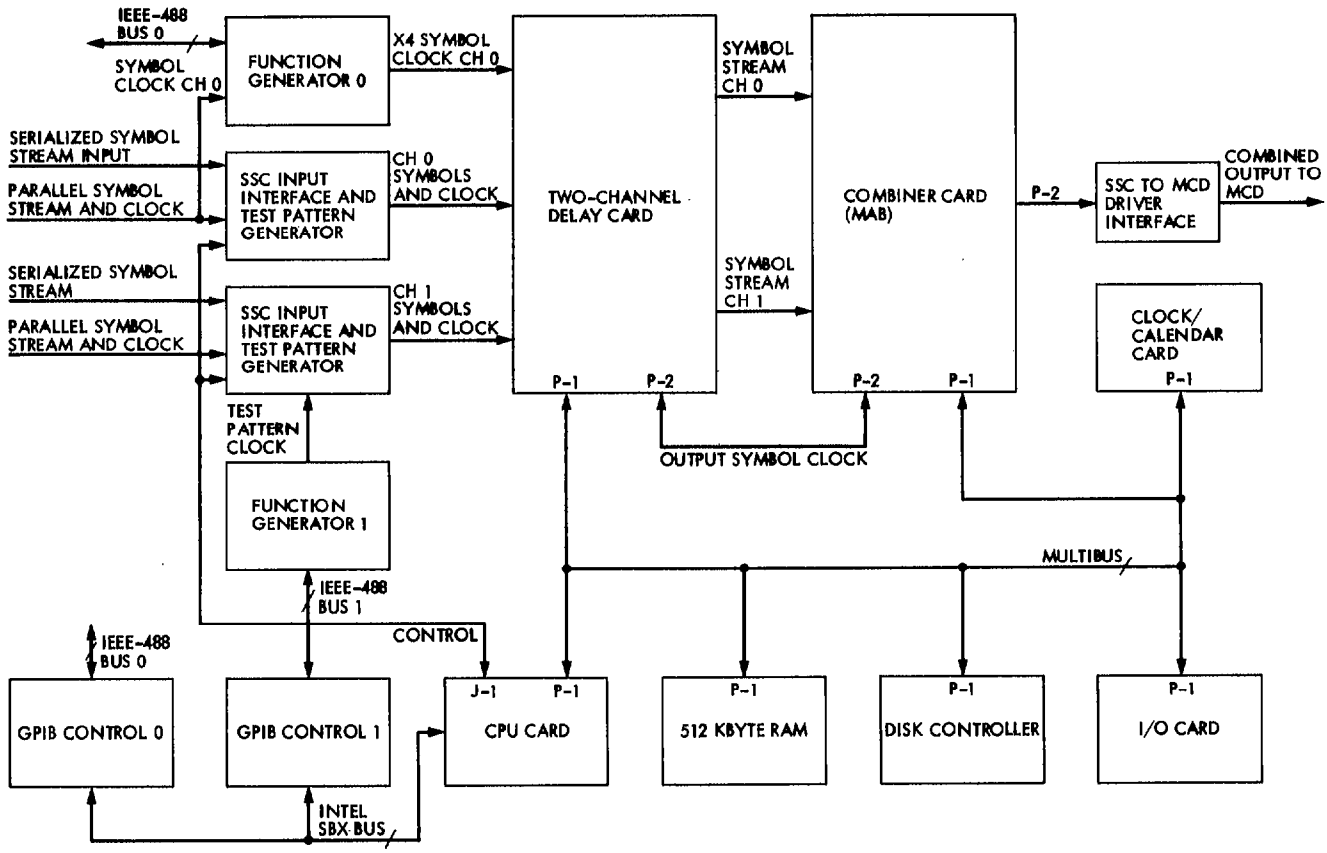

Fig. 2. Symbol-stream combiner block diagram for two-station configuration

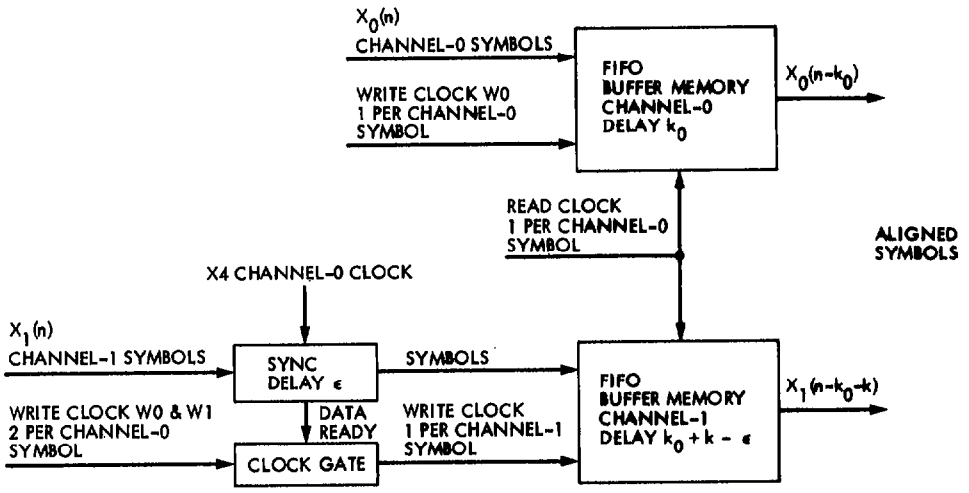

Fig. 3. Delay Card signal flow

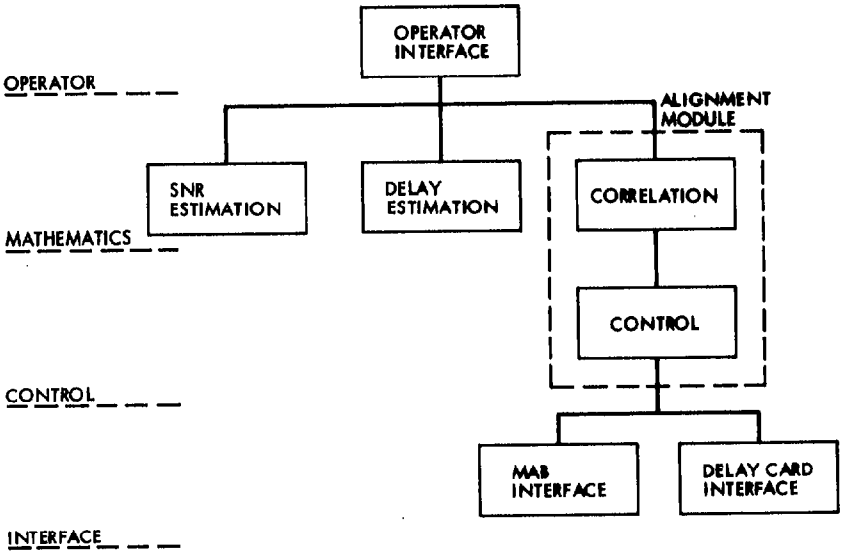

Fig. 4. Software organization