Programmable Digital Baud Integrators for the Radar High-Speed Data Acquisition System

K. H. Farazian and R. F. Jurgens
Communications Systems Research Section

As part of the planetary radar upgrade program to increase the resolution and speed of the radar system and in support of radio and radar astronomy, a new high-speed data acquisition system has been designed. Included in this article is a description of the programmable digital Baud Integrators used at the early stages of this system.

I. Introduction

With the advance of technology in LSI and VLSI, there exists a potential for the use of digital integrated systems in real-time processing areas that were previously implemented with analog circuitry. Digital circuits have become more attractive since they are less subject to distortion and interference than analog circuits, and can be easily regenerated so that noise does not accumulate in transmission. In addition, they have potential for extremely low error rates and high fidelity through error detection and correction, and they have greater reliability and can be mass produced. This article describes an all-digital technique for the Baud Integrators of the Radar High-Speed Data Acquisition System, a technique that avoids the inherent problems associated with analog systems such as the need for calibration and adjustment. The integration period of this system is selectable in 100-ns steps from 100 ns to 3276700 ns.

In the Radar High-Speed Data Acquisition System implemented to support the Deep Space Network program, the incoming IF signal is digitized immediately and all further processing is done digitally. Figure 1a shows the functional block diagram of the proposed radar system and Fig. 1b shows the front end of this system where the Baud Integrators are employed. The TRW TDC1025E1C analog-to-digital (A-D) converter boards produce 8-bit samples that are passed to the digital Baud Integrators, which are used as matched detectors for the range code elements. The Baud Integrators sum the samples for a preprogrammed number of samples without producing any overflow. The result is rounded to the most significant 8 bits. Of these 8 bits, four are used as extended bits for future use and four are sent out for further processing. The number of samples, N, and the scaling factor are the two inputs that must be supplied to the Baud Integrators. These are controlled by the VAX 11/780 host computer via a Unibus DR11C interface.

Figure 2 shows that the Baud Integrator can be broken into two parts. The first part is the Prebaud Integrator System, which represents a finite impulse response (FIR) filter operating at a fixed 50-MHz clock rate. The second part is the Postbaud Integrator System that is clocked with the 10-MHz drifted clock as are the following digital processors. Since the drifted clock is computed from the 50-MHz clock, its edges are stable at the 50-MHz clock rate.

II. Prebaud Integrator

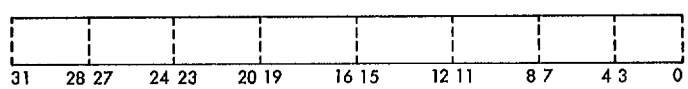
The function of the Prebaud Integrator is to add five successive samples and produce the correct result with no overflow every 20 ns to the Postbaud Integrator. The input to the Prebaud Integrator is the 8 bits of the TRW A-D converter clocked at 50 MHz. Refer to Fig. 3. The Prebaud Integrator, which has a FIR architecture associated with it, employs buffered adders that can operate up to a maximum of 50 MHz. The maximum clock frequency of this system is restricted only by the speed of the adders. In this system, the Fairchild Fast™ series 12-bit full adder with fast carry has been used. This procedure is faster than the 12-bit lookahead carry ALU, which is commonly used.

The 50-MHz input/output rate of the Prebaud Integrator not only significantly reduces the error introduced into the calculations by the shifting of the 10-MHz drifted clock of the Postbaud Integrator, but also eliminates the need for any "clear" or "reset" signal. That is, at most, only one sample will be deleted or used twice in the integration when the 20-ns corrections are made in the drifted clock. Also, being an iterative network, this configuration makes it easy to expand the number of bits or replace the adder modules with faster chips in the future.

The Prebaud Integrator can also be implemented using an Infinite Impulse Response (IIR) System as shown in Fig. 4. Here double-buffered accumulators are used to add five successive samples while the other branch is stable for unloading. Because of the high 50-MHz clock rate, the (A-D) converter output is split into two branches, each operating at a reduced rate of 25 MHz. Finally, the two branches are brought back together and added. Note that when one branch is adding three samples the other is adding two and vice versa. The output of this system will be at 10 MHz and must be resampled by the 10-MHz drifted clock of the Postbaud Integrator in a resampling circuit. The 10-MHz output and the resampling circuit of this IIR system increase the error introduced in the system significantly compared to the FIR system, making the IIR system less desirable. For example, the resampling involves deleting or using a 100-ns sum twice whenever the sample clock is corrected by 20 ns unless some more complicated scheme is employed. Refer to Fig. 5 for a graphic representation of this comparison. On the other hand, because each branch of the IIR system operates at the reduced rate of 25 MHz, this system is attractive for some applications where the chip count is important.

III. Postbaud Integrator

The Postbaud Integrator uses the double-buffered TRW TDC1043J3C[1] multiplier-accumulator chip, which adds N successive samples of the Prebaud Integrator in offset binary. Because of the reduced rate of the 10-MHz drifted clock, no branching is necessary. However, because of the large number of accumulations, the sum must be scaled so that the result is placed in the correct bit position for further processing. This is done by the multiplier portion of the TRW chip. Refer to Figs. 6 and 7 for block diagrams. The number of samples accumulated, N, is programmable along with the scaling factor associated with it by the VAX 11/780 host computer via a Unibus DR11C interface. N ranges from 2 to 2^{15} and is supplied in a two's-complement format via four binary counters. This reduces the number of chips required to input it in binary. The scale factor is written in binary and uses the equation, scale = $2^M/N$, where $M < 17$ depends on the number of inputs to the postbaud integrator. The following calculation assumes that the A-D converter is adjusted so that zero volt corresponds to an average value of 127.5 and that there are 11 output lines from the Pre- to the Postbaud Integrator. These 11 output lines will be the 11 most significant bits (MSBs) (out of 16 bits) X-input of the TRW chip, namely X5 to X15 where X0 to X7 are not used and therefore are pulled down. The scaling factor will be the 16-bit Y-input lines of the multiplier-accumulator. Depending on how many samples are added, the scaling factor is so chosen as to place the result in the MSB of the output of the TRW chip. These bits are selected to be P23 to P30 with P23 to P26 as the optional extended bits. Due to the accumulation in the Prebaud Integrator, samples of the (A-D) converter with the average of 127.5 now have the new average value of 5 × 127.5. With the correct scaling factor, N samples are accumulated and placed at the 8 MSBs of the 32 output bits of the multiplier-accumulator chip. This means that the fractional part starts at bit number 23.



BIT LOCATIONS

Expressing 127.5 in the hexadecimal format and having 32 bits where the decimal point is just before bit 23, one can write

$$7F.7FFFFF < 127.5 = 7F.800000$$

$$= 7 \times 2^{28} + 15 \times 2^{24} + 8 \times 2^{20}$$

$$= 2.139 \times 10^9$$

[1] *TRW TDC1043 VLSI Multiplier-Accumulator Preliminary Information*. TRW Inc., La Jolla, Calif., 1983.

Then, to calculate the scaling factor, use the following equation:

$$N \times 2^5 \times 5 \times 127.5 \times \text{scale} = 2.139 \times 10^9$$

or

$$\text{scale} = 104852.9/N < 2^{17}/N = 131072/N$$

There is a factor of 2^5 because X5 to X15 are the only actual inputs from the Prebaud Integrator.

Therefore select

$$\text{scale} = 2^{15}/N$$

extracting the output at bit locations P23 to P30. For example, if $N = 2$ (minimum value of N, adding only two samples) then scale = 2^{14}, which implies that the input is shifted by 14 bit locations. With the input being X5 to X15, the result will appear at output bit locations P19 to P29. When two of these are added, the 8 MSBs of the 9-bit addition result are placed at output bits P23 to P30. Note that M could have been chosen to be 16. In this case, the 8 Most Significant Products (MSPs) of the TRW chip, namely P24 to P31, would have been the correct output to use for further processing of the result.

The maximum clock frequency of Postbaud Integrator is limited by the TRW chip, which can run up to a maximum of 11 MHz, as was verified in the laboratory.

The Baud Integrator can also be designed to operate in two's complement, which has some advantages and disadvantages relative to offset-binary. These are fully discussed in the next section. In the remainder of this section, however, two's-complement hardware implementation is compared to that of the offset-binary already discussed. The adders in the Prebaud Integrator stage and the TRW chip in the Postbaud Integrator stage both have the capability of operating in two's complement. However, to avoid overflow, the resolution of the system decreases. To increase the resolution to the same 8 bits as in the offset binary, more chips are required. The two's-complement operation of the system is achieved by extending the 8 output bits (0 to 7) of the Prebaud Integrator, with bit 7 being the sign bit, to 16 bits at the Postbaud Integrator input. This 16-bit input (0 to 15), with its bit 15 carrying the sign bit, is in turn extended to 35 bits internally by the TRW chip where the sign bit now is bit 34. Notice that with the TRW chip, three-state output drivers are provided for one 16-bit word, the MSP, and one 3-bit word, the extended product (XTP). The least-significant product is not available with the TDC1043J3C, but is held internally for use in accumulation. This would mean that in the addition of small numbers, barely any information, if any, regarding the result of the addition will show up at the external output. To overcome this problem, one can implement the process just described by the IIR system discussed in the previous section where the scaling of the samples and number of samples added must be programmable. This would require a more complex system with an increased chip count.

IV. Two's-Complement Operation Analysis

This section deals with the analysis of the Baud Integrator operation in two's complement. As is shown in the following, this scheme requires less memory space, which reduces the number of registers used in the system. On the other hand, it introduces some problems that make this system less desirable.

Assume that the incoming signals, n_i, to the Baud Integrator are independant random variables with the following characteristics:

$$E\{n_i\} = 0 \text{ (zero-volt average)}$$

and

$$E\{n_i^2\} = \sigma_n^2$$

where E is the expected value operator. Then the output of the Baud Integrator, which is the sum of these samples, will have the following characteristics:

with

$$S = \sum_{i=1}^{N} n_i$$

$$E\{S\} = 0$$

and

$$E\{S^2\} = N\sigma_n^2 = \sigma_S^2$$

or

$$\sigma_S = \sqrt{N}\,\sigma_n$$

This implies that the output register grows as $\sqrt{N}$ in the two's complement compared to N in the offset-binary. So a noticeable savings in memory space can be achieved for a large number of additions.

In spite of this fact, there are other factors that make this system less desirable. For one, the sign bit extension must be implemented; and for another, the final result must be scaled properly for further processing of the signal. These were fully discussed at the end of Section III. In addition, either system must be able to operate with test signals that do not have the statistical properties alluded to in the above discussion. This makes the two's-complement operation equally or more complex than the offset binary.

V. Computer Interface

The main interface to the VAX 11/780 computer for the Radar Baud Integrators is a Unibus DR11C (Ref. 1). The DR11C requires three address locations for operation on the Unibus. Address XXXO is DRCSR (DR11C Control and Status Register). The second address location can be used as a read/write port and is being used for write only. The third address location is for read only and is being used for the purpose of reading back the Baud-Integrator internal registers.

Figures 8 and 9 show the formats and functions of the baud internal control and status register (ICSR) and functional hold registers. The DR11C CSR bits CSR1 and CSRO are used to control the mode of operation in read/write to DR11C addresses. With both CSR1 and CSRO equal to zero, addresses 2 and 3 write or read from the ICSR in the Baud Integrator. With CSR1 = 0 and CSRO = 1, addresses 2 and 3 write and read from the registers pointed to by the ICSR. The register pointer within the ICSR can be set to auto increment on read or write.

Figure 9 shows the two internal registers for controlling the Postbaud Integrator, setting N and the scaling factor.

VI. Summary and Conclusion

The Baud Integrator employs an all-digital system technology instead of the customary analog technology. It operates with two coherent input clocks running at 10 MHz and 50 MHz. The Prebaud Integrator sums five successive samples and the Postbaud Integrator accumulates up to 2^{15} samples of the Prebaud Integrator. Both N and the scaling factor are programmable via a Unibus DR11C interface from the VAX 11/780 host computer.

Acknowledgments

The authors wish to thank Stan Brokl for original interface design.

References

1. S. S. Brokl, "Polynomial Driven Time Base and PN Generator, *The Telecommunications and Data Acquisition Progress Report 42-75*, pp. 84-90, July-September 1983. Jet Propulsion Laboratory, Pasadena, Calif., November 15, 1983.

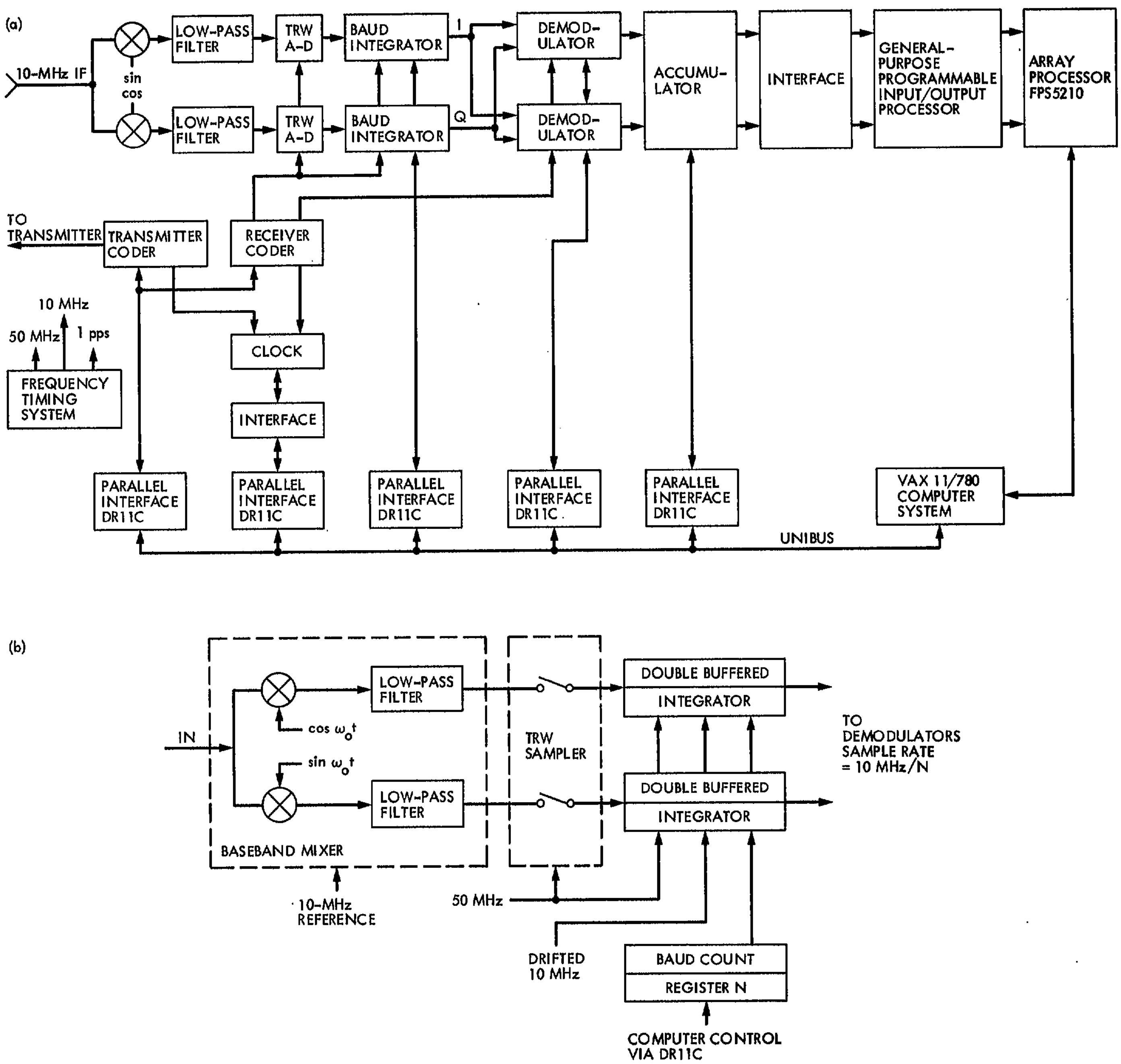


Fig. 1. High-resolution radar system: (a) functional block diagram; (b) front-end digital processing system

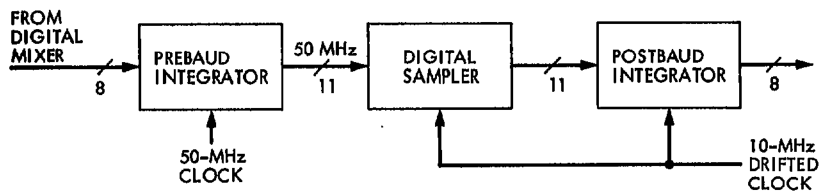


Fig. 2. Separation of the baud integrator into pre- and postbaud integrator with resampling in the center

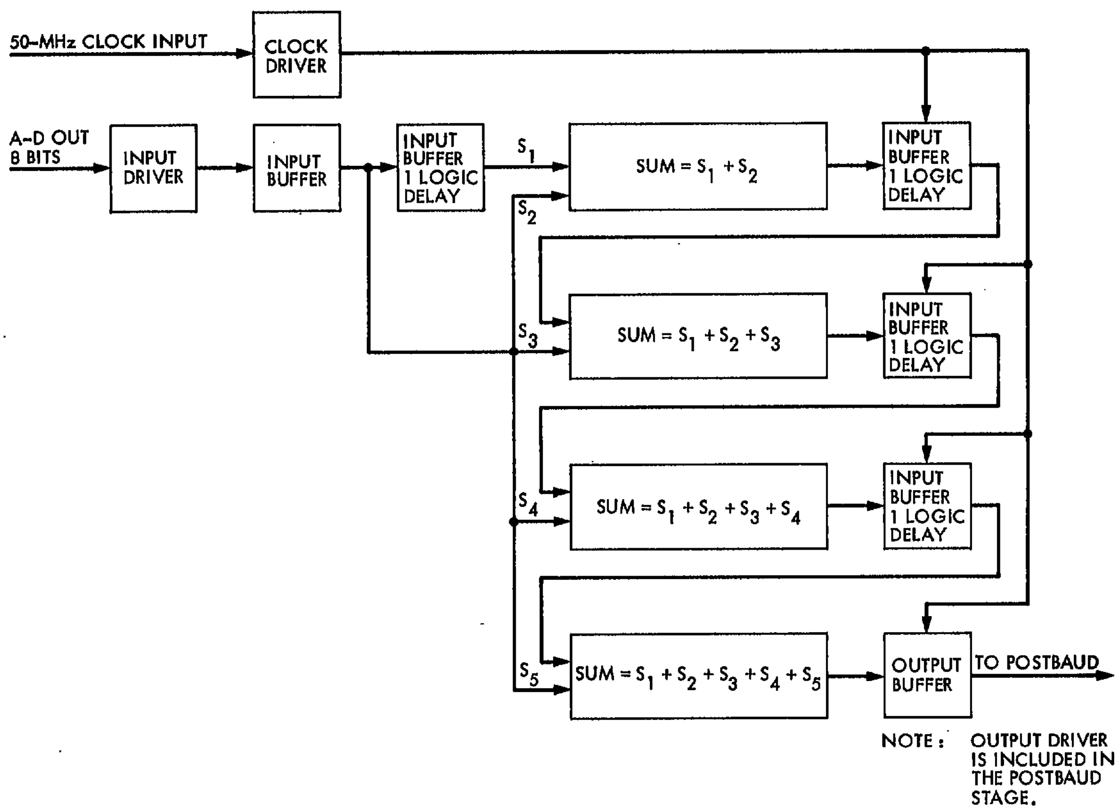
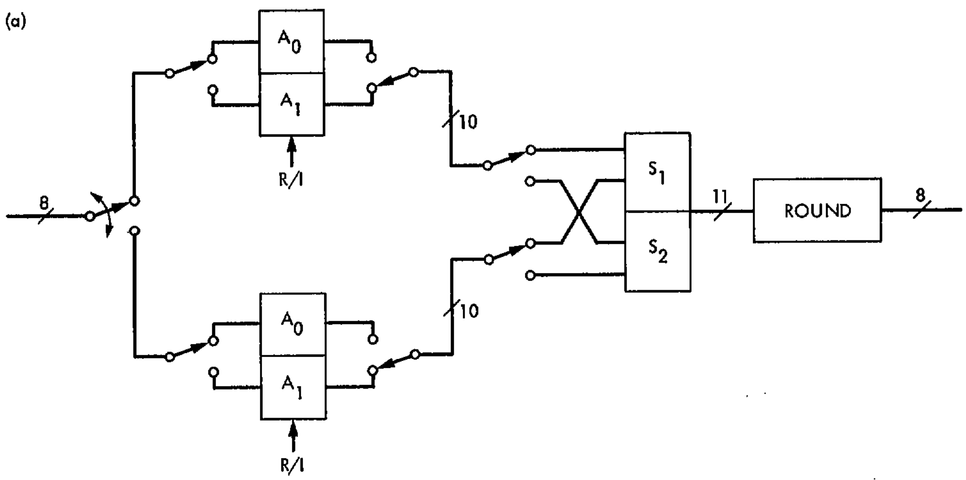


Fig. 3. Prebaud integrator design block diagram



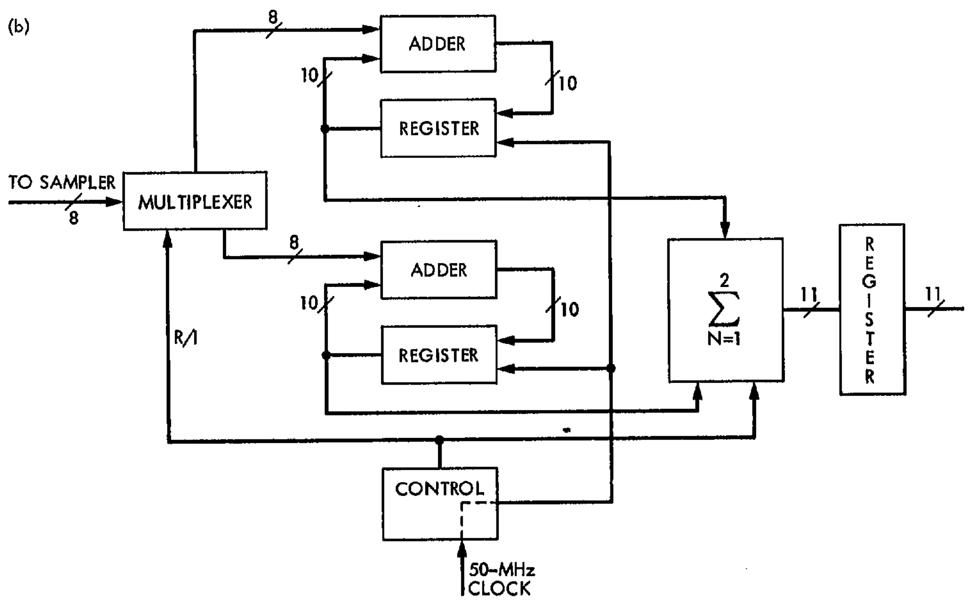


Fig. 4. Prebaud integrator with all clocks derived from the stationary 50 MHz: (a) using IIR system (integrate and dump); (b) double-buffered block diagram of (a)

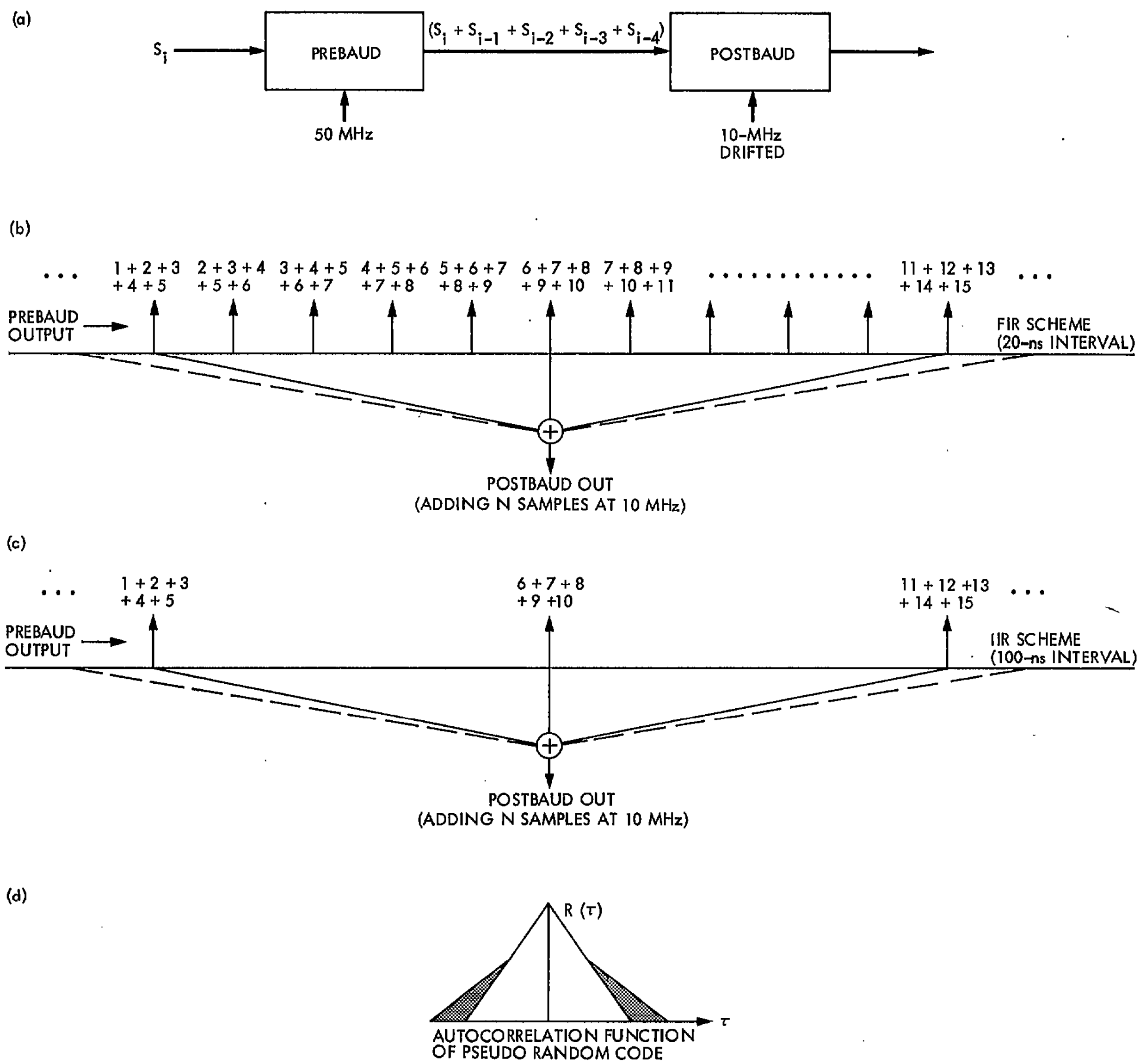


Fig. 5. Comparison of the FIR and IIR structures for the prebaud integrator design: (a) system block diagram; (b) FIR structure with an output rate of 50 MHz; (c) IIR structure with an output rate of 10 MHz; (d) autocorrelation function of pseudorandom code where the shaded area represents the error introduced with the shifting of the 10-MHz drifted clock. This error is reduced significantly in the FIR scheme.

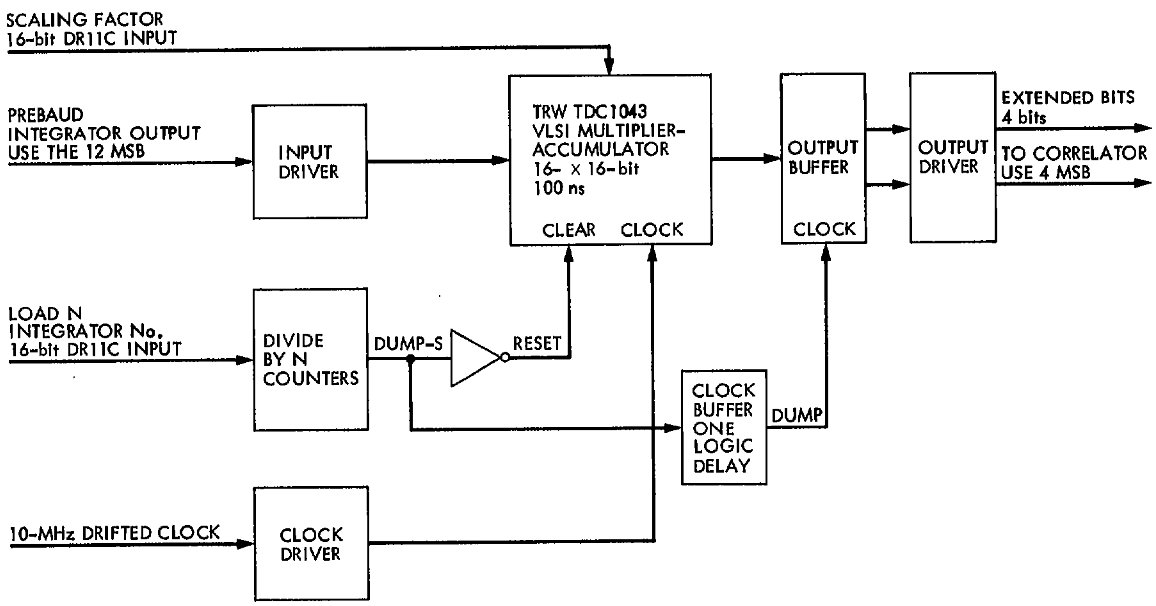


Fig. 6. Postbaud integrator design

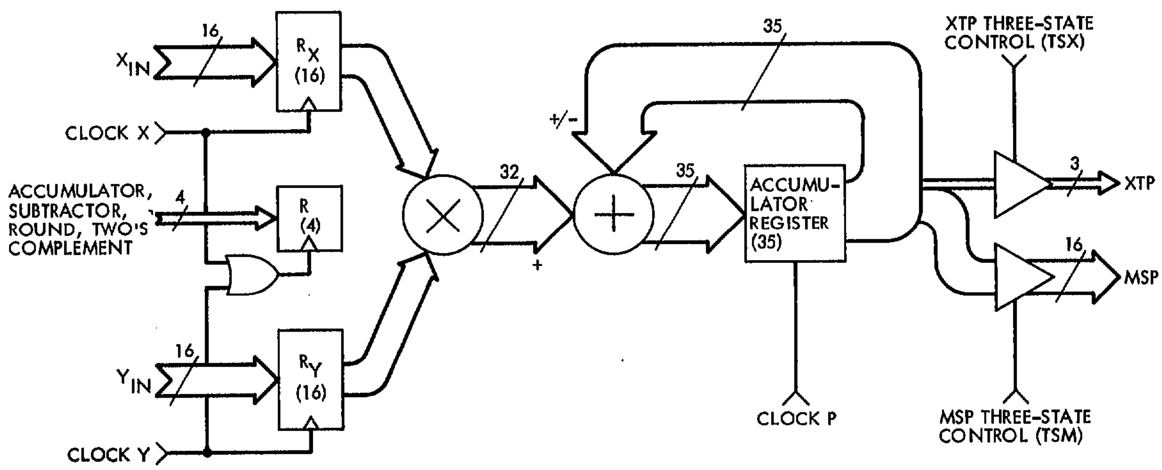
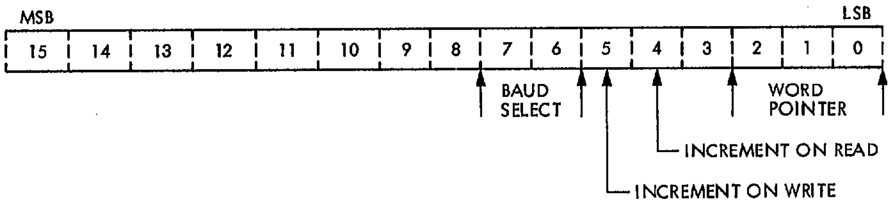


Fig. 7. Functional block diagram of the 10-MHz TRW TDC 1043J3C, 16- × 16-bit, VLSI multiplier-accumulator



WORD POINTER

000 = SCALE
001 = LOADN
010 =   F
011 = F U U
100 = O T S
101 = R U E
110 =   R
111 =   E

BAUD INTEGRATOR SELECT

00 = B.I. 1
01 = B.I. 2
10 = B.I. 3
11 = B.I. 4

DR11C MODE CONTROL BITS

CSR1	CSR0	
0	0	= R/W ICSR
0	0	= R/W FUNCTION REGISTERS POINTED TO IN THE SELECT AND WORD POINTER
1	0	= FOR FUTURE USE
1	1	= FOR FUTURE USE

Fig. 8. Baud ICSR

ICSR

WORD POINTER	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
000	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
001	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Fig. 9. Function register formats