Controller and Interface Module for the High-Speed Data Acquisition System Correlator/Accumulator

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One complex channel of the High-Speed Data Acquisition System (a subsystem used in the Goldstone solar system radar), consisting of two correlator modules and one accumulator module, is operated by the controller and interface module. Interfaces are provided to the VAX UNIBUS for computer control, monitor, and test of the controller and correlator/accumulator. The correlator and accumulator modules controlled by this module are the key digital signal processing elements of the Goldstone High-Speed Data Acquisition System. This fully programmable unit provides for a wide variety of correlation and filtering functions operating on a three megaword/second data flow. Data flow is to the VAX by way of the I/O port of a FPS 5210 array processor.

I. Introduction

A new digital signal processing and data acquisition system is installed in the pedestal room at DSS-14 at Goldstone in support of radio astronomy and solar system radar experiments. Figure 1 is an overall block diagram for this system. This article is about the correlator assembly; the complete system is described in *TDA Progress Report 42-77* (Ref. 1).

The Controller and Interface board (CI) ties together four major components of the High Speed Data Acquisition System (HSDAS): the VAX 11/780 computer (by way of the UNIBUS), the correlators, the accumulators, and the array processor (Ref. 1). Additionally, the controller provides the timing and distribution of clock and control signals to the two correlators and one accumulator board, and provides the interface path to the array processor. Together the four modules comprise two data channels (or one complex data channel) which make up one Complex System Unit (CSU). Control paths are provided from the VAX 11/780 computer to the correlators and accumulators (Ref. 2), and data paths into the Floating-Point System array processor (FPS 5210) (by way of the General Purpose Programmable I/O Processor [GPIOP]) are also provided. Each correlator can be programmed to compute as many as 256 lags of four-bit cross-correlation and autocorrelation data using a single-bit reference function and single-bit mask function. Also, each correlator is usable as a digital finite impulse response (FIR) filter. The CI is contained on one standard universal wire wrapping board type 8136-UG6 manufactured by Augat Inc. and holds the 150 integrated circuits (Fig. 8) used.

Figure 2 is a block diagram showing the control and data paths to and from the CI, and therein we see its relation to the correlators and accumulators in the system. The major control path is from the VAX 11/780 by way of a DR11C I/O port. Through this port, one configures and runs the

correlators and accumulators in the desired modes. A discussion of the operating modes is in Section II below. An additional port from the GPIOP is used to monitor the status of the accumulator memories. Through this port GPIOP software commands the accumulator memory contents to be transferred using direct memory access (DMA) to the array processor memory. Each accumulator is double buffered and has a FULL flag and an OVERFLOW flag. The FULL flag is monitored by the GPIOP and indicates when data is ready to be unloaded from the accumulator. The OVERFLOW flag indicates that the accumulator memory was not unloaded in time and has been at least partially overwritten with new data. The operation of the DMA and flags is explained in Section IV, below.

II. Computer Control Paths

The major function of the CI is to distribute data and system clock signals to the correlators and accumulators and to control their operation independently of the computer (see Fig. 3, a block diagram for the CI). A 256 × 12 bit memory is included for downloading of test data and filter and mask functions into the correlators from the VAX. Control functions are downloaded from the VAX by way of a DR11C I/O port (a UNIBUS compatible interface used with several devices in the radar system, Ref. 3). The Polynomial Driven Time Base and PN Generator (Ref. 3) provide the time base and coding signals for the CI. Figures 4 and 5 illustrate the Control and Status Register (CSR) and the internal function registers accessible through the DR11C port to the CI. Note that one complex channel is serviced by one controller (see Figs. 9 and 10). Figure 3 illustrates the lag counters and registers and the accumulation counters and registers.

The Correlator/Accumulator (Cor/Acc) control and status register (CSR) (Fig. 4) is a broadcast register which is used to communicate individually with all function registers in the selected Cor/Acc, and is therefore received and decoded on all CI boards. Bits 6 through 8 determine which CI board is selected. The word pointer bits 0 through 2 determine which function register is selected. Bits 4 and 5 set the automatic increment of the word pointer and are used for multiple reads or writes from the computer. The CLEAR bit (position 10) is broadcast to all CI boards and is used to initialize all internal control functions and flags to a known inactive state throughout the system. MASTER RUN (bit 15) is broadcast to all CI boards throughout the system and starts the Cor/Acc operation at a known 1 second epoch.

The 256 × 12 CI memory is used to hold correlator test data and filter and mask coefficients. Although only 12 bits are used, it is organized as if it were two bytes using only 6 bits each and numbered as if all 16 bits were present. Bits 0 through 3 of the first byte contain data for correlator A, bit 4 is the mask, and bit 5 is the code for correlator A. Bits 8 through 11 of the second byte contain data for correlator B, with bit 12 as the mask and bit 13 as the code. The memory has two address generators. Each is multiplexed and split so that each byte can be independently downloaded into the correlator. The addresses are organized so that address 00 corresponds to the last data downloaded into the correlator. The address generators are strobed by the system clock during downloading. The computer reads and writes both bytes and is not split in addressing. It uses the function register 0 (Fig. 5) as a pointer to the buffer memory location to be written. Function register 1 is a window into the buffer memory. The computer address generator location may be incremented automatically while writing to the window permitting a block data transfer from the computer. The mask bits allow programming any length of correlation function up to 256 lags. The reference bits allow any single bit function up to 256 lags to be loaded into the correlator. By using the mask and reference bits the correlator can run also as a binary FIR filter.

The function register 2 controls mode and data downloading for correlator A from the buffer memory. Function register 3 controls correlator B in the same way as A. Each correlator can run in three separate modes and can accept data from two separate sources selected by bit 15. In the LONG CODE AUTO mode (bit 14 on), the correlator runs continuously, updating the reference input modulo 256. In the SHORT CODE mode the correlator runs continuously modulo the number set as maximum in function register 4. In both modes the data and reference are continuously streaming. In the SHORT CODE mode the mask (bit 13) must be loaded for the selected length set in register 4. In the FIR FILTER mode the reference and mask are downloaded from the buffer prior to running, and bits 14 and 13 are not set. In this mode the reference is not updated and the correlators run as an FIR filter. The ZERO BUFFER ADDRESS bit 12 is used prior to downloading reference data or masks into the correlator from the buffer memory. The AUTO LOAD FROM CODER bit (3) is used for testing and for streaming data into the correlator reference directly from the coder between word detects. Each of the bits 0 through 2 allows for selectively downloading segments of the buffer memory into the correlator without altering the contents of an unselected segment. Function register 4 defines the maximum lag that will be used by the correlator/accumulator pairs. The first byte controls accumulator A and correlator A. Similarly, the second byte controls accumulator B and correlator B. In the LONG CODE AUTO mode both bytes would be loaded with FF Hex (i.e., all 256 lags are used).

Function registers 5 and 6 specify the number (N) of coherent sums computed for each lag in accumulator A and B

respectively. Function register 7 enables and clears the accumulator's internal address generators and must be set properly prior to running.

III. Data Paths

Figure 2 best illustrates the data path connections into and out of the CI. The input multiplexer allows for choosing one of two inputs to each correlator. The input word consists of four bits of data, one bit for reference, and one bit for external loading of the mask. The number system is offset binary (Ref. 2), and the size of each word out of each correlator lag is 12 bits. This means that the accumulator can add up to 65,536 samples of 12-bit wide data, giving a maximum result 28 bits wide. The GPIOP accepts up to 38 bits in word width. Each correlator yields a 256 lag by 6-bit output (4 data bits, one reference bit, and one mask bit) which can be easily passed to other CSU modules to extend the number of lags.

IV. GPIOP Array Processor Interface

This CI module provides high-speed DMA transfer of data from the accumulator memories to the FPS 5210 Array Processor via the GPIOP I/O channel. The burst transfer rate is 3.0 million samples/sec with no reformatting of data to floating point in the GPIOP. With reformatting, the burst transfer rate is 1.5 million samples/sec. The burst length is dependent upon the size of the array processor memory (now 256K words deep).

Figure 6 illustrates the GPIOP Command and Device Control words and Data Format words. Bits 17 through 19 select which CI module is accessed and bit 16 selects accumulator A or B for DMA read. Bits 13 through 15 are command bits that define the following functions:

NULL	No request
REPORT	Tests response of device status; Ready = 1 or Overflow = 1
SEND	Sets selected device for DMA transfers
CLEAR	Clears Ready and Overflow bits to false
INIT	Zeros address register in the Accumulator

It is important to note that the NULL command must precede each of the other commands to prevent spurious transient "commands" in the CI interface.

V. Summary

The CI modules control individual CI units, providing the node which ties the VAX, in its controlling and monitoring tasks, to the remainder of the high-speed data acquisition system. These modules provide for distribution of A/D converter input, accumulation control (by way of the GPIOP), system clock distribution, and system control. The complete HSDAS will consist of 8 CSU modules configured with a multiplexer as shown in Fig. 7. Three channels have been completed and tested. They were used during the April/May Venus inferior conjunction radar experiment at Goldstone. That series of measurements confirmed that system operation is correct. Completion of the remaining 5 CSU modules is in progress.

References

1. Deutsch, L. J., Jurgens, R. F., Brokl, S. S., "Goldstone R/D High Speed Data Acquisition System." *The Telecommunications and Data Acquisition Progress Report 42-77*, Jet Propulsion Laboratory, Pasadena, Calif., Jan.-Mar. 1984, pp. 87-96.
2. Brokl, S. S., "Demodulator and Accumulator for the High Speed Data Acquisition System." *The Telecommunications and Data Acquisition Progress Report 42-77*, Jet Propulsion Laboratory, Pasadena, Calif., Jan.-Mar. 1984, pp. 97-103.
3. Brokl, S. S., "Polynomial Driven Time Base and PN Generator," *The Telecommunications and Data Acquisition Progress Report 42-75*, Jet Propulsion Laboratory, Pasadena, Calif., July-Sept. 1983, pp. 84-90.

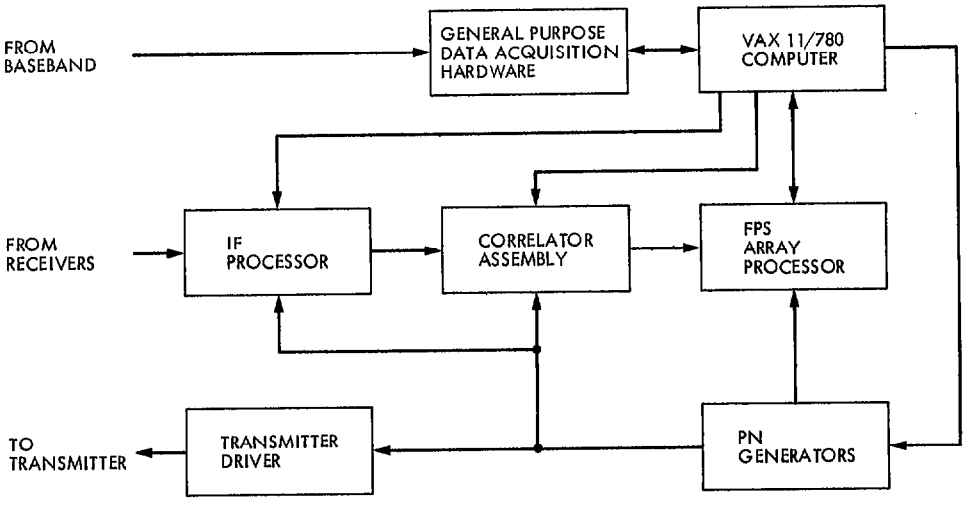


Fig. 1. High Speed Data Acquisition System overall block diagram

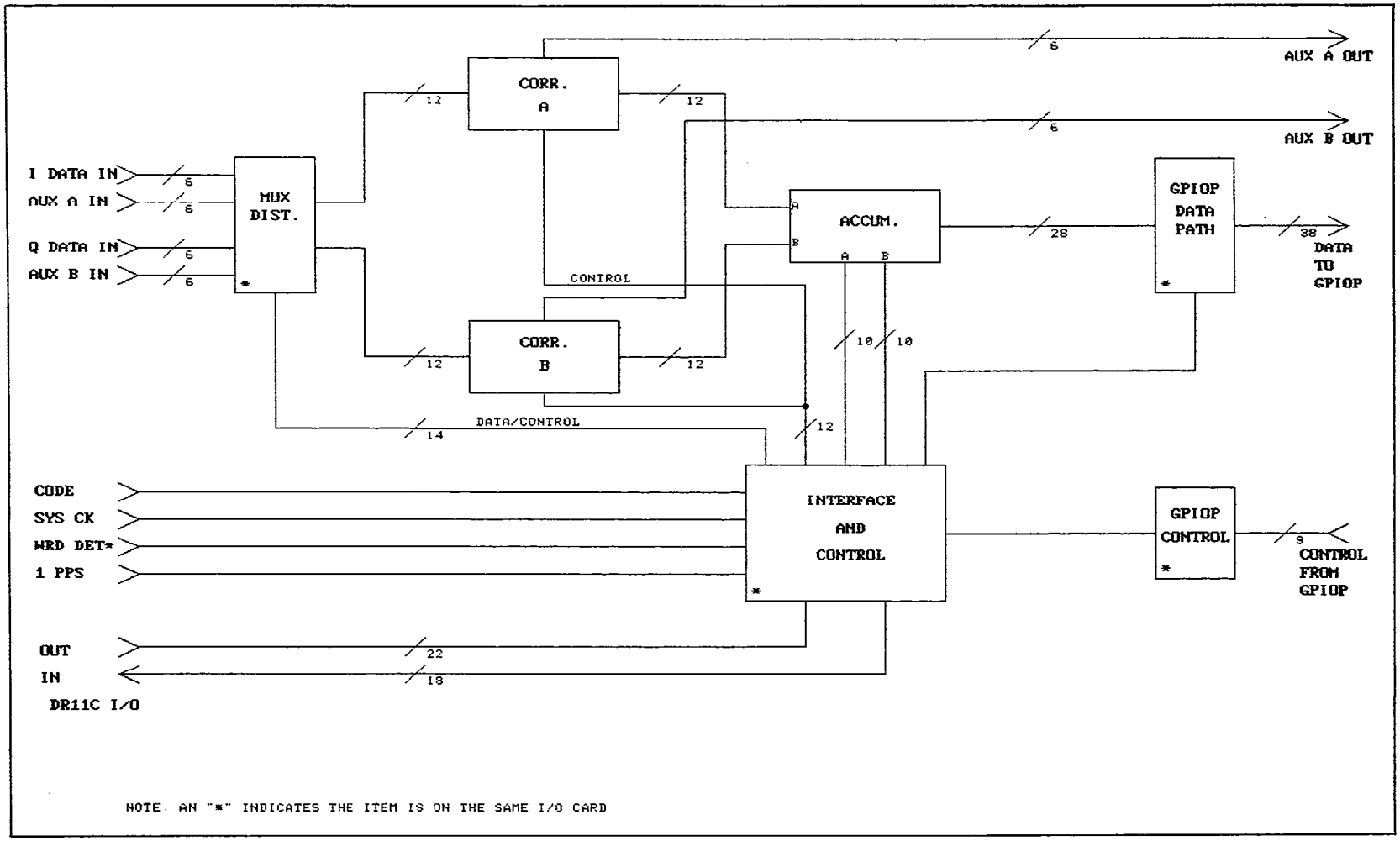


Fig. 2. Correlator/Accumulator block diagram

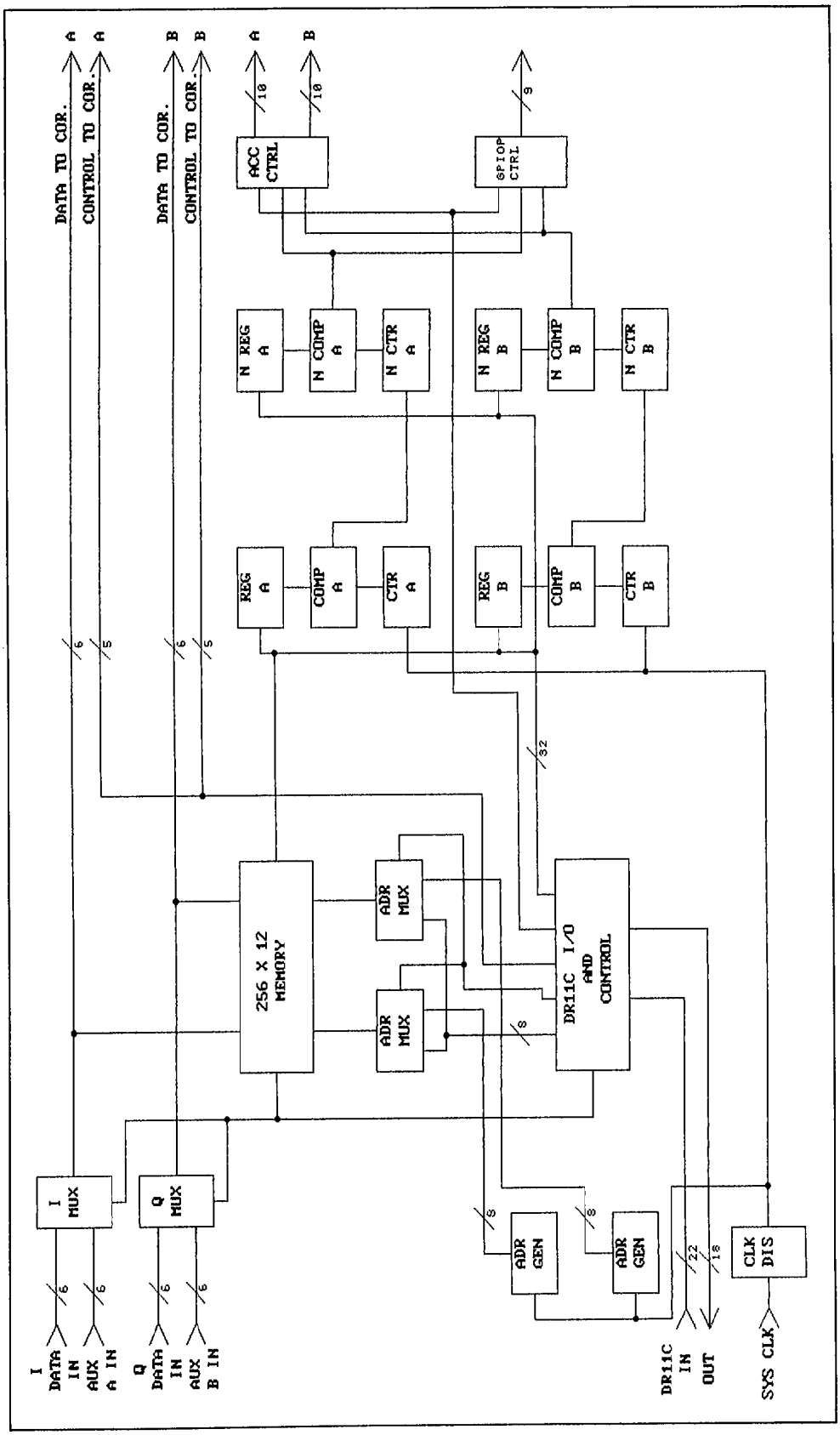
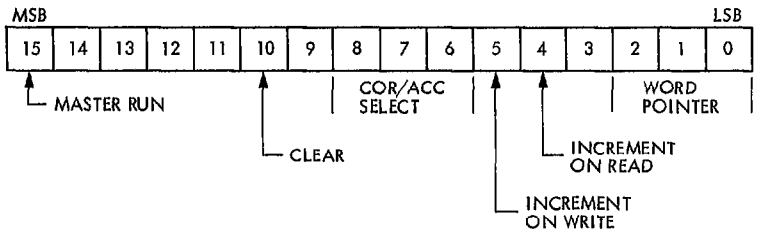


Fig. 3. Controller and Interface block diagram



COR/ACC SELECT	WORD POINTER
000 = COR/ACC 1	000 = COR BUFFER ICSR
001 = COR/ACC 2	001 = COR BUFFER WORD
010 = COR/ACC 3	010 = COR A ICSR
011 = COR/ACC 4	011 = COR B ICSR
100 = COR/ACC 5	100 = SET MAX ADR. A & B
101 = COR/ACC 6	101 = SET N FOR A
110 = COR/ACC 7	110 = SET N FOR B
111 = COR/ACC 8	111 = ICSR FOR A & B

NOTE:
DR11C MODE CONTROL BITS

CSR1	CSR0	
0	0	= READ/WRITE ACCUM CSR
0	1	= READ/WRITE FUNCTION REGISTERS POINTED TO IN THE ACCUM. SELECT AND WORD POINTER.
1	0	= RESERVED FOR FUTURE USE
1	1	= RESERVED FOR FUTURE USE

Fig. 4. Correlator/Accumulator control and status register format

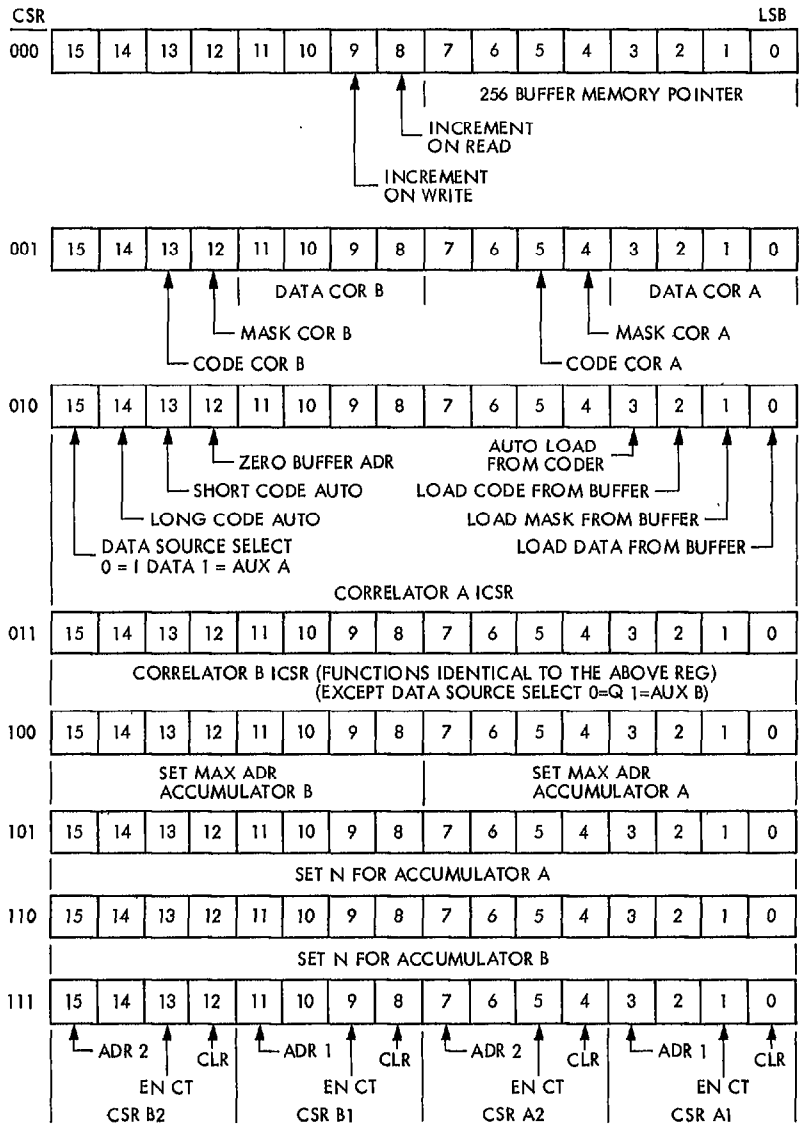


Fig. 5. Correlator/Accumulator function register formats

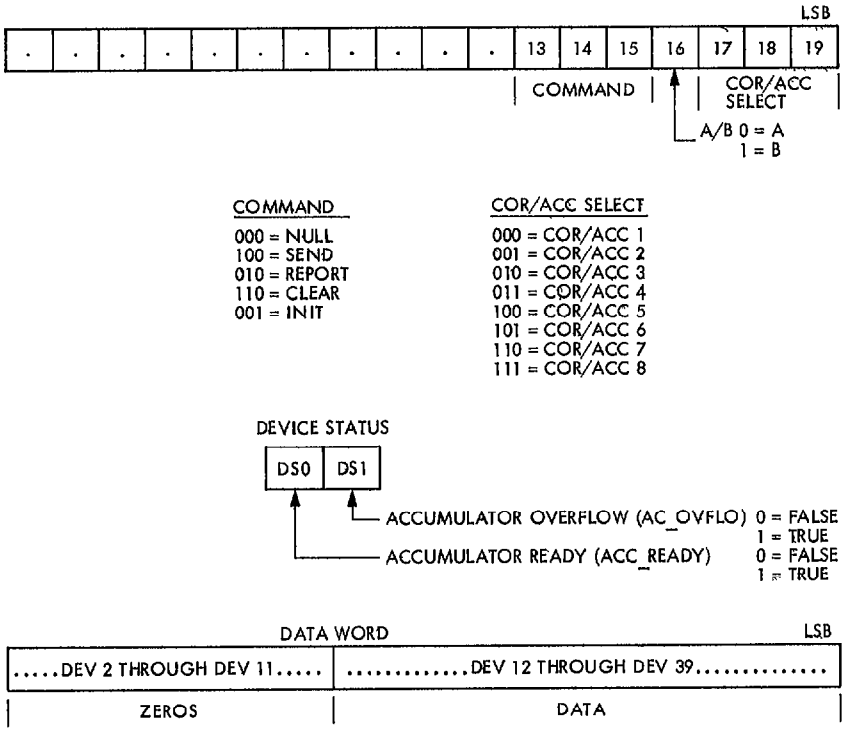


Fig. 6. GPIOP command and device word formats

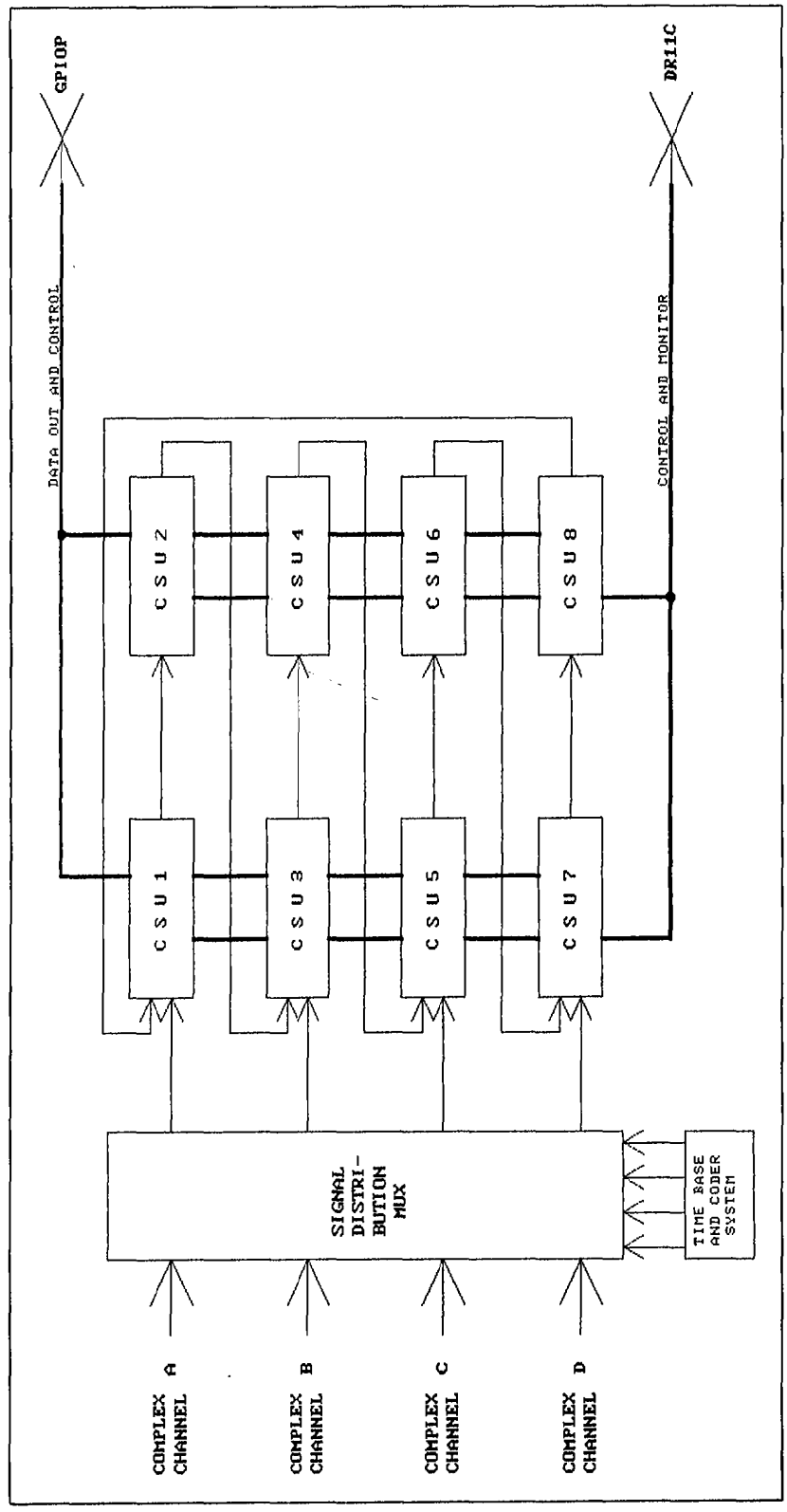


Fig. 7. Signal distribution diagram

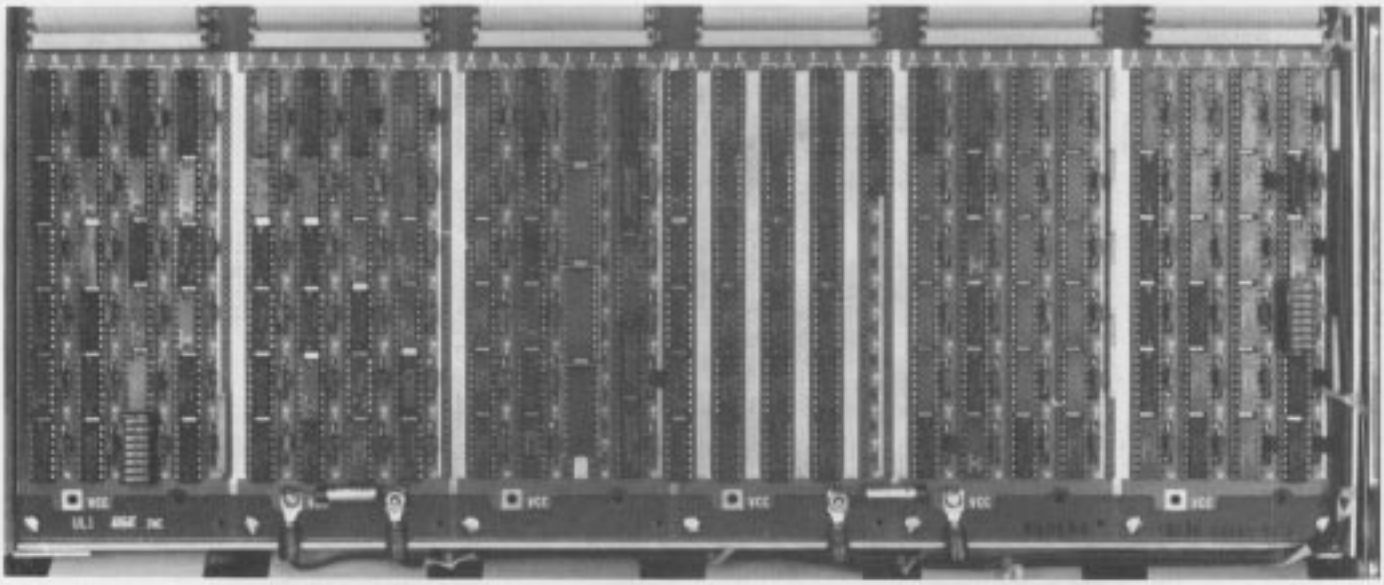


Fig. 8. Controller and Interface board

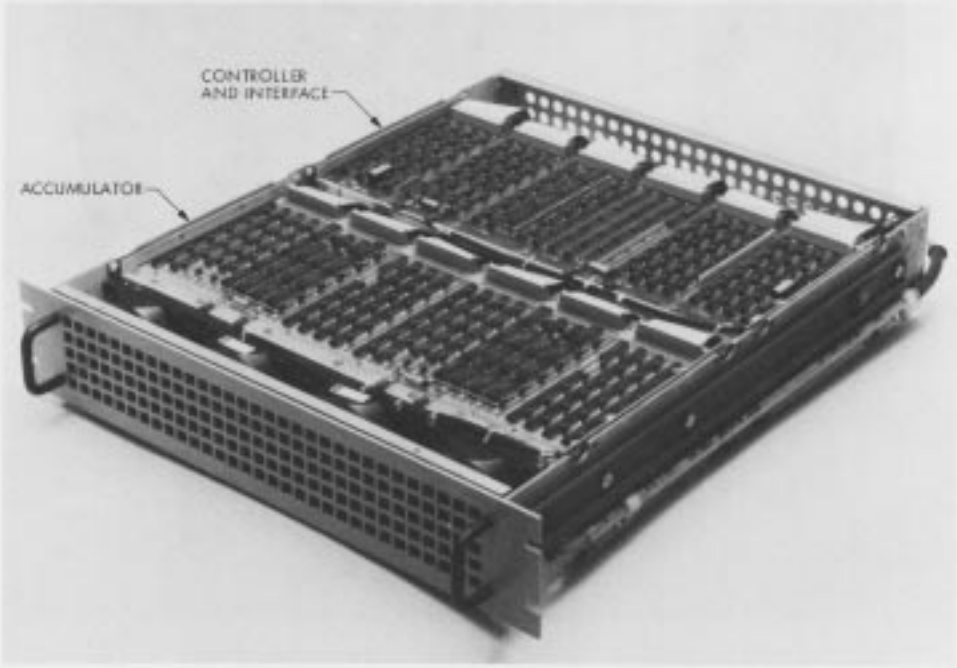


Fig. 9. Correlator/Accumulator System Module, top view

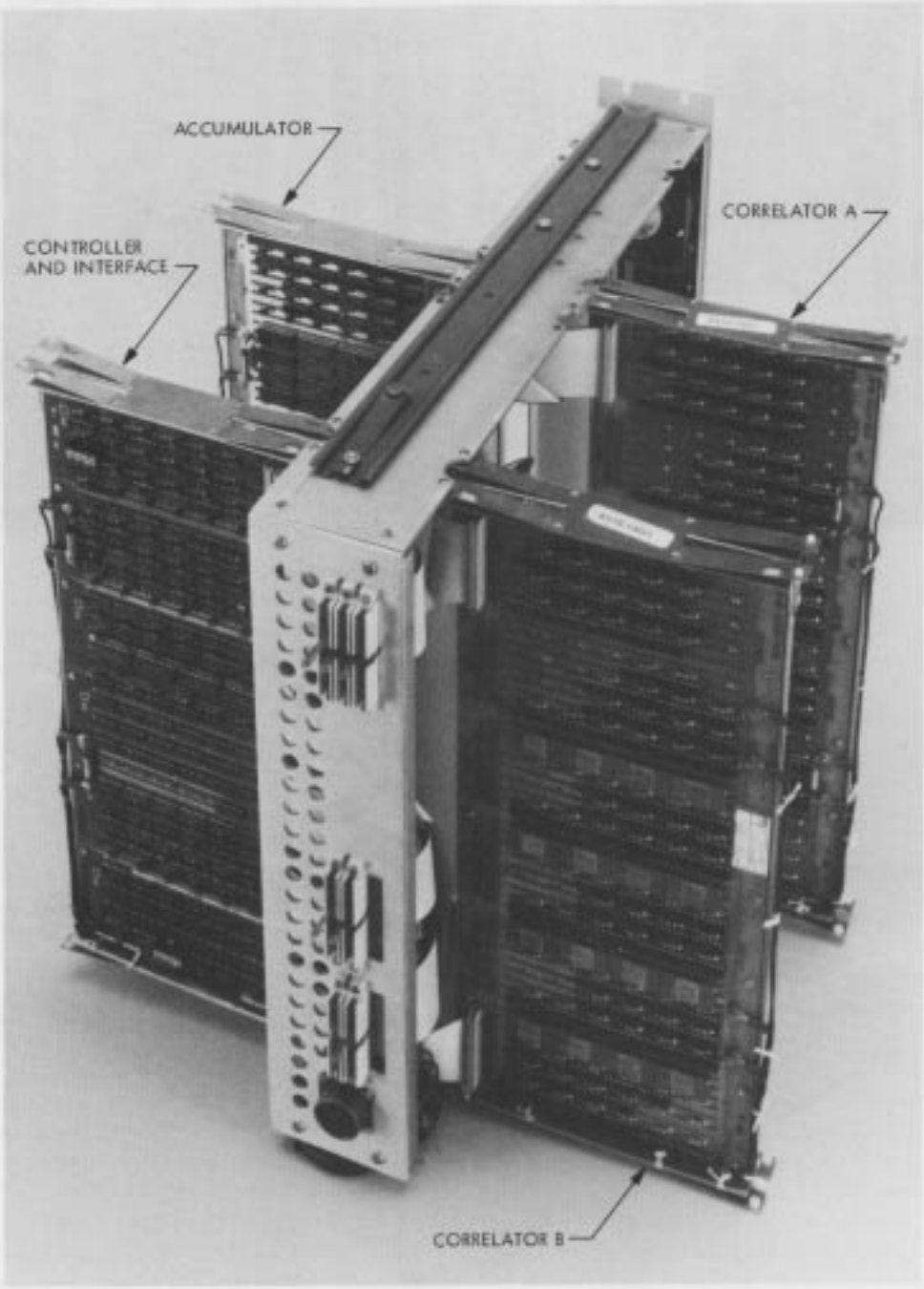


Fig. 10. Correlator/Accumulator System Module, open view