A General Monitor and Control Interface to the VAX UNIBUS by Way of the DR11-C I/O Port

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The High Speed Data Acquisition System for the Goldstone Solar System Radar requires a number of interfaces for monitor and control functions for the special purpose data acquisition hardware. One common interface design is used. A large number of external control and monitor registers may be addressed and observed with this interface design, by using only three address locations on the UNIBUS and a standard DEC supplied input/output port. A broadcast control and status register is introduced which addresses any number of different units and registers.

I. Introduction

Digital Equipment Corp. supplies several types of interface ports (DR11-C, DR11-WC, and others); each one is designed for a limited number of address entries onto the UNIBUS. The UNIBUS is a single common path that connects the processor and all peripherals. The bus contains 56 lines for address, data and control information. In order to access a large number of peripheral device registers, a special interface is required for each different application. Presented here is a simple computer controlled general I/O structure designed for monitor and control functions using a DR11-C I/O port (Ref. 1) with an external Broadcast Control and Status Register (BCSR) and multiple function registers. It is designed to be used with the DR11-C but the idea lends itself well to any addressed bus with limited I/O capability. The DR11-C uses three address locations on the UNIBUS; one for communication with the I/O port internal registers, one for transferring data to an external register, and one for receiving data from an external register. By assigning different values to itself, the internal register may be used as a pointer to the external registers and allows broadcasting an external BCSR for further coding and communications to external function registers. A type of indirect addressing is generated so that, with only three address locations used on the UNIBUS, any number of external registers may be addressed, read, or written.

II. Limitations with the DR11-C Interface

Figure 1 shows the register assignments for the DR11-C interface. The DRCSR register has only two control bits (CSR0, CSR1) for conditioning what the DROUTBUF and DRINBUF registers read from or write to an external device. A typical interface could therefore read or write only four external registers. This is far too few for many monitor and control functions for the High Speed Data Acquisition System and most other general applications. The DR11-WC has a direct-memory-access controller which allows a large number of external memory locations to be read or written but costs about six times more than the DR11-C. Also, the DR11-WC has more functions than are required for monitor and control applications. Since the monitor and control applications for the Goldstone Solar System Radar do not require high data throughput, the following solution using the DR11-C I/O port and external controller was adopted.

III. The General Monitor and Control Interface, a Solution to This Problem

Using the CSR0 and CSR1 bits in the DRCSR register as pointers that tag what area DROUTBUF and DRINBUF read and write enables a large number of external registers to be addressed. The following example will illustrate how this can be done using an external broadcast control and status register. A large number of external devices and registers can be communicated with through one port by using this technique. In simple terms this is a form of conditional indirect addressing.

As a simple example, assume the broadcast register format is as shown in Figs. 2 and 3. Both CSR0 and CSR1 are zero and a write operation is requested. This write is to all broadcast registers in all units. (The subsequent read operation will now only come from the unit selected that was written in the above write.) If no unit was selected, all 1's will appear on the data bus indicating that nothing was activated during readback. Now, in the simple case where CSR0 = 1 and CSR1 = 0 we now read and write only to the registers pointed to by the broadcast register pointer and unit selected. Unit selection is achieved with a simple decoder shown in Fig. 4. In this example, only eight units are possible. This could be extended, but consideration of bus loading and bus length to other units reduces the maximum number to no more than ten. In this example, eight switches, pull up resistors, and an 8-to-1 multiplexer (74LS151) are all that are needed to select a unit. When a large number of identical units are being used, each one can now be made to look like any other without changing the software. Only the switch positions need be changed. With this logic, a unit can be unselected by having all switches on. This allows for unselecting bad units without removing the hardware. The "on" position for each switch generates ground to the inputs D0, D1, . . . , D7 on the 8-to-1 multiplexer. To decode a module and generate the MODEN TRUE signal, only one switch should be turned off per unit. Switch one signifies unit 0 and switch position eight signifies unit 7 when the data select bits A, B, C on the multiplexer decode D0 through D7. That is when MODEN is TRUE. Table 1 illustrates the unit decoder operation; XXX in the Address column indicates "don't care" conditions.

The Broadcast Control and Status Register (BCSR) (see Fig. 5) addresses the decoded unit using bits ICSR06, ICSR07, and ICSR08. Bits ICSR00, ICSR01, ICSR02, and ICSR03 comprise the function register pointer. Bits ICSR04 and ICSR05 can be used to automatically increment the register pointer. The bit ICSR04 set to 1 will increment the function register pointer by one each time a function register is written to. With ICSR05 set to a 1 every time a function register is read, the pointer is incremented. Table 2 illustrates the decoding for reading and writing the function registers.

The broadcast register can be read only when MODEN is true. The tri-state buffer required on the BCSR is not shown. Bits ICSR09 through ICSR15 can be used individually for control and monitoring of needed internal tasks that must occur simultaneously on a number of units.

Figure 6 illustrates the buffers required for communication into and out of the DR11-C board. Additionally, the control decoding for reading and writing the registers and incrementing the function register pointer is illustrated. Figure 7 shows one type of function register that can be used. The clocks for reading and writing shown in Fig. 5 could control any type of register or control function. Each AM25S18 has both a register output plus a tri-state output to monitor its internal condition. This ensures that the busses used in the interface are functional. Only the first two 16 bit register files and the last register file are shown in Fig. 7. In Fig. 6, NDRDY* provides the clock when decoded in the 74138 for CKFR00, CKFR01, . . . , CKFR15. The function DTRAN* provides the read signal by way of the 74138 decoder for RDFR00, RDFR01, . . . , RDFR15. The function CKCSR loads data into the BCSR when CSR0 and CSR1 are both zero. The function FRDET is true when CSR0 is one and CSR1 is zero. The function CKPTR* increments the function register pointer every time a function register is read or written if the appropriate ICSR04* or ICSR05* bits are set. The signals DI00 through DI15 are data inputs to the function registers. DO00 through DO15 are function register data outputs.

IV. Conclusion

This simple interface is easily constructed and can be changed to suit a wide variety of interactive applications using the UNIBUS on a VAX computer. FORTRAN callable software drivers have also been developed at JPL to run under the VAX/VMS operating system. This type of interface was used by three different engineers while developing the Goldstone Solar System Radar and reduced three different types of hardware and software interfaces to only one.

Reference

1. "DR11-C General Device Interface User's Manual," Digital Equipment Corp., Maynard, Mass., 1978.

Table 1. MODEN decoding

Switch Positions								Address			MODEN
D0	D1	D2	D3	D4	D5	D6	D7	A	B	C	Y
0	0	0	0	0	0	0	0	X	X	X	False
1	0	0	0	0	0	0	0	0	0	0	True
0	1	0	0	0	0	0	0	1	0	0	True
0	0	1	0	0	0	0	0	0	1	0	True
0	0	0	1	0	0	0	0	1	1	0	True
0	0	0	0	1	0	0	0	0	0	1	True
0	0	0	0	0	1	0	0	1	0	1	True
0	0	0	0	0	0	1	0	0	1	1	True
0	0	0	0	0	0	0	1	1	1	1	True
0	0	0	0	0	0	0	1	0	0	0	False

Notes: 1. All eight positions can be individually decoded true and will not decode on all zeros or another switch position not selected.
2. Dip Switch Position: 0 = switch on, 1 = switch off.

Table 2. Function register write and read decoding

ICSR03	ICSR02	ICSR01	ICSR00	NDRDY*	DTRAN*	FRDET	Output Function True
0	0	0	0	1	1	0	All Outputs False
0	0	0	0	0	1	1	CKFR00
0	0	0	0	1	0	1	RDFR00
0	0	0	1	0	1	1	CKFR01
0	0	0	1	1	0	1	RDFR01
0	0	1	0	0	1	1	CKFR02
0	0	1	0	1	0	1	RDFR02
0	0	1	1	0	1	1	CKFR03
0	0	1	1	1	0	1	RDFR03
0	1	0	0	0	1	1	CKFR04
0	1	0	0	1	0	1	RDFR04
0	1	0	1	0	1	1	CKFR05
0	1	0	1	1	0	1	RDFR05
0	1	1	0	0	1	1	CKFR06
0	1	1	0	1	0	1	RDFR06
0	1	1	1	0	1	1	CKFR07
0	1	1	1	1	0	1	RDFR07
1	0	0	0	0	1	1	CKFR08
1	0	0	0	1	0	1	RDFR08
1	0	0	1	0	1	1	CKFR09
1	0	0	1	1	0	1	RDFR09
1	0	1	0	0	1	1	CKFR10
1	0	1	0	1	0	1	RDFR10
1	0	1	1	0	1	1	CKFR11
1	0	1	1	1	0	1	RDFR11
1	1	0	0	0	1	1	CKFR12
1	1	0	0	1	0	1	RDFR12
1	1	0	1	0	1	1	CKFR13
1	1	0	1	1	0	1	RDFR13
1	1	1	0	0	1	1	CKFR14
1	1	1	0	1	0	1	RDFR14
1	1	1	1	0	1	1	CKFR15
1	1	1	1	1	0	1	RDFR15

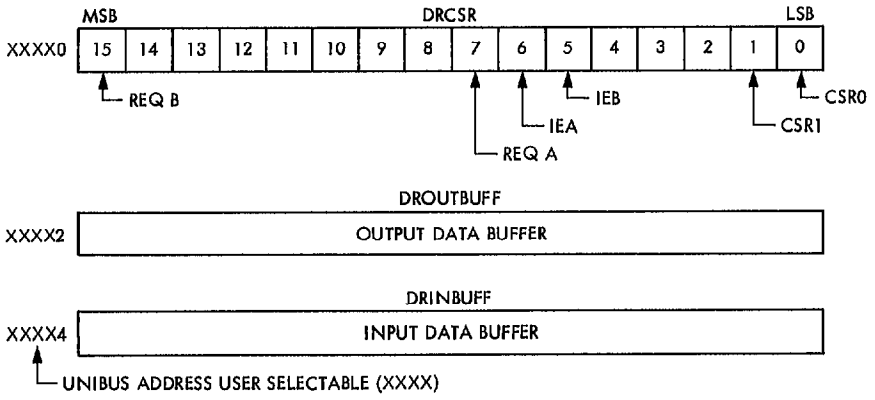
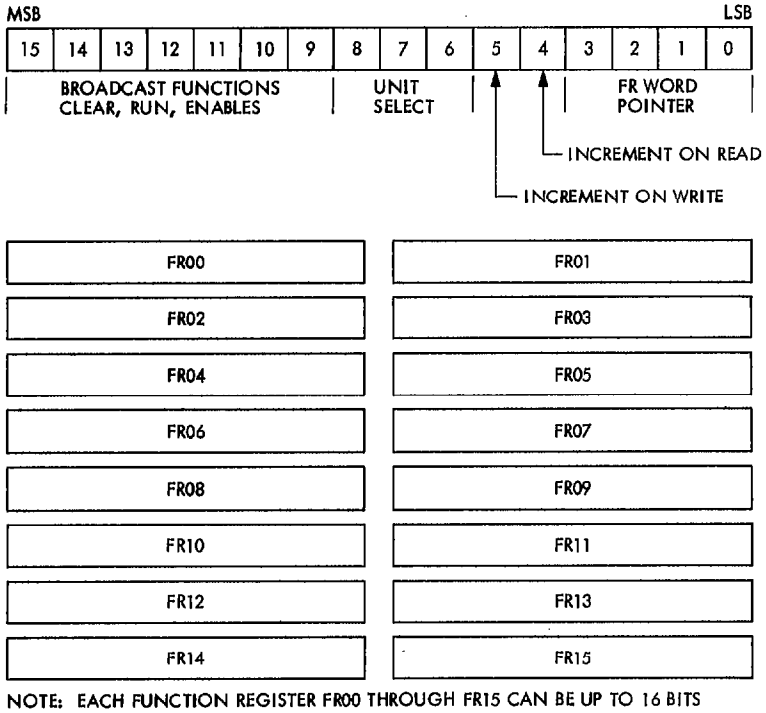


Fig. 1. DR11-C register assignments



NOTE: EACH FUNCTION REGISTER FR00 THROUGH FR15 CAN BE UP TO 16 BITS

Fig. 2. Broadcast control and status register with function register formats

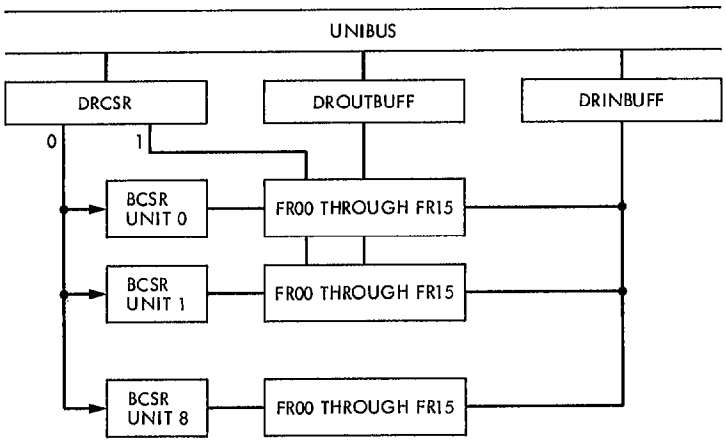


Fig. 3. Control and data flow diagram for register pointing

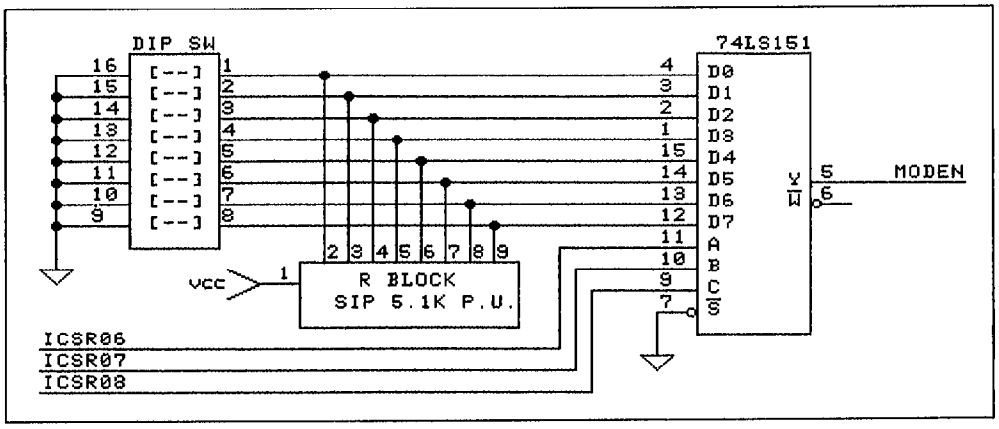


Fig. 4. Unit decoding

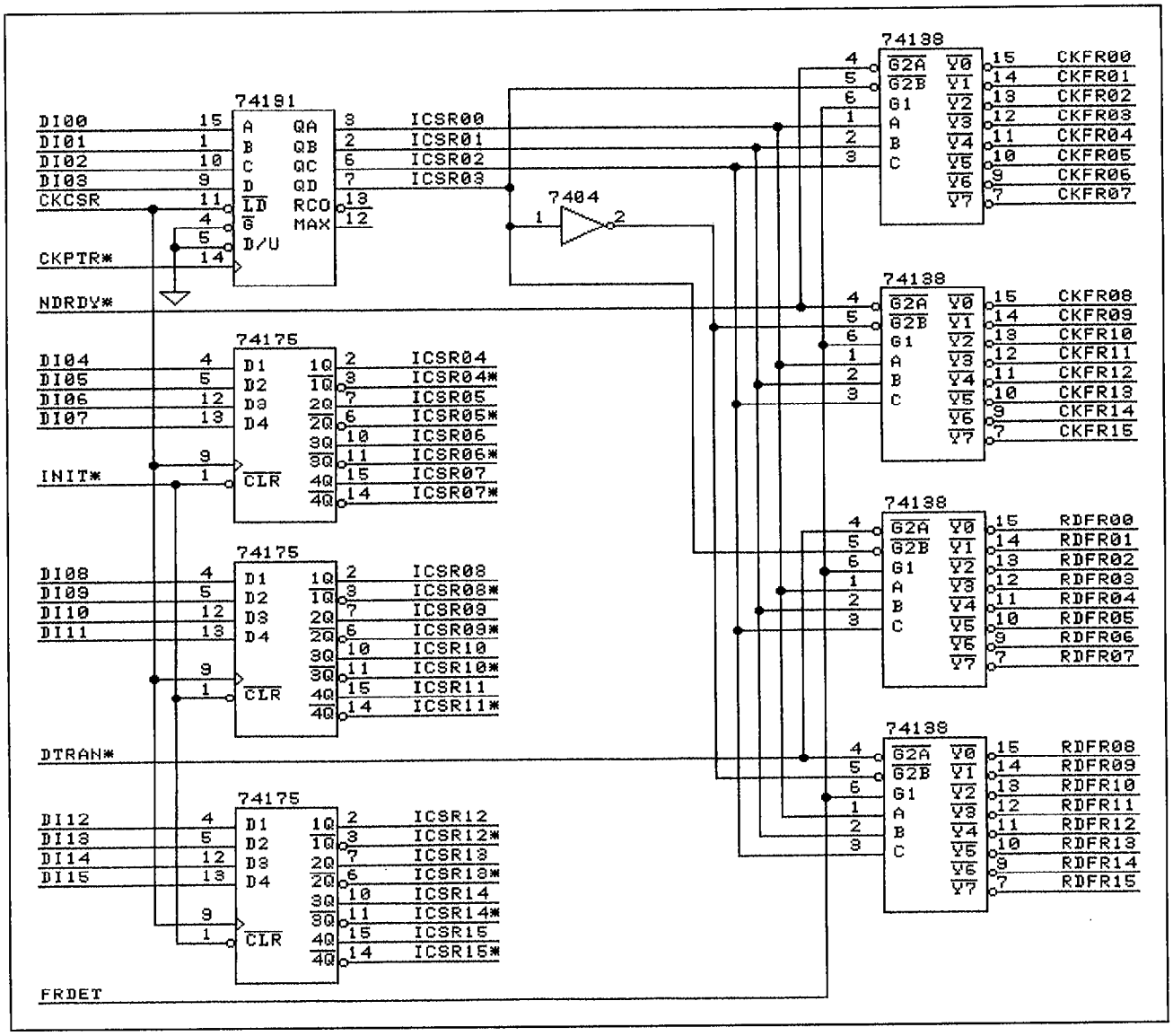


Fig. 5. Broadcast control and status register (BCSR)

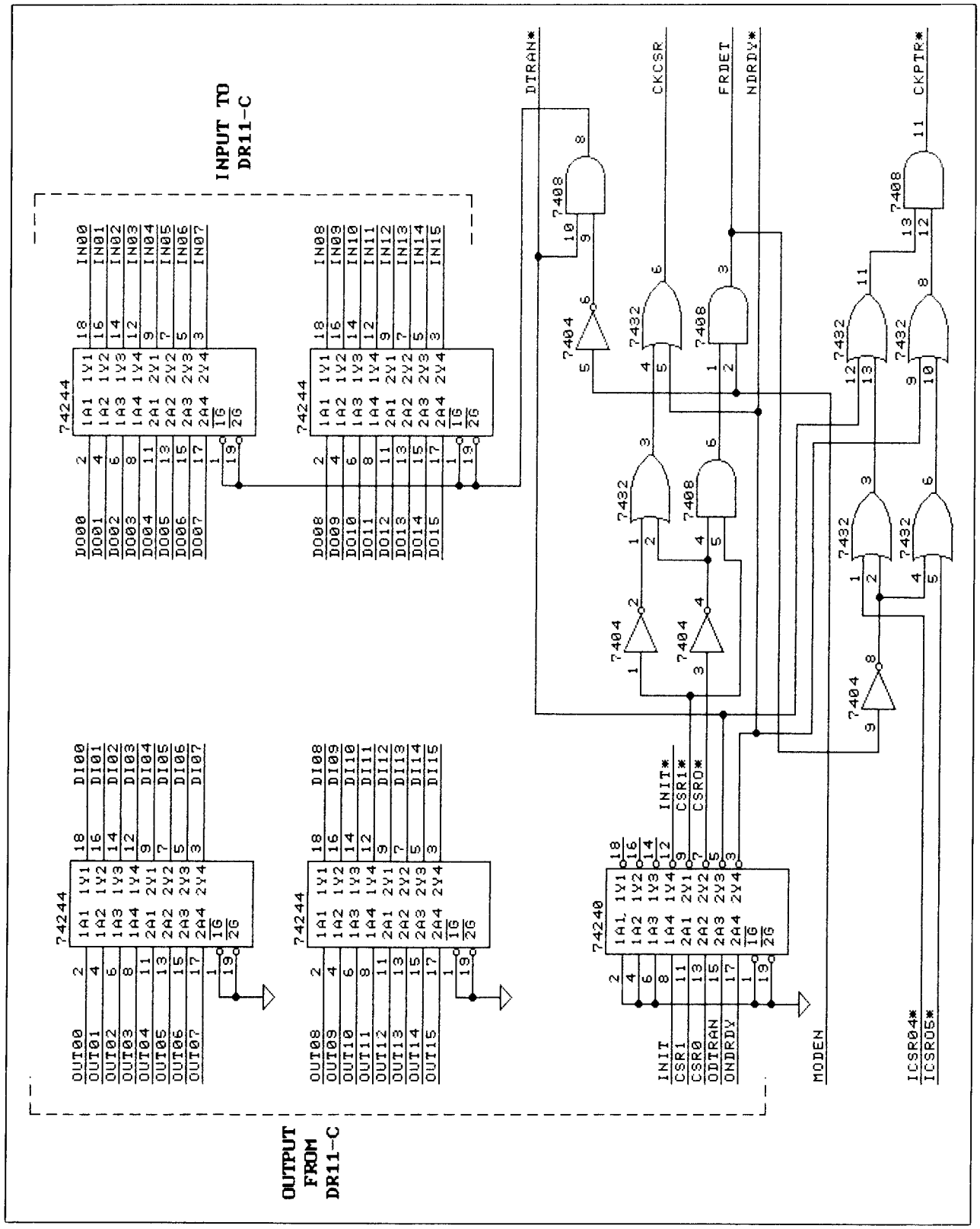


Fig. 6. DR11-C input/output buffers

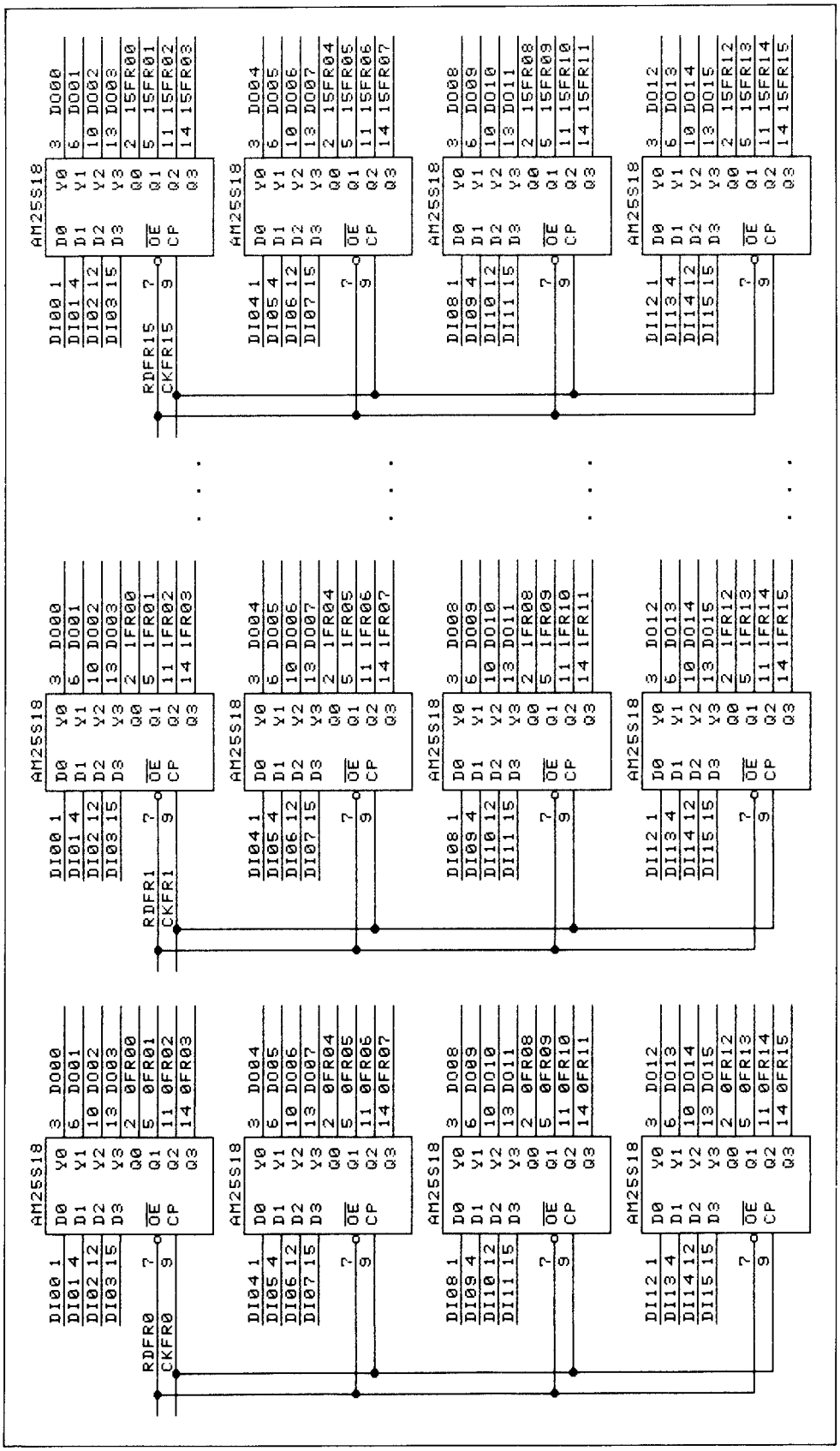


Fig. 7. Function registers