

DSN Advanced Receiver: Breadboard Description and Test Results

D. H. Brown and W. J. Hurd

Communications Systems Research Section

A breadboard Advanced Receiver for use in the Deep Space Network has been designed, built, and tested in the laboratory. Field testing was also performed during Voyager Uranus encounter at DSS-13. The development of the breadboard is intended to lead towards implementation of the new receiver throughout the network. In this article, the receiver is described on a functional level and then in terms of more specific hardware and software architecture. The results of performance tests in the laboratory and in the field are given. Finally, there is a discussion of suggested improvements for the next phase of development.

I. Introduction

The advent of high speed digital signal processing hardware over the last few years has enabled the application of digital solutions to classically analog problems. This, in many cases, has allowed for increased performance, while reducing cost and maintenance requirements. In the area of communications, signals can now be digitized and processed at rates high enough to allow for wide signal bandwidths, such as those required in communication systems found in the Deep Space Network (DSN). The Advanced Receiver (ARX) has been designed for the DSN and uses these advanced digital technologies as well as certain modern communication theory results, such as sideband-aided carrier tracking, to achieve improved performance over existing analog receivers. The theoretical background on the ARX has been well documented elsewhere [1-14]. The goal of the ARX project is to develop a receiver for implementation throughout the DSN. A breadboard ARX has been built and tested.

A. Receiver Description

The ARX is a hybrid analog/digital receiver which uses intermediate frequency sampling and digital phase locked loops to perform carrier tracking, subcarrier tracking, and symbol synchronization. It has been designed to avoid certain inherent problems associated with analog implementations such as DC offsets in mixers and amplifiers, and the need for precise RF calibration and adjustment. In addition, the digital system allows for more flexibility and increased reliability while reducing cost and space requirements.

Figure 1 shows the ARX broken into functional blocks. The receiver uses the open loop IF signal at 53 MHz from the RF front end and performs all subsequent processing through symbol detection. In the IF assembly, the carrier phase locked loop is locked to a submultiple of the sampling rate, as described in section IIA, and then the signal is digitized. All further processing is digital. The receiver performs the carrier

tracking functions currently handled in the Deep Space Stations by the Block III and Block IV receivers, in addition to the subcarrier tracking and symbol synchronization functions of the baseband assembly (BBA). The ability to fit all of the signal processing into one chassis reduces the number of interfaces between subsystems and thereby increases reliability. It also greatly simplifies the implementation of sideband aided and fully suppressed carrier tracking, since the carrier, the subcarrier, and the symbols are processed in the same assembly.

B. Scope of Article

This article describes the design, development, and testing of the advanced receiver. This includes theoretical concerns, hardware and software design, and the results of tests in the laboratory and in the field. It is shown that the receiver performance compares well with expected results in all areas. In some areas, test results suggest improvements which could be made.

II. Breadboard System Description

The breadboard ARX consists of three modules: an intermediate frequency assembly (IFA), a signal processing assembly (SPA), and a test signal assembly (TSA). The IFA performs intermediate frequency sampling, and serves as the point of closure for the carrier and symbol loops. The SPA contains all of the digital signal processing hardware and software which is necessary to operate the three loops. The TSA uses built-in fixed frequency oscillators or externally supplied reference frequencies to generate IF test signals. A block diagram is shown in Fig. 2.

A. Intermediate Frequency Assembly

The IFA interfaces the receiver to the station. Its block diagram is given in Fig. 3. The input to this assembly is an IF signal which has been open loop down converted to approximately $53 \text{ MHz} \pm 0.5 \text{ MHz}$. The signal is then bandpass filtered before passing through a total power automatic gain control (AGC). Then the carrier loop is closed by mixing the output of the AGC amplifier with the carrier reference. The carrier reference signal is produced by mixing a constant 46.25 MHz signal with the output of the carrier loop numerically controlled oscillator (NCO), and has a nominal resulting value of 48 MHz . After the AGC output is mixed with the carrier reference, it is filtered and digitized by the A/D. The clock input to the A/D is the sum of frequencies of a fixed 18.0 MHz reference and the symbol synchronization loop NCO. It has a nominal value of 20 MHz and serves to close the symbol synchronization loop. The carrier and symbol loops are linked in such a way that the received carrier frequency is phase

locked to exactly $1/4$ of the A/D sampling rate, and there are a constant integer number of samples per symbol.

This sampling process is known as intermediate frequency (IF) sampling [1]. The carrier is not demodulated to analog baseband for phase detection, but instead is phase locked to a known reference before being digitized, in this case one quarter of the sampling rate. Demodulation and phase detection are done digitally. This technique removes the effect of any DC bias in the A/D converter, since the DC component will be translated out of band when the signal is digitally mixed to baseband. Locking to a multiple of the symbol rate, known as synchronous IF sampling, has the added advantage of easing the carrier demodulator implementation (see section III), though problems may arise at low signal-to-noise ratio (SNR) due to the A/D clock coupling into the signal path (see section VIII).

B. Signal Processing Assembly (SPA)

The SPA contains the signal processing hardware and software. Figure 4 shows the SPA in block diagram form and Fig. 5 shows the signal processing hardware in more detail. The SPA performs the operations which implement the phase detectors and loop filters for the carrier, subcarrier and symbol loops. It also contains hardware and software for fast acquisition and signal parameter estimation.

1. Residual carrier phase locked loop. Residual carrier phase detection is accomplished using the quadrature (Q)-channel samples. The phase detector output is the sum of some fixed number, N , of consecutive Q-channel samples. A complete mathematical analysis is given in [1]. This summation imposes a low pass filter operation on the channel with bandwidth determined by the number of samples in the sum. The effect of this filtering operation can be assumed to be negligible as long as the effective filter bandwidth is wide compared to the bandwidth of the carrier phase locked loop.

The gain at the output of the hardware phase detector is a function of the number of Q-channel samples in the sum, the square root of the power in the carrier, and any hardware scaling constants. This phase detector output is then passed to a microprocessor which implements type II and type III loop filters as described in [2].

Carrier amplitude is estimated by summing the inphase (I)-channel samples over the same time interval as the carrier phase detector. The signal is further summed in software and then scaled to produce the estimate.

2. Subcarrier phase locked loop. The subcarrier phase detection and synchronization is done by employing an optimum Costas loop. A complete mathematical analysis is

given in [1]. The carrier Q samples are multiplied in the two arms of the Costas loop by phase quadrature square wave reference signals at the subcarrier frequency. The products in the two arms of the Costas loop are then summed over one symbol time to implement matched filter detection. These phase quadrature symbol time sums are multiplied together and summed over a longer interval to produce the phase detector output. The subcarrier phase detector gain is given by the number of terms in the phase detector sum, the hardware gain factors, and the ratio of data power to noise spectral density. As for the carrier loop, the microprocessor implements type II or type III loop filters.

3. Sideband-aided carrier tracking. The Advanced Receiver also has the ability to perform sideband-aided carrier tracking after subcarrier lock is achieved. In this scheme, a Costas type phase detector is implemented for carrier tracking by adding a third arm, with carrier inphase and subcarrier inphase. The other arm of the carrier Costas loop is carrier quadrature, subcarrier inphase. The output of the carrier Costas phase detector is added to the output of the residual carrier phase detector with appropriate weighting [1].

4. Symbol synchronization loop. A transition tracking symbol synchronization loop is used, as described in [18]. Symbol phase detection is accomplished by summing across symbol transition windows. The summation is multiplied by the transition direction (-1, 0, +1) and then these products are summed over a longer interval. The width of the window is selectable from software.

Detector gains are given by the hardware gains and the data signal level. The gain does not depend on the window width, provided the symbol transition is within the window. The phase detector output is filtered in a type II or type III loop as above.

5. SNR and signal parameter estimation. Integrated symbols are used to estimate symbol SNR by applying the split symbol SNR estimator as described in [19] for the Baseband Assembly Demodulation Synchronization Assembly. The symbol squared and early-late products are averaged in hardware and then combined in software to produce the estimate.

The SPA produces estimates of signal parameters based on observed quantities measured during signal processing. Parameters measured include carrier power to noise spectral density (P_c/N_0), data power to noise spectral density (P_d/N_0), and steady state carrier phase error (ϕ_{ss}).

6. Fast acquisition. The SPA also performs signal processing for fast acquisition. Fast acquisition is implemented by doing an FFT on the complex I and Q pairs at the output of

the carrier phase detector. A sinusoid at the output of the phase detector indicates a frequency difference between the input carrier frequency and the mixing reference. The frequency of this sinusoid is then fed back as a correction to the initial prediction of carrier frequency.

C. The Test Signal Assembly (TSA)

The test signal assembly provides modulated signals for test and evaluation of the advanced receiver and is shown in block diagram form in Fig. 6. The reference frequencies for the test assembly can be generated by internal oscillators which supply fixed frequencies or by external synthesizers. An internal noise generator injects noise into the signal. Signal to noise ratios and modulation indices are controlled by attenuators for the carrier, data and noise channels. The test assembly uses three input frequencies, a carrier, a subcarrier and a symbol clock, to form a residual carrier signal biphase modulated with a square wave subcarrier. The TSA can also produce direct carrier modulated signals and Manchester coded signals. The data can be either the data clock or a repetition of a 1023-bit-length pseudonoise (PN) sequence that is generated in the TSA.

The internal crystal oscillators are tuned to produce a Voyager II type signal. The test carrier frequency is 53 MHz, the nominal down-converted down link frequency. The subcarrier is at 360 kHz and the symbol rate is 43.2 kbps. This configuration is used in the field when no external synthesizers are available.

III. Signal Processing Hardware

The signal processing assembly contains digital signal processing, control, and system hardware in a Multibus I enclosure. The boards in the Multibus chassis are:

- (1) Intel SBC-8614 Single Board Computer (SBC)
- (2) Array Processor
- (3) 512K RAM Card
- (4) Serial I/O Card
- (5) Disk Controller Card
- (6) Signal Processing (SP) Board
- (7) Timing and Control (T&C) Board
- (8) Two Numerically Controlled Oscillators (NCOs)

In addition, there is a display monitor for operator interface and a dual floppy disk drive for program storage and data logging. The CRT, disk drives, and the RAM, I/O, and disk controller cards fall into the category of system hardware

and are used for monitor and control of the breadboard ARX. They are not fundamental to receiver operation.

The signal path through the SPA is shown in a block diagram in Fig. 5. The digitized signal from the IF assembly is fed to the timing and control board, where it passes through a complex demodulator producing an I channel and a Q channel. The I and Q data and timing signals then go to the signal processing board and into a bank of multiply-accumulate chips (MACs) which produce carrier, subcarrier, and symbol phase error signals and signal statistics. The phase detector outputs are input to the SBC which implements the three loop filters. The filter outputs are the control signals that drive the carrier, subcarrier, and symbol NCOs, and close each of the loops. The SBC also processes signal statistics to produce estimates of signal parameters. In the fast acquisition mode, the SBC passes I and Q channel values to the FFT processor and processes the resulting transforms to obtain frequency estimates.

A. Sampling and Carrier Demodulation

Synchronous IF sampling allows the T&C board to perform the complex carrier demodulation without the use of a multiplier. In the synchronous IF sampling scheme, the digital demodulating frequency is identically 1/4 of the sampling rate. Complex demodulation requires quadrature references. These are easily obtained by recognizing that the sine and cosine reference signals have only four values per cycle, since there are only four samples per cycle of input carrier. The sine and cosine arguments can then be chosen to be multiples of $\pi/2$ radians, which results in the reference signal taking on values from the repeating stream (. . . 0, 1, 0, -1 . . .). Thus in this special case, demultiplexing into odd and even samples and then multiplying alternately by +1 and -1 is equivalent to complex demodulation followed by the summing of every two consecutive samples in each channel. It should be noted that the summation of consecutive samples is valid only when the phase information is narrow band in relation to the sampling frequency. The summation is actually a crude low pass filter operation, which could introduce amplitude distortion, with a normalized frequency transfer function of the form [20]

$$H(\nu) = \left(\frac{1}{N} \right) \left[\frac{\sin \left(N\nu \frac{\pi}{2} \right)}{\sin \left(\nu \frac{\pi}{2} \right)} \right]$$

where

N = number of terms in the sum

ν = normalized frequency = $2f/f_s$

B. Timing and Control

Multiply-accumulate chips (MACs) are used for subcarrier demodulation, symbol integration, phase error accumulation over fast (carrier) and slow (subcarrier and symbol) loop filter update periods, and SNR estimation. The accumulation period for each of these MACs is controlled by a series of counters on the T&C board. These counters are loaded from software computed values during the hardware initialization routine.

C. Signal Processing

There are 12 MACs on the signal processing board which perform the necessary operations for tracking and data detection. In addition, the integrated symbol values are passed to an external device for decoding or other further processing. The MACs and the signals they produce are shown in Fig. 5. Seven signals are used by the SBC, and five intermediate values are used only by the SP board. Since the signals these devices produce are the key outputs of the signal processing hardware, they are described below.

- (1) RCE is the sum of Q-channel samples over one carrier update period and is used as the residual carrier phase error signal.
- (2) AMP is the sum of I-channel samples over one carrier update period and is used as a measure of carrier amplitude.
- (3) DCE is the output of a carrier Costas-type phase detector formed by the product of the inphase carrier and inphase subcarrier channels, summed over one carrier update period and is used as the data aided carrier phase error signal. A weighted sum of RCE and DCE is the input to the carrier loop filter.
- (4) SCE is the subcarrier Costas loop phase output. First, carrier Q-channel samples are multiplied by subcarrier inphase and quadrature square wave references, and the products are summed over one symbol time to form the matched arm filter outputs. Then the product of these channels is taken and summed over one subcarrier update period to form the subcarrier phase error signal.
- (5) SSE is the symbol synchronization loop phase output. It is formed by summing carrier Q-channel samples across a symbol boundary and multiplying this sum by the output of a transition detector [18], and then summing this over several symbols. The width of the summation window around the boundary is a software selectable fraction of one symbol time. When the phase error is small and there is a transition, the sum across that transition is proportional to the magnitude of the

phase error, and its sign is given by the product of the sign of the sum and the sign of the transition.

- (6) PWR and MSQ are the two signals used to compute the split symbol estimate [19] of the ratio of symbol energy to noise density (E_s/N_0). PWR is formed by squaring the sum of the samples in one symbol, and summing these squares over one subcarrier update period. MSQ is formed by multiplying the sum of the samples in the first half of a symbol by the sum of the samples in the second half of that symbol, and summing this product over one subcarrier update period. These values are combined in the software to produce the estimate of E_s/N_0 .

The above signals are read by the SBC. The RCE, DCE, SCE, and SSE signals are all input to the digital loop filters implemented by the SBC. The output of the carrier and symbol synchronization filters go to the NCOs. The NCOs in turn output analog signals to the IF assembly. The output of the subcarrier filter goes to the subcarrier NCO, which is located on the T&C board. The RCE signal is also combined with AMP to produce an estimate of carrier phase angle. The SNR and PWR signals are combined to form the estimate of E_s/N_0 . The following signals are intermediate results used only by the SP board.

- (7) QSMODE is the summation of the inphase subcarrier channel over one symbol time. The inphase subcarrier channel is formed by taking the product of the carrier quadrature channel and the internally generated sine phase subcarrier reference. It is used as the soft output symbol value. It is also used by the SP board for transition detection, as the inphase arm of the subcarrier Costas loop, as the quadrature arm of the sideband aided carrier loop, and is squared to form PWR.
- (8) QCMODE is the summation of the quadrature subcarrier channel over one symbol time. The quadrature subcarrier channel is formed by taking the product of the carrier quadrature channel and the internally generated cosine phase subcarrier reference. The QCMODE signal is used as the quadrature arm of the subcarrier Costas loop.
- (9) ISMODE is the summation of the product of the carrier inphase and internally generated sin phase subcarrier reference, over one symbol time. It is used as the inphase arm of the sideband aided carrier loop.
- (10) DQSMMDM is the summation of the inphase subcarrier channel across the symbol transition over the software selected window width. It is used to form SSE.

- (11) DQSH is the summation of the inphase subcarrier channel over one-half of one symbol time. It is used to form MSQ.

D. Scaling

The output detected symbol value is the summation of the inphase subcarrier channel over one symbol time and can be written as

$$D(nT_s) = \sum_{k=nN}^{((n+1)N)-1} (\text{SCALE} * [2^{2*\text{MODE}}] * \sin[\omega_{sc} kT + \hat{\phi}] * q[kT])$$

where SCALE and MODE are software selectable scaling constants. This is the output of the subcarrier inphase arm MAC. When E_s/N_0 is greater than -3 dB, SCALE and MODE are set such that the mean value of the output data is 21.5 binary units for compatibility with current telemetry processing equipment. At $E_s/N_0 = -3$ dB, the noise standard deviation is equal to the signal mean. When E_s/N_0 is less than -3 dB, the noise dominates, and summation overflow could occur. Therefore, at SNRs below -3 dB, the scaling factors are chosen so that the standard deviation of the noise is 21.5.

The values assigned to MODE and SCALE are computed by the SBC based on *a priori* signal parameters. The value of MODE is determined by the symbol rate. If the symbol rate is less than 1 kps then it is set to one, otherwise it is set to four. This is to prevent overflow in the accumulators at low symbol rates. Once MODE is fixed, SCALE is calculated as above and quantized to one of sixteen levels. The SCALE value is introduced into the signal stream through the subcarrier reference signal. The output of the NCO that produces the sine and cosine waveforms necessary for the subcarrier Costas loop is modified by two PROMs. These PROMs take the sine and cosine amplitudes, the SCALE value, and four control signals to produce the references. The control signals select between sine wave or square wave subcarriers, and non-return-to-zero or Manchester modulation, and can also select signals for testing.

E. Fast Acquisition Processing

An array processor is used to perform FFT processing for fast acquisition. When in the fast acquisition mode, the SBC stores consecutive values of RCE (carrier Q channel) and AMP (carrier I channel). The AMP and RCE signals are combined to form the complex value

$$X(t) = \text{RCE} + j \text{ AMP}$$

After 128 values of $X(t)$ have been collected, the SBC passes the location of the data in shared memory to the array processor, which computes the magnitude squared of the complex FFT. This process is repeated four times and the power spectra are accumulated. The array processor then does a "peak pick" which is a procedure which returns the number of the FFT bin which had the highest magnitude response. From this number, an estimate of the frequency difference between the actual input signal and the carrier reference is derived. This offset is added to the initial carrier reference frequency and the loops are enabled. The range of frequencies covered by the FFT is equal to the carrier loop update rate, and is divided into 128 frequency bins.

IV. Signal Processing Software

Loop filter implementation and overall control are orchestrated by the Advanced Receiver software. The operation is divided between real time interrupt driven routines to perform the loop filter operations and a background process that communicates with the user and does low rate computations.

A. Environment

The Advanced Receiver software was developed on an 8086/87 processor based system running under the CP/M operating system. The majority of the code (4000 lines) is written in Pascal with the remaining code in assembly language. The software was developed on the target system, which proved advantageous in the research and development phase. This approach is not recommended for the implementation phase, where the use of separate reusable development systems would be a more cost effective allocation of resources.

B. Structure

The Advanced Receiver software maintains two key run time processes: loop filtering and user interface. The loop filter process is timing critical and therefore is the higher priority or foreground process. The user interface is the lower priority background process. In addition, the software controls the hardware and software initialization routines.

The loop filter processing is an interrupt driven foreground process. The phase detector outputs, which are input to the loop filters, are generated on the signal processing board. When phase data are ready, an interrupt is generated by the signal processing board and one of the interrupt service routines responds by reading and processing the new data. The interrupt service routines are written in assembly language to increase speed. There are two interrupt routines; one that services the carrier loop only, and one that serves all three loops. This enables the carrier loop filter to be updated more frequently

and enables wider bandwidth carrier loops. After an interrupt has been serviced, program control returns to the background process.

The background process handles the calculation and display of system parameters and control of the receiver configuration. Menu selectable displays allow the user to select loop configurations and input *a priori* signal information or predicts. While the receiver is running, there are menu selectable displays for each loop's performance and an overall system performance display.

C. Dynamic Filter Modification

An important feature of the software architecture is the ability to dynamically change loop parameters, or change filters "on the fly." In other words, it is possible to change loop bandwidths, loop types, and damping coefficients without losing lock. This is possible due to the interrupt driven nature of the loop filters and the careful implementation of the filter equations. This is important since lock acquisition can be accomplished with wide bandwidth type II loops, and then the loops can be changed to narrow bandwidth type III loops for low phase jitter tracking.

The interrupt driven nature of the code helps to facilitate dynamic filter modification. When the operator requests a change in any or all of the tracking loop filter bandwidths, the background process begins to compute new filter coefficients. Meanwhile, the foreground process continues to service the interrupts and to process the incoming data using the current loop parameters. Once the new coefficients have been computed and stored into memory, the address pointer to the location of the filter coefficients is toggled such that the next time an interrupt service routine is called, it will use the most recently computed coefficients.

The loop filter equations must be implemented in such a way that avoids sharp discontinuities in filter output when loop parameters are changed. The digital transfer function of the loop filter used is of the form [2]

$$F(z) = G_1 + G_2 \left(\frac{Tz}{[z - 1]} \right) + G_3 \left(\frac{T^2 z^2}{[z - 1]} \right)$$

where G_1 , G_2 , and G_3 are filter coefficients and T is the sampling period. The second and third terms represent scaled single and double integrators in the z domain respectively. The second term is implemented as the sum of all previous inputs and the third term as the sum of all previous sums of inputs. The filter output can be written as

$$y(k) = G_1 x(k) + G_2 \sum_{i=0}^k x(i) + G_3 \sum_{i=0}^k \sum_{j=0}^i x(j)$$

Intuitively, the first term can be viewed as the phase correction term, the second as the frequency (velocity) correction term, and the third as the frequency rate (acceleration) correction term. If the gain coefficients vary with time, than a change in these coefficients should not perturb the previous corrections in phase, frequency and frequency rate. In order to account for the time varying nature of the loop coefficients, these coefficients must be brought inside the summations as below

$$y(k) = G_{1k} x(k) + \sum_{i=0}^k \left[G_{2i} x(i) + \sum_{j=0}^i G_{3j} x(j) \right]$$

where the second subscript on the G 's indicates time dependance.

V. Receiver Operation

The ARX breadboard was designed as a research tool to validate ARX concepts. While it is not designed for use by operators in the field, its menu driven structure makes using the receiver simple and easy to learn. The normal operating mode would correspond to the maintenance mode of an implemented receiver whose prime user interface would be the Link Monitor and Control (LMC).

A. Breadboard Receiver

The current configuration of the ARX is designed for direct operator control, as this most easily lends itself to development and testing. All monitor and control functions are passed on an RS232 connection between the receiver and a CRT monitor. The operator enters signal characteristics and tracking requirements on the keyboard and then observes key performance parameters on the display screen.

The receiver software is fully menu driven. There are three levels of menus. From the main menu, the operator selects from one of these six options:

- (1) Review and modify parameters
- (2) Run self test
- (3) Run real time
- (4) Run real time with fast acquisition
- (5) Log data
- (6) Reinitialize (reinitialization).

At any time, the operator can exit from the main menu to the CP/M operating system. After selecting an activity from the main menu, the operator is presented with the appropriate submenu for that activity. Thus the operation of the receiver is self documented.

The "Review and modify parameters" option is selected when the loop or data parameters are to be changed or examined. Submenus include data specifications, carrier, subcarrier, and symbol loop parameters, and filter update rates. The entire receiver configuration can also be stored onto and recalled from a floppy disk. This allows for the storage of different receiver configurations which can easily be recalled and reloaded.

The "Self test" module runs a built-in hardware self test that is in ROM in the hardware. This module is still under development.

There are two real time tracking options. The first, "Run real time," executes the basic receiver software. This software implements the loop filters, collects and processes statistics on loop performance and signal characteristics, and controls the output of information to the screen.

The second real time tracking option, "Run real time with fast acquisition," executes an FFT on the carrier inphase and quadrature channels to determine the error in initial frequency estimate. This information is then fed back and a new frequency estimate is produced. This estimate is used as the center frequency for the carrier phase lock loop and the loops begin operation as in the "Run real time" option. Lab experimentation has shown that with the fast acquisition utility, carrier lock can be achieved in less than 2 seconds in the presence of Doppler rates in excess of 1 Hz/sec over a range of ± 250 Hz.

The main menu option "Log data" allows the user to toggle a software switch which controls data logging to a floppy disk. When this switch is on, tracking statistics and configuration information are written to a disk for later analysis. Data logging is transparent to the user.

The final option available in the main menu is "Reinitialization." Selecting this option resets and reinitializes all hardware and software. It is equivalent to restarting the program.

B. Operation of ARX for DSN Implementation

Current plans are that the receiver implemented in the DSN will have two distinct operating modes: normal mode and maintenance mode. The receiver will most often be in the normal mode, where it will receive commands from the

station operator via the LMC network. The maintenance mode will be reserved for times when the receiver requires testing, repairs, or modification. The maintenance mode can also be used if there is a failure of the LMC or LMC interface.

The normal mode will include several features that simplify the operation of the receiver. Routine acquisition is envisioned as a two step process. First, radiometric predicts are loaded into the receiver via the LMC. Then the receiver is commanded to acquire downlink. This command initiates an acquisition strategy which includes an FFT frequency search, fast acquisition, lock detection, and automatic bandwidth reduction. The receiver will constantly monitor its own performance. The operator also has full control to set the receiver configuration in a manual acquisition mode. Simple "help" utilities and menu driven options will further simplify operation.

The maintenance mode will facilitate field servicing and allow the receiver to be operated through a maintenance port, bypassing the LMC. This mode will make available diagnostic routines and monitor functions. In the maintenance mode, the receiver will be able to be operated as if from the LMC. In addition, test routines will exercise individual hardware and software blocks, simplifying the trouble shooting process. Access to board level monitor functions will allow the downloading of special test routines, and the loading and testing of new modules of the receiver software.

VI. Laboratory Tests

The Advanced Receiver breadboard has undergone initial testing in the laboratory. Tests have been conducted to determine its tracking and acquisition performance, phase jitter, and phase bias. These tests have proven valuable in giving confidence to initial assumptions and revealing areas in which modifications for the future are indicated.

A. Range of Operation

Tests were done to determine the range of functional operation of the receiver under different configurations. Laboratory results have shown the receiver can track effectively under the following conditions:

Carrier Frequency	53 MHz \pm 0.5 MHz
Subcarrier Frequency	20 kHz to 960 kHz
Symbol Rate	36 sps to 200 ksp/s
Symbol SNR	-20 dB to +25 dB

These results are preliminary and do not reflect the full operating range of the receiver. The lower limit on symbol

SNR is higher at lower symbol rates due to practical limitations on how narrow the symbol and subcarrier loops can be made. Further tests of operating limits will be determined and published at a later date.

B. Fast Acquisition and Tracking Under Voyager Conditions

Tests were done with the ARX to simulate Voyager II signal characteristics as received at a 26-meter antenna, such as DSS-13 at Goldstone. The signal parameters are tabulated below.

Carrier Frequency = X-Band (Open loop downconverted to 53 MHz)

Subcarrier Frequency = 360 kHz

Symbol Rate = 43.2 ksp/s

Modulation Index = 72 deg.

E_s/N_0 = -10 dB

Doppler Rate Uncertainty (df_c/dt) = 1 Hz/s

P_c/N_0 = 26.6 dB-Hz

The Doppler rate uncertainty was simulated by sweeping the carrier frequency synthesizer input to the test signal assembly at the appropriate rate.

Initial acquisition of this signal was achieved with the following receiver configuration.

Carrier Loop

Bandwidth = 10 Hz
Loop type = II

Subcarrier Loop

Bandwidth = 0.1 Hz
Loop type = II

Symbol Sync Loop

Bandwidth = 0.1 Hz
Loop type = II

Using the FFT based fast acquisition scheme, the receiver was able to lock to the above signal and produce good symbol SNR estimates with a better than 99% success probability in less than 20 seconds. This is as fast as can be expected since the SNR estimates are only made once per 10 seconds.

After initial acquisition, the carrier loop parameters were modified to improve performance. In order to reduce phase jitter, the loop bandwidth was reduced from 10 Hz to 3 Hz. There is a limit however, to the minimum amount of bandwidth necessary in a type II loop in the presence of dynamics. The steady state phase error for a type II loop is proportional to the frequency rate divided by the square of the loop bandwidth. Thus, to allow for further bandwidth reduction and thereby improved loop SNR, the carrier loop was changed to a type III loop, which has zero static phase error for constant frequency rate. Table 1 shows the loop SNR and static phase error in the different stages of acquisition. After the type III loop is implemented, the static phase error goes to zero as expected. Then the bandwidth is further reduced to 1 Hz with a resulting loop SNR of 26.6 dB.

C. Swept Acquisition Test

The Advanced Receiver breadboard was tested for its ability to acquire high dynamic carrier signals. These are characterized by Doppler rates that are higher than the current FFT processor could handle without smearing. One hundred trials were performed [10] for three different loop parameter cases, each with an initial frequency offset of ten times the loop bandwidth. The loop bandwidth was set to 10 Hz and the carrier loop SNR was set to 13 dB for each case. Table 2 shows the sweep rate, measured probability of acquisition, and theoretical probability of acquisition for each of the three cases. There is a good level of agreement for cases 1 and 2, using type II loops. The discrepancy between actual and expected results in case 3, where type III loops are used, can be attributed to small DC offsets in the carrier phase detector output, which accumulate quickly in the double integrator of the third order loop.

D. Phase Error Jitter Measurements

Measurements were made on the carrier loop phase jitter in the presence of varying amounts of noise (Rafferty, Wm., "Phase Error Jitter Measurements on the Advanced Receiver Residual Carrier Phase Locked Loop," JPL Internal Document, IOM 331-86.5-117, Jet Propulsion Laboratory, Pasadena, Ca, May 15, 1986). The results were compared to those predicted by standard linear theory with favorable results. Under typical operating conditions, such as those experienced at Voyager II Uranus encounter, the measured phase error variance as a function of loop signal to noise ratio was within 1 dB, worst case, of that predicted by linear theory.

In the simple case of the unmodulated carrier tracking loop, the linear model of the relation of phase error variance, σ_ϕ^2 , to loop SNR, SNR_L , is given by

$$\sigma_\phi^2 = 1/\text{SNR}_L$$

In Fig. 7, the above function is plotted along with the phase error variance results derived from experimental data. From the figure we see that the carrier phase locked loop agrees well with linear theory. The divergence of the linear theory from the actual measured curve at high SNR is not unexpected due to the presence of a noise floor in the phase locked loop which becomes apparent at high SNR. The ARX carrier loop implementation is in close agreement with the discrete time difference equations when operating in the normal region of loop SNRs, from 10 dB to 30 dB.

E. Phase Bias Measurements

During various tests and operation of the receiver, it has been observed that there is a static phase error at low SNR due to bias in the carrier phase detector output. This is evidenced by the fact that the measured carrier power is sometimes higher when there is a Doppler rate than when there is no Doppler rate. This occurs with a type II loop when the phase error due to Doppler rate cancels the phase error in the phase detector. Further, when the carrier loop is not closed, the mean value of the phase detector output is not zero; instead it is a nonzero value that varies over time and with relative physical positioning of the IFA and the SPA. Various attempts were made to eliminate or reduce the bias. These included adding power supply isolation between the A/D and IF circuits, shielding the A/D converter, and rerouting cables. The bias changed with configuration, but was not substantially reduced. One possible cause of this bias is on the A/D card itself, or even on the conversion chip.

A test was run to determine if the coupling between the digital processing and the IF and the A/D circuitry caused the problem. The A/D was tested with a noise input, but without running the normal digital circuitry. A separate test circuit was used to measure the bias, instead of the normal processing. The test setup measures the power at one quarter of the sampling frequency when the input to the A/D is gaussian noise, which is white relative to the bandwidth of the sampling process. A signal at one quarter the sampling rate is periodic in four samples. Thus the amplitude of this component can be measured by mixing the A/D output with a frequency at one-fourth of the sample rate, much in the same way that carrier amplitude is measured in the carrier inphase channel in the receiver. To ease the implementation, only the sign bit was examined and the results were averaged over several seconds to reduce the variance of the noise.

The actual test involved designing a circuit to demultiplex the A/D output into four time sequential channels. The A/D was clocked at 20 MHz and the number of negative A/D outputs for each channel over a 10-second period was then recorded. Analysis of the results showed that the amplitude of

the bias term is in the order of several ten thousandths of a least significant bit, which corresponds to a ratio of interference power to noise spectral density of 5 dB-Hz to 10 dB-Hz. This value becomes significant when tracking very weak signals, such as Pioneer 10 at a 64-m station, with P_c/N_0 approximately 14 dB-Hz. The effect was significant, but not dominant in tracking Voyager from DSS-13, with P_c/N_0 24.4 dB-Hz as discussed in section VII.

VII. Demonstration at Voyager 2 Uranus Encounter

On January 24, 1986 the Advanced Receiver tracked the Voyager 2 spacecraft at Uranus encounter. This field test was performed at DSS-13, Goldstone, California. During the encounter, the receiver locked onto and tracked the residual carrier, subcarrier, and symbol stream. The overall receiver performance met all expectations.

The carrier signal to noise spectral density ratio was typically 24 dB-Hz, with some variation due to changing modulation index and elevation angle. Type III residual carrier phase locked loops with one-sided bandwidths of 1.5 Hz were successfully used to track Doppler rates in excess of 2 Hz/sec with a resultant phase error due to dynamics of less than 0.5 degree. The type III loops have no steady state phase error due to frequency rate (acceleration), and the error due to jerk (the derivative of acceleration) is proportional to the jerk times $(1/B_L)^3$. At Uranus encounter, the maximum predicted steady state phase error due to jerk is less than 0.2 degrees with a 1.5 Hz type III loop. Thus the actual steady state phase error was dominated by the phase detector bias, discussed in the preceding section. A Block IV receiver, operating at minimum bandwidth of $2B_{LO} = 10$ Hz, would have an actual one-sided loop bandwidth of 18 Hz, a static phase error 1.5 degrees at 2 Hz/sec Doppler rate, and a loop SNR of 11 dB. The loop SNR with the ARX operating with a 1.5 Hz loop is 22 dB. Thus the Advanced Receiver achieves a significant increase in loop SNR of about 11 dB.

At Uranus encounter, the ARX also achieved subcarrier lock and symbol synchronization, and produced estimates of symbol SNR. The tracked data rates varied from 25.6 kbps with E_s/N_0 of -7.2 dB to 14.4 kbps with E_s/N_0 of -4.4 dB. In all cases the modulation index was known, so that the relationship between P_c/N_0 was also known. Our estimates of P_c/N_0 and E_s/N_0 were consistent with this relationship to within 0.1 dB. Considering possible uncertainties in modulation index and losses in the symbol and subcarrier loops, our measurements indicate correct performance of the subcarrier demodulator, the symbol synchronizer, and the SNR estimator.

VIII. Possibilities for Future Improvement

Testing of the breadboard ARX and continuing analysis and research has highlighted some areas in which the performance of the receiver could be enhanced.

A. Offset Carrier

The ARX bias problem can be handled in several ways. One way would be to reduce the magnitude of the spurious frequency component at one quarter of the sampling rate by improving the design of the A/D unit, further isolating the sampling clock from the signal path. Though this may be technically possible, the wisdom of such an approach is not clear. One of the traditional problems with analog phase locked loops at low carrier power to noise power ratios is a lack of isolation between the input and reference signals. The only source of in-band spurious components in the ARX digital loop is at the A/D converter. Hence if we can move this component out of band, we have effectively removed the interference without having to increase the analog isolation circuitry.

The problem of generating spurious energy at the carrier frequency can be avoided by offsetting the sampling clock from four times the carrier IF. By offsetting, the sampling clock's subharmonic is moved away from the carrier frequency which will help to assure a high level of isolation in the feedback path. This offset should be selectable, to avoid the possibility of the subcarrier or data being corrupted if the sampling subharmonic happens to fall in band. The main disadvantage to this technique is that demodulation now requires actual complex multiplication at the sampling rate, but this is feasible with currently available VLSI chips.

B. Fixed Sampling Rate

To eliminate jitter in the carrier phase locked loop introduced by insufficient compensation for symbol loop coupling effects in the sampling clock, it is recommended that the sampling rate be fixed and not depend on the symbol loop. This will necessitate the redesign and new analysis of the symbol loop. There will be some loss in performance because there will be a noninteger number of samples per symbol. This loss will be negligible except at very high data rates, which only occur with direct carrier modulation types. The impact of effect at high rates is currently under study.

C. Subcarrier Windowing

Recent results [11] indicate that substantial improvements can be made in subcarrier tracking by windowing the subcarrier reference signal, in a manner similar to windows now used in the ARX for the symbol synchronization loop. Since the cost to do this is minimal and implementation is straightforward, it is suggested that this be done in future systems.

D. Loop Filters

Substantial work has been done recently in loop filter design [2, 5, 8, 9, 12]. Some benefit versus cost tradeoffs need to be done, but changing the form of the loop filters should be considered. The main potential benefits are for wide loop bandwidths, i.e., when the required loop bandwidth approaches the update rate of the loop filter.

E. Smoothing Estimators

Smoothing has been proposed as a method of improving carrier phase estimation [4, 5, 13, 14]. A 5.0 dB to 5.6 dB reduction in carrier phase tracking error can be achieved without narrowing the bandwidth of the phase locked loop. This is very important when the signal is weak and the loop bandwidth cannot be narrowed due to spacecraft Earth dynamics or system instabilities. This situation occurs when using small antennas in an array, or for weak spacecraft like Pioneer 10. Smoothing virtually eliminates radio loss whenever the phase locked loop can maintain lock.

F. Doppler Extractor

In anticipation of requirements for ARX DSN implementation, a digital Doppler extractor will be designed. This will take integrated uplink phase from the exciter and compare it to integrated downlink phase from the ARX to produce an estimate of two-way Doppler. These computations can be performed by the ARX signal processing assembly.

IX. Conclusions

A breadboard Advanced Receiver (ARX) has been built and demonstrated in the laboratory and in the field. It performs carrier tracking, subcarrier tracking, symbol synchronization, and data detection with improved performance over current DSN subsystems. Advanced features include FFT based fast acquisition, sideband aiding, and increased reliability to serve the flight projects of the 1990's.

Acknowledgments

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**Table 1. Lab tracking performance test with $f = 1$ Hz/sec,
 $E_s/N_0 = -10$ dB, $P_c/N_0 = 26.6$ dB-Hz**

Loop bandwidth B_L (Hz)	Loop type	Steady state phase error ϕ_{ss} (deg)	Phase error jitter σ_ϕ (deg)	Loop SNR _L ρ (dB)
10	II	-1.2	8.5	16.6
3	II	-13.5	4.7	21.8
3	III	0	4.7	21.8
1	III	0	2.7	26.6

**Table 2. Swept acquisition test with $B_{LC} = 10$ Hz
 $P_c/N_0 = 23$ dB-Hz**

Loop type	Loop parameters		Sweep rate (Hz/s)	Theoretic probability of acquisition	Experimental probability of acquisition
	r	k			
II	2	0	30.4	0.92	0.95
II	4	0	24.8	0.87	0.88
III	4	0.25	20.8	0.82	0.42

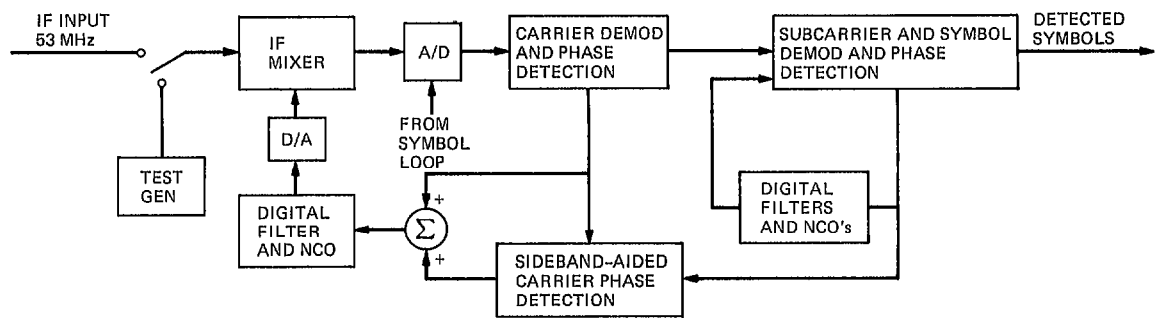


Fig. 1. ARX functional block diagram

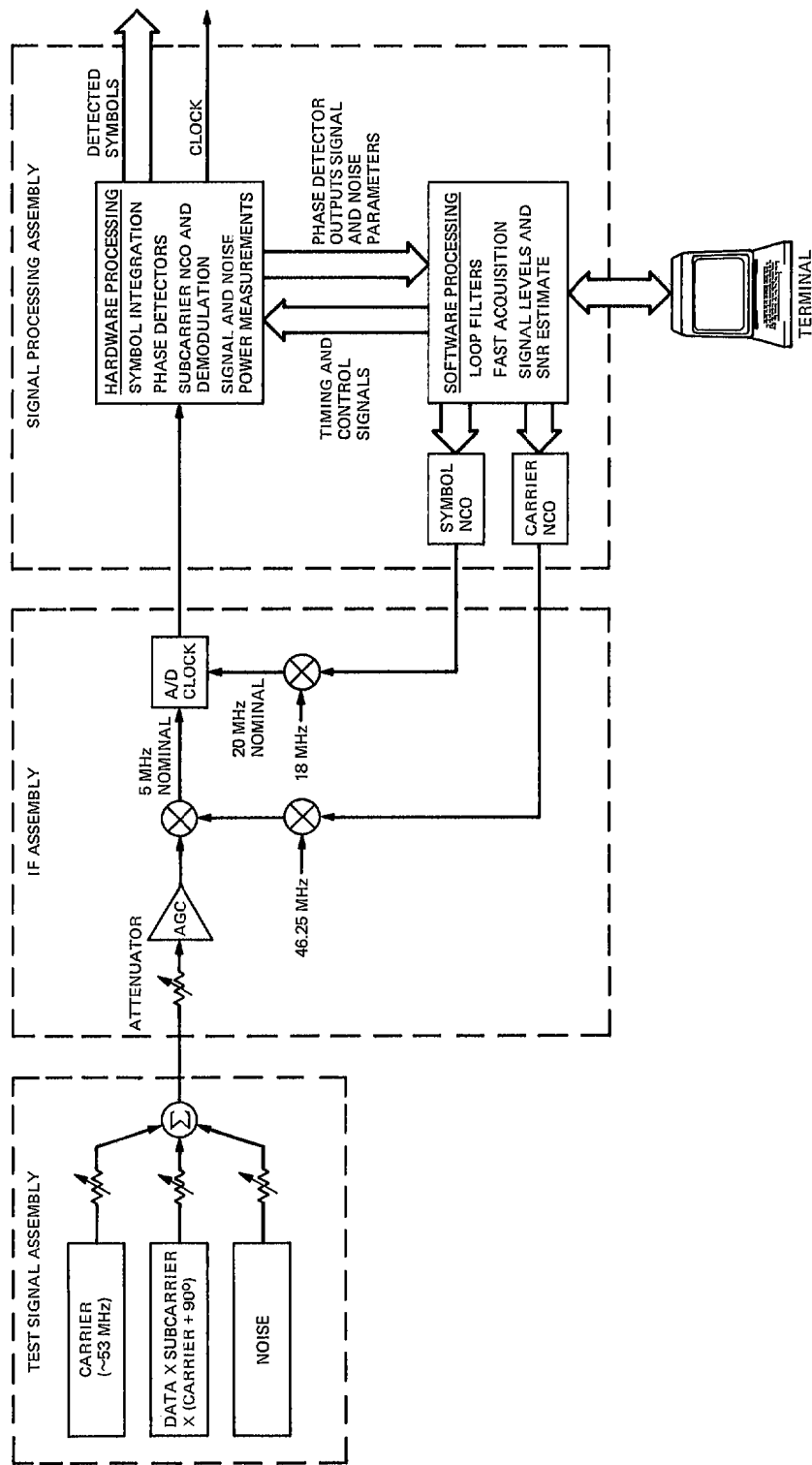


Fig. 2. ARX system block diagram

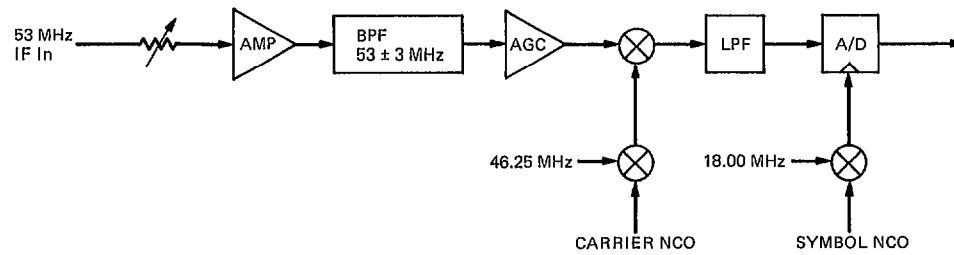


Fig. 3. ARX IF assembly

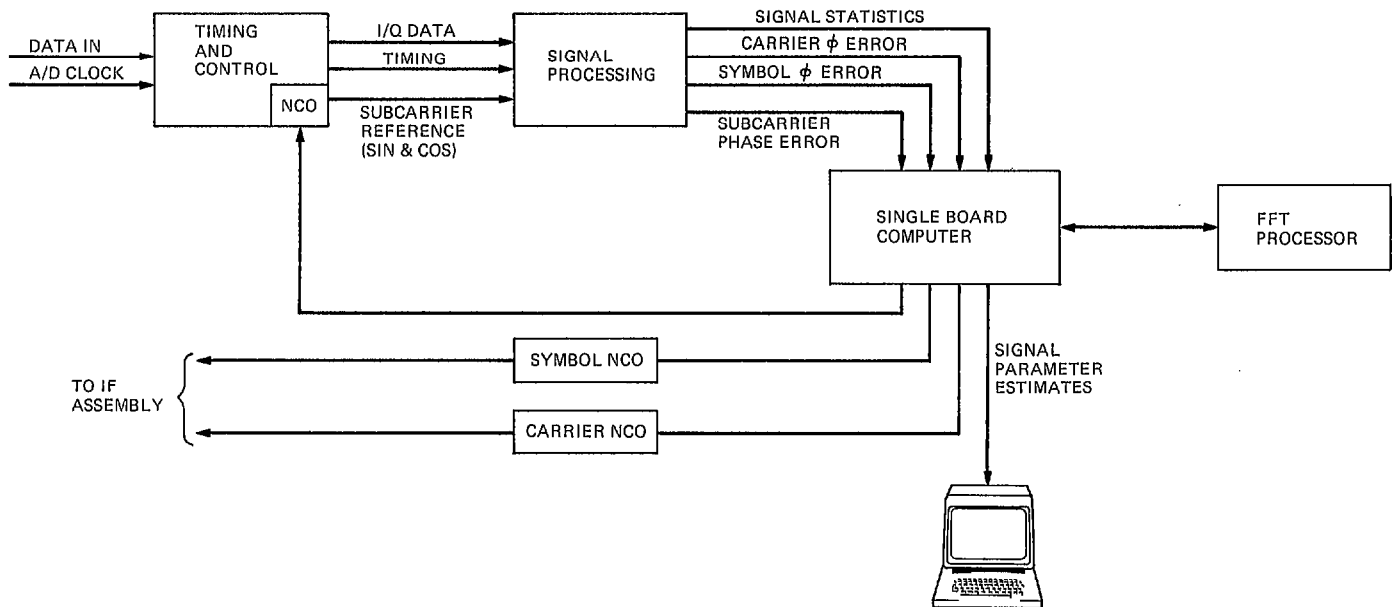


Fig. 4. ARX signal processing assembly

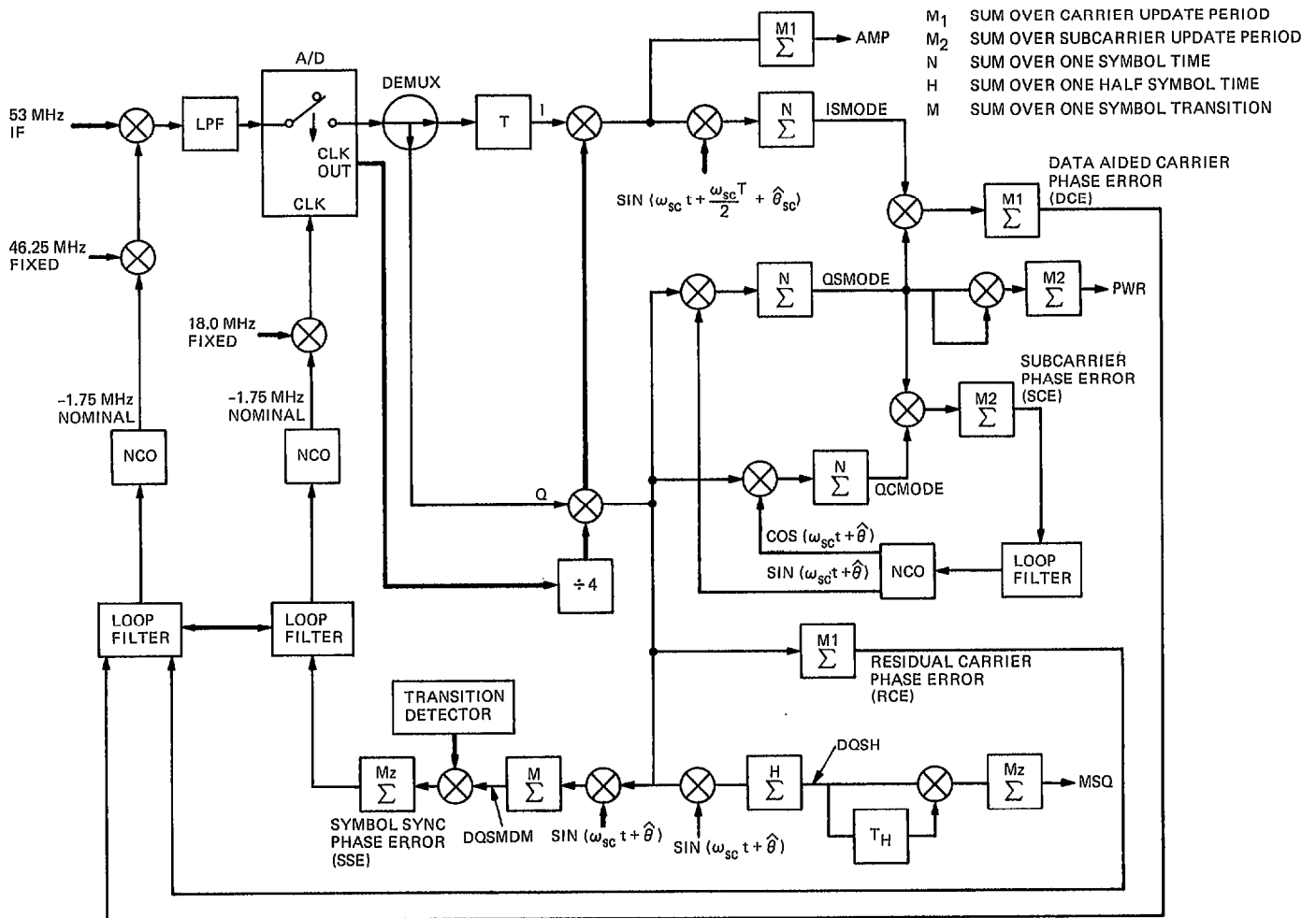


Fig. 5. ARX signal processing diagram

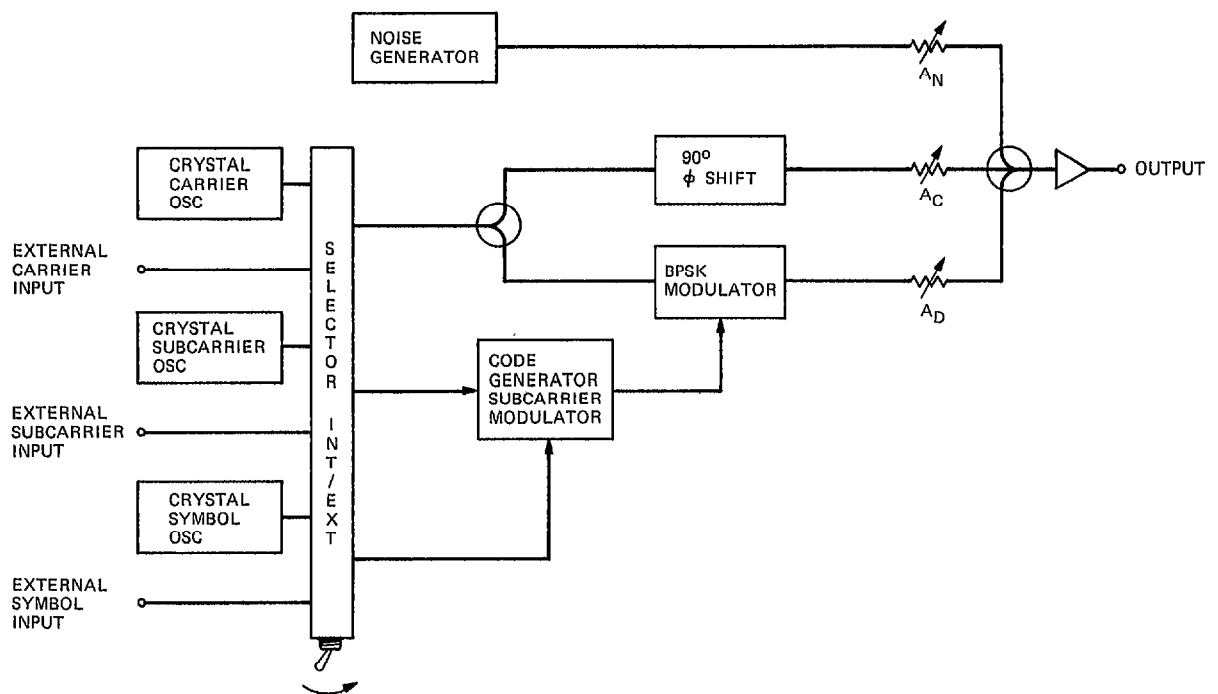


Fig. 6. ARX test signal assembly

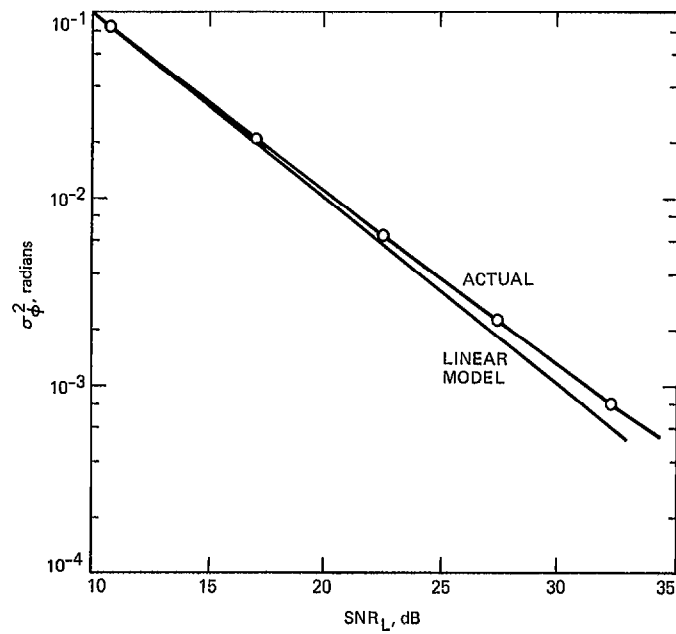


Fig. 7. Linear and actual phase error variances as a function of SNR_L