An Electronically Tuned, Stable 8415-MHz Dielectric Resonator FET Oscillator for Space Applications

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A voltage-controlled 8415-MHz FET oscillator stabilized by a dielectric resonator is described. The oscillator provides a linear electronic tuning range of over 3.2 MHz with a flat power output equal to +1.8 dBm (27°C nominal), a single-sideband noise to carrier ratio of -68 dBc/Hz at 1 kHz off carrier, and a frequency temperature coefficient of 0.54 part per million/°C over a -24°C to 75°C range. The oscillator withstood 150 krads (Si) of gamma radiation with no significant performance degradation. The overall performance of the FET oscillator is in many ways far superior to that of an equivalent bipolar oscillator for space applications.

I. Introduction

An 8415-MHz FET oscillator was developed for application as a phase-locked oscillator in a transponder for a spacecraft-based system, the NASA standard X-band transponder. The advantages of this system were reduced size and complexity due to the elimination of multiplier chains; excellent frequency stability; electronic tunability over a large bandwidth; simplicity of temperature compensation; and low power consumption.

This article describes a high stability voltage-controlled FET oscillator that includes an amplifier connected in a feedback loop with a temperature-stabilized dielectric resonator. The oscillator configuration [1]–[4] and design were optimized to meet the design goals. A detailed comparison of FET oscillator performance against that of a bipolar oscillator is given [5], [6]. This technology development was successfully transferred to a telecommunications equipment contractor. A summary of this technology transfer effort is given in Section V.

II. FET Oscillator Design and Performance

The block diagram of the FET dielectric resonator oscillator (FET DRO) [1]–[3] is illustrated in Fig. 1. A photograph of this oscillator is shown in Fig. 2. The oscillator consists of a single-stage FET (Mitsubishi MGF 1402) amplifier of 11.6 dB gain, a 10-dB coupler, and a dielectric resonator on a 1.65-mm quartz spacer in the amplifier drain-to-gate shunt feedback loop. The dielectric resonator is made of barium tetratitanate of dielectric constant k = 38.6, and its unloaded Q is equal to 4800 at 8400 MHz. The resonator has a temperature coefficient of +3.5 ppm/°C. One part of the coupler supplies the output signal, while the other supplies the signal to the feedback loop. The insertion loss of the feedback loop, including the resonator and the coupler, is about 7.8 dB. The loop has an excess gain of 3.8 dB. A hyperabrupt silicon tuning varactor (Metallics MMD830-P55) at the end of a quarter-wavelength open stub is used to tune the circuit. The resonator coupling and open-stub line lengths are adjusted to provide an electronic tuning of 3.4 MHz. The measured loaded Q (Q_L) is

approximately equal to 2700. Further reduction in the loaded Q will increase the tuning range but will degrade the phase noise of the oscillator. The circuit is etched on a 0.635-mm alumina substrate that is solder attached to a plated titanium base plate of a thickness equal to 0.89 mm. The circuit is enclosed in a rectangular box as shown in Fig. 2. The dimensions of the box are 51.8 X 40.4 X 26.9 mm and can be reduced to 38.1 X 38.1 X 20.3 mm. The FET DRO is mechanically tuned between 8412 MHz and 8490 MHz with a metal disc tuner over the dielectric resonator, and can be set within ±2 kHz.

The electronic tuning characteristics of the FET DRO are illustrated in Fig. 3. The electronic tuning range at any temperature setting within the designed temperature range from -20°C to +75°C is greater than 3.2 MHz (measurements were made at -24°C, 0°C, +27°C, +52°C, and +75°C). The varactor bias (frequency control voltage, V_{FC}) voltage range is from 0 to +15 V. The selected value for the nominal frequency control voltage was equal to 8 V. The tuning is quasi-linear, and its deviation from the best straight line fit over the 3.2-MHz tuning range is within ±14 percent. The nominal power output at room temperature (27°C) is +1.8 dBm, with a maximum power variation of ±0.3 dB over the tuning range.

The FET DRO was tested for the temperature dependence of oscillator frequency and power. The results, as shown in Fig. 4, indicate less than a 1-MHz peak-to-peak frequency drift and less than a +2.1 ppm/°C peak-to-peak temperature coefficient over the measured temperature range. The average temperature coefficient over the temperature range is less than +0.54 ppm/°C. The peak-to-peak power variation over the temperature range is less than 0.9 dB, and the total peak-to-peak power variation over the temperature range, including 0.5 dB maximum power variation over the 3.2-MHz tuning range, is less than 1.5 dB. The single-sideband (SSB) phase noise density levels measured at different temperature settings and at different tuning bias levels [4] were found to be within the range of -66 to -69 dBc/Hz at a 1-kHz offset from the carrier. These results meet the specified design requirements (Table 2) for application in a spacecraft transponder.

III. Bipolar (BJT) Oscillator Design and Performance

The purpose of this design study was to compare the performance of the bipolar dielectric resonator oscillator against that of the FET oscillator for a spacecraft transponder application. The bipolar dielectric resonator oscillator (bipolar DRO) [5], [6] is designed as a negative resistance oscillator. The basic breadboard oscillator layout and component locations on an alumina substrate are shown in Fig. 5. The NPN bipolar transistor (NE64587) used for this application is packaged in a common collector configuration to facilitate heat transfer from the transistor chip to the heat sink by solder attachment of the transistor package directly to the heat sink. The stabilizing dielectric resonator is the same as that used in the FET oscillator circuit. The dielectric resonator mounted to a 1.65-mm quartz spacer is coupled to the base microstrip line by placing it at about one-quarter wavelength away from the transistor base terminal. The positioning of this dielectric resonator is critical as it determines the cavity-loaded Q, electronic tuning range, phase noise, and power output characteristics. Electronic tuning of the bipolar DRO oscillator is accomplished by means of simple bias tuning, to vary the transistor base–collector capacitance. The transistor biasing network is illustrated in Fig. 6.

The electronic tuning characteristics shown in Fig. 7 were obtained by adjusting the dielectric resonator position to provide about 3.5 MHz of linear electronic tuning (125 kHz/V) over the frequency control base voltage (V_{FC}) range of -20 V to +8 V. The electronic tuning deviation from the best straight line fit over this 3.5-MHz tuning range is less than ±3 percent. The measured loaded Q is approximately equal to 600. Output power variation over the electronic tuning range was less than 0.8 dB. The power output is equal to -3.8 dBm at V_{FC} = 0 V and at a temperature of 25°C. The measured SSB phase noise is less than -70 dBc/Hz at a 1-kHz offset from the carrier in a 1-Hz bandwidth at any temperature setting (-25°C to to +72°C) and electronic tuning bias level. The measured temperature performance of the bipolar oscillator with a temperature-compensated (T_{cf} = +3.5 ppm/°C) dielectric resonator is illustrated in Fig. 8. The frequency temperature stability is better than -2.4 ppm/°C over -25°C to +72°C. However, the power output of the oscillator varied by about 6 dB over the full temperature range, which can be flattened by employing buffer amplifiers. The main reason the bipolar DRO was not pursued further for a spacecraft transponder application was its large power consumption (750 mW vs. 90 mW for a FET). However, the bipolar DRO is ideally suited for applications where low phase noise design is most important.

IV. Performance Comparison of FET and Bipolar Oscillators

In this section, a comparison of the FET DRO and the bipolar DRO for similar output frequency (8400- to 8500-MHz) and electronic tuning bandwidth (3-MHz) requirements is presented. Oscillator circuit configurations and devices are compared in Table 1. Both of these circuits use a stabilizing dielectric resonator. The bipolar DRO is a low Q (Q_L = 600) negative resistance oscillator, whereas the FET DRO is a high Q (Q_L = 2700) shunt feedback oscillator. In the case of the bipolar DRO, it was necessary to lower the Q_L to 600 to ob-

tain the required 3.2-MHz linear electronic tuning, which in effect increased the phase noise. However, the measured phase noise of the bipolar DRO is about 5 dB lower than that of the FET DRO. This is a direct consequence of a lower $1/f$ noise corner frequency [1] for the bipolar device [5]. The $1/f$ noise corner frequency for the bipolar transistor [5] is approximately equal to 6.3 kHz, whereas that for the FET device [7] is 700 kHz. The bipolar oscillator is bias tuned by tuning the transistor collector–base junction capacitance. The FET DRO is tuned by applying voltage across a silicon tuning diode whose shunting capacitance is electromagnetically coupled into the resonator fields.

A complete list of the X-band (8415-MHz) DRO design goals attempted, along with the results achieved by the bipolar and FET oscillators, is compiled in Table 2. The goals for the mechanical frequency setting (8400 to 8500 MHz ±5 kHz), electronic frequency tuning range (3 MHz), tuning linearity (±15 percent), and frequency pulling (<100 kHz for 1.5:1 VSWR load) have all been met or exceeded. The frequency temperature stability goal is <2 ppm/°C. The dielectric resonator used in these oscillators has a temperature coefficient of +3.5 ppm/°C. The measured average values of frequency temperature stability over the -20°C to +75°C range for FET and bipolar oscillators are 0.54 ppm/°C and -2.4 ppm/°C, respectively. Further temperature compensation is necessary for the bipolar oscillator. Nonharmonic spurious signals are less than -60 dBc for both oscillators. All spurious signals are less than -77 dBc for the FET oscillator. The bipolar oscillator has a second harmonic level of -16 dBc at its output and can be reduced to the goal requirement of less than -40 dBc by a buffer amplifier and a filter. The bipolar oscillator generates a power level equal to -3.8 dBm at its emitter output. It requires a buffer amplifier to increase its power output to the 0-dBm goal requirement level and to flatten the power variation to the ±1-dB goal over the tuning bandwidth and temperature ranges. The FET oscillator meets the power output and power flatness requirements without a buffer amplifier, thus saving the additional power consumption and volume that would be required by the amplifying circuits.

These oscillators were exposed to cobalt-60 gamma radiation at a level of 150 krads (Si), and the effects of radiation on the oscillators were studied. The overall results for these oscillators indicate insignificant change in the measured parameters such as frequency, power, phase noise, bias current, and tuning characteristics.

The four main trade-off concerns between these oscillators are (1) power consumption; (2) phase noise; (3) linear tuning bandwidth; and (4) power flatness. The bipolar oscillator requires a maximum of 750 mW of dc power and operates at an efficiency of about 0.07 percent. The FET oscillator has better efficiency (1.5 percent) and requires less than 90 mW of dc power (88 percent lower than the bipolar DRO) over the required 3-MHz electronic tuning range. The single-sideband (SSB) phase noise that can be achieved for bipolar and FET oscillators is between -69 and -75 dBc/Hz and -66 to -69 dBc/Hz at 1 kHz from the carrier, respectively. Lower SSB phase noise values are possible by reducing the electronic tuning range. For a given tuning bandwidth the bipolar DRO provides lower (by 5 dB or more) phase noise characteristics than the FET DRO.

V. Summary of the Dielectric Resonator Oscillator (DRO) Technology Transfer Effort

The DRO technology discussed in the previous sections was transferred to the NASA X-band (8415-MHz) transponder contractor for implementation into the transponder design receiver local oscillator phase-locked loop (7459 MHz) and the exciter downlink oscillator phase-locked loop (8415 MHz). The contractor-fabricated engineering model local oscillator FET DRO (7459 MHz) is shown in Fig. 9. The circuit is etched on a 0.635-mm-thick alumina substrate that is solder attached to a plated molybdenum base plate of a thickness equal to 0.635 mm. The circuit is enclosed in a rectangular (aluminum) box of dimensions 30.5 × 38.1 × 13.7 mm. The selected FET for this application is a high gain (12-dB) FET (Mitsubishi MGF 1402) with a low $1/f$ noise corner frequency (700 kHz) [7]. The circuit is designed as a series-feedback negative resistance oscillator [1], [3]. The length of the 37-ohm shorted stub attached to the FET source lead and the length of the 37-ohm transmission line between the drain lead and the 50-ohm output line are optimized for a maximum reflection coefficient (at 7459 MHz) at the gate. The gate is conjugately matched with the equivalent resonant circuit model of the dielectric resonator coupled to the 50-ohm line attached to the gate. The position and the spacing of the dielectric resonator relative to the gate transmission line are adjusted for the conjugate match with a zero-degree phase shift at the dielectric resonator reference plane at the operating frequency. The dielectric resonator mounted on a 2.5-mm-high quartz spacer is electromagnetically coupled to the gate line at a distance of 5.4 mm from the gate (see Fig. 9). The circuit is tuned by a hyperabrupt silicon tuning diode (Alpha DKV6550C-304-001) attached to a quarter-wavelength 50-ohm open stub line. The open stub is electromagnetically coupled to the dielectric resonator. The circuit layout also consists of a 50-ohm quarter-wavelength trap at 6 GHz with a 100-ohm series resistance attached to the drain circuit to suppress spurious oscillations at around 6 GHz.

The adhesive used between the dielectric resonator and the quartz spacer, as well as between the spacer and the alumina, is

Ablebond 293-1. Five adhesive materials were evaluated for their dielectric constant, outgassing, peel strength, and cure cycle. The adhesive trade-off summary is tabulated in Table 3. Of these, two adhesive materials—Ablebond 293-1, with a high peel strength equal to 3.88 kg, and Solithane 113-300, with a low peel strength equal to 0.68 kg—were further evaluated by measuring in a test fixture the temperature-induced shift in the resonant frequency of the adhesive-mounted dielectric resonator of temperature coefficient 0 ppm/°C. The shift in the resonant frequency of the resonator over the qualification temperature range of −20°C to +75°C for Solithane 113-300 adhesive was 910 kHz, while that for Ablebond 293-1 was 630 kHz. The performance of the adhesive Ablebond 293-1 is clearly superior in terms of its high peel strength and low temperature-induced frequency drift. Ablebond 293-1 was the adhesive selected for the engineering model FET DRO.

The electrical frequency tuning vs. temperature performance characteristics of the 7459-MHz FET DRO (Fig. 9) are shown in Fig. 10. A bias tuning range of 6.5 V (nominal) ±6 V provided a tuning capability of ±1.8 MHz minimum over the hardware qualification temperature range of −20°C to +75°C, with a tuning linearity of less than ±10 percent. The oscillator results show an overall frequency temperature slope of +3.7 ppm/°C. This frequency drift can be further compensated by using a dielectric resonator of a thermal coefficient approximately equal to −3.7 ppm/°C. The RF power output variations with tuning voltage and temperature are shown in Fig. 11. The nominal RF power output level at a +6.5-V tuning voltage and at 25°C is +4.23 dBm. The maximum power variation from the nominal power level is ±0.5 dB over the tuning voltage and qualification temperature ranges. The measured single sideband phase noise at a 1-kHz offset from the carrier was less than −60 dBc/Hz. The output of the oscillator has a second harmonic signal level of −25 dBc and a nonharmonic spurious signal level of −2 dBc at 11,896 MHz. These spurious signals require further filtering to satisfy the requirements of −40 dBc for harmonic signals and −65 dBc for nonharmonic spurious signals.

VI. Conclusions

The FET DRO is more efficient and consumes considerably less dc power than the bipolar DRO. Measured SSB phase noise data confirm that the bipolar's performance is clearly superior to that of the FET oscillator, being about 5 dB lower in phase noise for frequency offsets of 100 Hz to 1 kHz from the carrier. For space applications, the FET DRO is preferred to the bipolar DRO because of its lower dc power consumption, better thermal frequency stability, linear electronic tunability, and higher RF output power capability. The technology transfer to industry was satisfactorily accomplished.

This article summarized the performance characteristics and demonstrated the feasibility of X-band (8415-MHz) dielectric resonator oscillators for space communication applications. Trade-offs between FET and bipolar oscillators have been identified and characterized.

Acknowledgments

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Table 1. Active device and dielectric resonator oscillator circuit comparisons

Parameter	FET DRO	Bipolar DRO
Nominal frequency	8415 MHz	8415 MHz
Active device	MGF 1402-01 Gate length = 0.8 μm Gate width = 400 μm	NEC 64587
Circuit configuration	Shunt feedback	Negative resistance
$1/f$ noise corner frequency (f_c)	>700 kHz	6.3 kHz
Device noise figure	2.5 dB	5.2 dB
Resonator type	Transtech D8512 (+3.5 ppm/°C) barium tetratitanate Q_0 = 4800 at 8400 MHz	Transtech D8512 (+3.5 ppm/°C) barium tetratitanate Q_0 = 4800 at 8400 MHz
Spacer	Quartz, spacer 1.65 mm	Quartz, spacer 1.65 mm
Cavity Q_L	2700 mm	600 mm
Tuning device	Hyper-abrupt silicon diode MMD 830-P55	Bipolar transistor base–collector junction capacitance is bias tuned
Mechanical dimensions	51.8 x 40.4 x 26.9 mm	47 x 31.8 x 24.1 mm

Table 2. Comparison of FET and bipolar dielectric resonator oscillators

Parameter	Specifications	Measured performance	
		FET DRO	Bipolar DRO
Mechanical tunability	8400–8500 MHz ±5 kHz	8412–8490 MHz ±2 kHz	8387–8601 MHz ±2 kHz
Electrical tunability	±1.6 MHz about f_0	±1.70 MHz (linear)	±1.75 MHz (linear)
Frequency tuning linearity	±15% to BSL	±14%	±3%
Output power*	0 ± 1 dBm −20°C to +75°C	+1.5 to +2.4 dBm	+0.8 to −4.7 dBm
Power flatness vs. tuning*	±0.5 dB	±0.3 dB	±0.5 dB
Power flatness vs. temperature*	±0.5 dB −20°C to +75°C	±0.5 dB	±3 dB
Total output power variation over both temperature range and maximum tuning range*	±1 dB −20°C to +70°C	±0.75 dB	±4.5 dB†
Frequency stability vs. temperature	2 ppm/°C between −20 and +75°C	+0.54 ppm/°C (average)	−2.4 ppm/°C
SSB phase noise at 1 kHz from carrier	−60 dBc/Hz	−66 to −69 dBc/Hz	−69 to −75 dBc/Hz
Harmonics	−40 dBc	−77 dBc	−16 dBc
Nonharmonic spurious	−65 dBc	−77 dBc	−68 dBc
Frequency pulling	100 kHz for 1.5:1 VSWR all phase load	<26 kHz	11 kHz
Frequency pushing ±1% supply voltage variation (gate and/or drain voltage)	<100 kHz	<25 kHz	<17 kHz
Frequency control terminal impedance	>2 kohms	1500 kohms	15.24 kohms
Power consumption*	<200 mW	90 mW	750 mW
Operating voltage	<±28 V	+4 and −2 V	−14 V ± 1%
Tuning voltage*	<±15 V	0 to −15 V	−15 to +8 V
Output impedance	50 ± 5 ohms	50 ± 5 ohms	50 ± 5 ohms
Efficiency*	>0.5%	1.5%	0.07%
Cold and hot turn-on at any temperature	OK	OK	OK
Radiation immunity*	150 krads (Si)	No performance degradation	No performance degradation

*Goals.
†Unbuffered output.

Table 3. Dielectric resonator oscillator adhesive trade-off summary

Material	Dielectric constant	Outgassing	Peel strength, kg		Cure	Form
			Unetched	Etched		
Epon 838/V125	2.95–3.85 @ 1 MHz, 25°C (estimated)	0.51–1.65% TML* 0.12–0.77% VCM† (est. range)	1.61	0.57	24 hours at 21°C or 2 hours at 66°C	Premixed frozen in syringe (epoxy)
Scotchweld 2216 Gary	5.51 @ 1 kHz, 24°C	0.82% TML 0.06% VCM	1.75	0.68	24–48 hours at 25°C or 2 hours at 66°C	2-part mix at 25°C (epoxy)
Solithane 113-300	3.4 @ 10 MHz, 27°C	0.50% TML 0.02% VCM (estimated)	0.68	1.34	48 hours at 25°C or 3 hours at 66°C	Premixed frozen in syringe (urethane)
Sigma Plastronics #1 typ II 1:1 ratio	2.7 @ 8000 MHz, 25°C	0.64% TML 0.01% VCM	1.11	1.59	8–10 hours at 25°C or 3 hours at 66°C	2-part mix at 25°C (epoxy)
Ablebond 293-1	3.6–4.0 @ 1 kHz, 25°C	1.32% TML 0.08% VCM	3.88	3.31	24 hours at 60°C or 4 hours at 75°C	Premixed frozen in syringe (epoxy)

*TML = total mass loss.
†VCM = volatile condensable material.

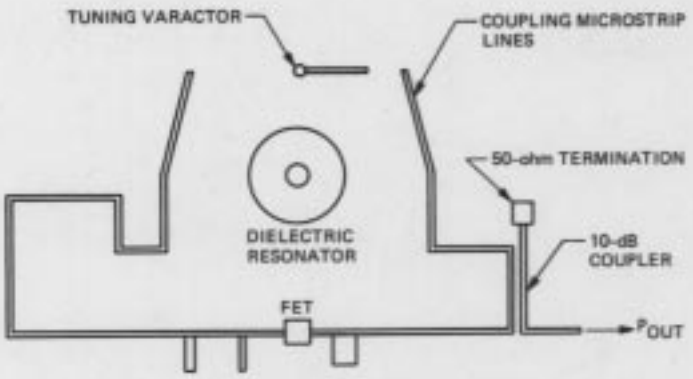

Fig. 1. Block diagram of the FET dielectric resonator oscillator

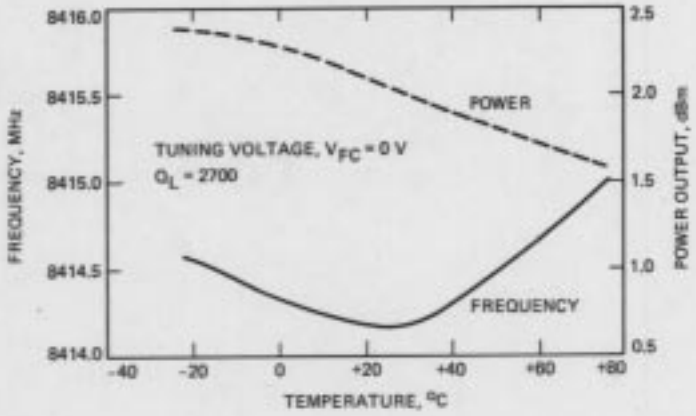

Fig. 4. FET DRO temperature performance characteristics

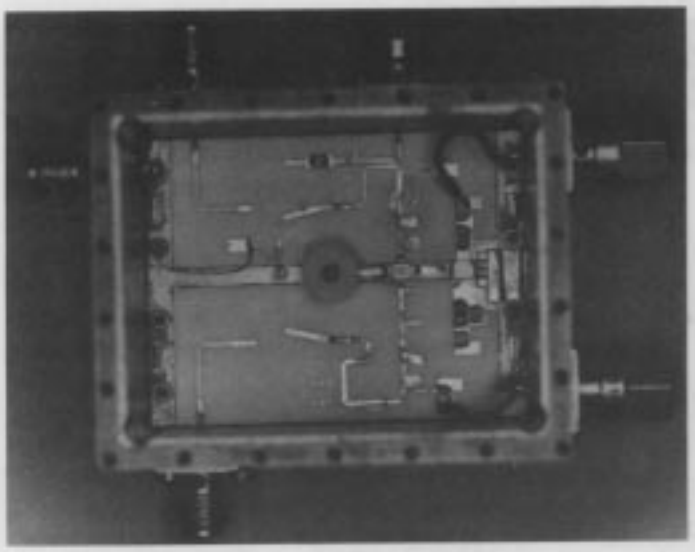

Fig. 2. FET dielectric resonator oscillator assembly

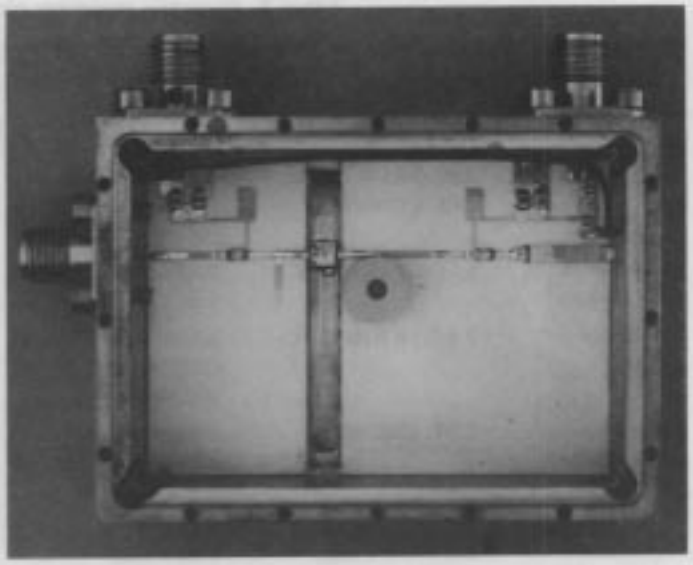

Fig. 5. Bipolar dielectric resonator oscillator assembly

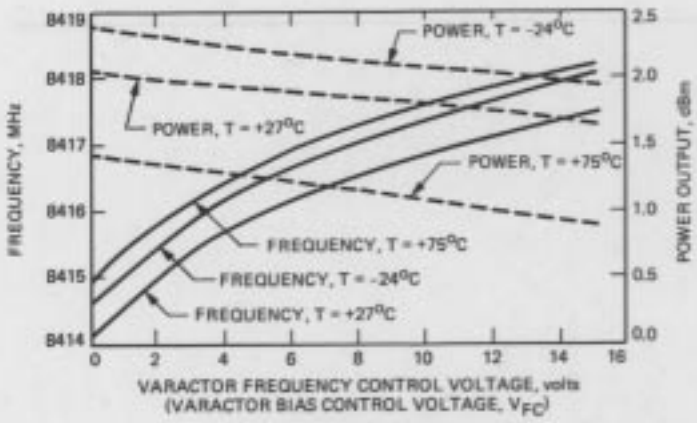

Fig. 3. FET DRO electronic tuning characteristics

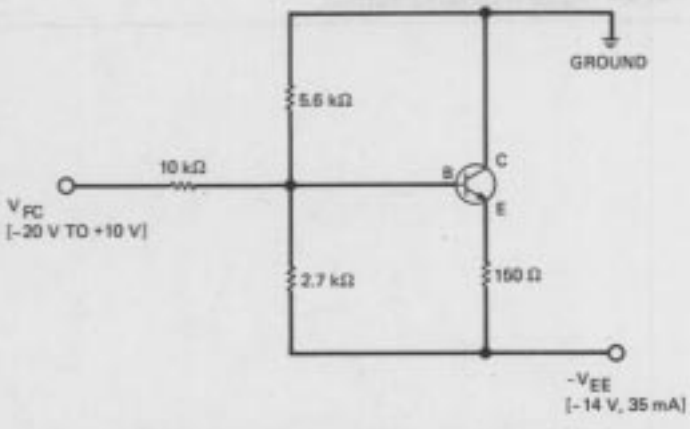

Fig. 6. Bipolar transistor DC biasing circuit for linear electronic tuning

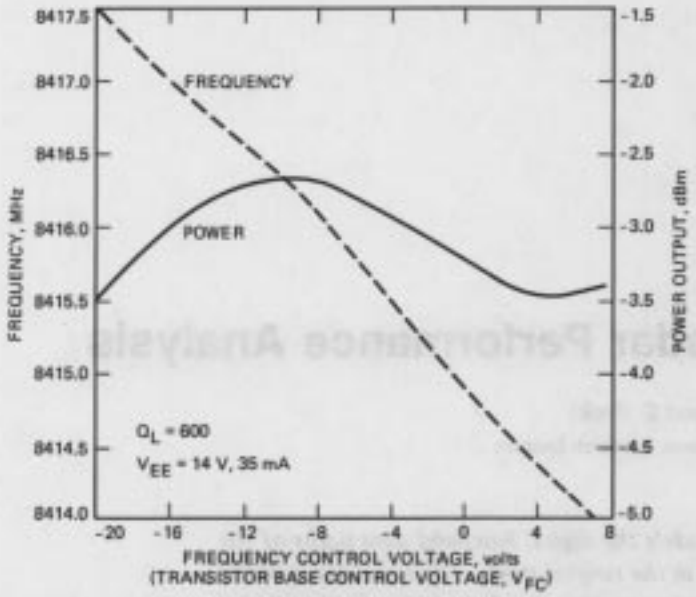

Fig. 7. Bipolar DRO electronic tuning characteristics

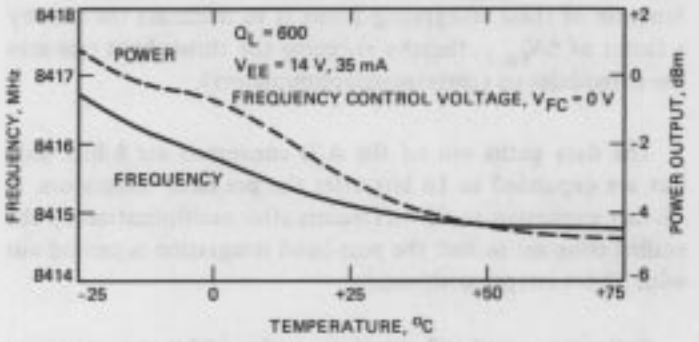

Fig. 8. Bipolar DRO temperature performance characteristics

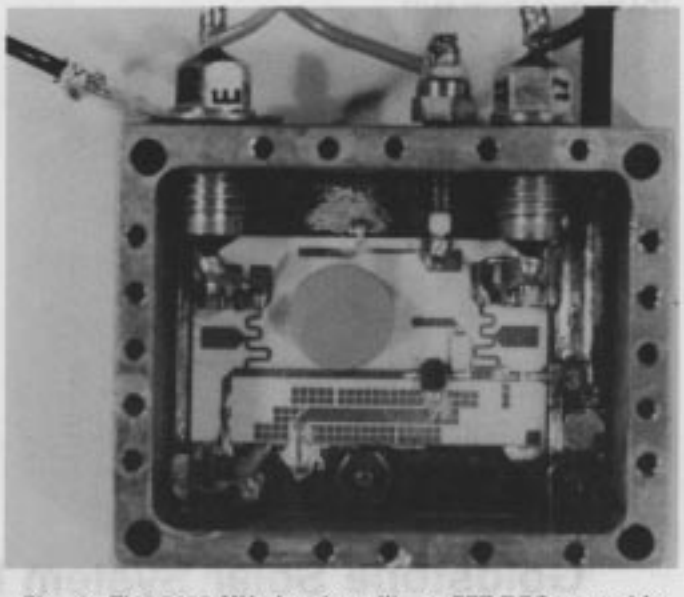

Fig. 9. The 7459-MHz local oscillator FET DRO assembly

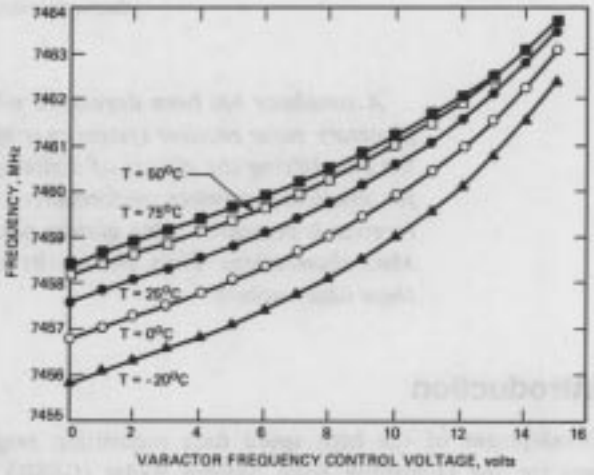

Fig. 10. The 7459-MHz local oscillator FET DRO electronic tuning characteristics

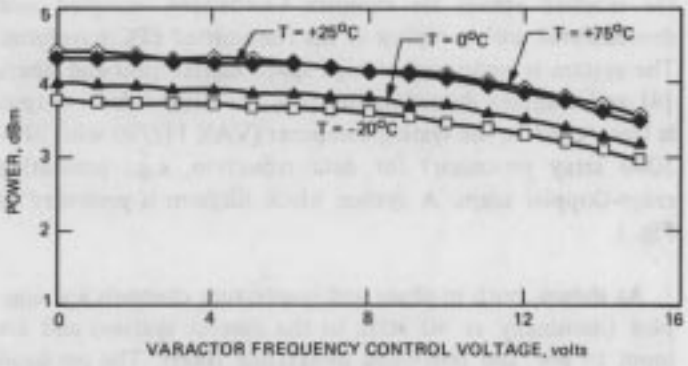

Fig. 11. The 7459-MHz local oscillator FET DRO output power vs. tuning voltage and temperature