Goldstone Solar System Radar Performance Analysis

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A simulator has been developed which models the digital baseband data paths of the planetary radar receiver system as configured in the ranging mode. The simulator is useful for quantifying the effects of digital quantization errors on radar receiver sensitivity and for predicting receiver performance. In this article, a performance analysis of the radar receiver is presented using system parameters that correspond to those for the upcoming Mars observations. Thus, the results provide an assessment of anticipated data quality for these observations.

I. Introduction

Development of the high speed data acquisition ranging system for the Goldstone Solar System Radar (GSSR) has been reported in a series of articles over the past several years [1]–[4]. For range-Doppler mapping applications, the system utilizes a binary phase-coded (BPC) transmitted waveform and the received echoes are complex basebanded, sampled, and demodulated with a replica of the transmitted BPC waveform. The system is composed of high speed digital front end filters [4] and complex demodulators [3]. The demodulator output is transferred to the system computer (VAX 11/780 with FPS-5000 array processor) for data reduction, e.g., generating range-Doppler maps. A system block diagram is presented in Fig. 1.

As shown, both in-phase and quadrature channels are sampled (nominally at 40 MHz in the current system) and are input to pre- and post-baud integrating filters. The pre-baud filter integrates 5 input samples per output data sample, and the post-baud filter integrates N_{baud} input samples per output data sample (N_{baud} is a user-specified input parameter). The function of these integrating filters is to decimate the data by a factor of $5N_{baud}$, thereby reducing the throughput rate into the demodulators (correlators/accumulators).

The data paths out of the A/D converters are 8 bits wide but are expanded to 16 bits after the pre-baud integrators. A further expansion to 32 bits occurs after multiplication by the scaling constant so that the post-baud integration is carried out with 32-bit integer arithmetic.

Following post-baud integration, the 32-bit data are truncated to the N_{bits} most significant bits (N_{bits} is nominally 4 but is treated as an input parameter for our performance analysis calculations). Finally, the truncated data are correlated and accumulated to produce a stream of correlation data which are output to the system computer.

Actually, the above block diagram corresponds to just one of the complex data acquisition channels. Multiple complex

channels are frequently used, e.g., in interferometry mapping of Venus. Thus, the performance analysis presented in this article is limited to monostatic, single polarization measurements which utilize only a single complex channel. Nevertheless, these results are indicative of trends in multi-channel system performance as a function of the various input system parameters.

II. System Overview

The basic function of the system (prior to the computer) is to correlate the received echoes with a replica of the transmitted BPC waveform:

$$\phi(\tau) = \int_0^T x(t)\, BPC(t+\tau)\, dt$$

where $x(t)$ is the received complex data, $BPC(t)$ denotes the BPC waveform which is a periodic binary pseudo-noise (PN) sequence generated by a linear shift register, and T is the period of the BPC waveform:

$$T = \Delta T N_{\text{code}}$$

where N_{code} denotes the PN code period and ΔT denotes the duration of a single code element (baud). The complex input, $x(t)$, is composed of the received (basebanded) signal plus system noise:

$$x(t) = s(t) + n(t)$$

In our systems analysis, we model the received signal as a Doppler-shifted and scaled version of the transmitted BPC waveform:

$$s(t) = A BPC(t)\, e^{j\phi} e^{j\Delta\omega t}$$

where the Doppler offset, $\Delta\omega$, is an input parameter.

In correlating the input data with the transmitted BPC waveform, the digital system hardware computes a maximum of 256 correlation lags (range bins): $\phi(k\Delta T/N_{os})$, $0 \leqslant k \leqslant 255$, where N_{os} represents the number of computed lags per code baud. ($N_{os}\Delta T$ also represents the time interval between data samples in the correlator; note that N_{os} can be controlled by the appropriate choice of N_{baud}.) As discussed in [3], the correlation lags are computed sequentially using a pipeline architecture. After the maximum number of lags (<256) is computed, a new set of correlation lags is computed, thereby generating the two-dimensional array of data:

$$c(i,k) \equiv \phi_i \frac{k\Delta T}{N_{os}}, \qquad 0 \leqslant k \leqslant 255$$

$$i \equiv \text{lag set index} = 0, 1, 2, \ldots$$

In computing the correlation data, lagged products are summed over the entire length of the code. However, this sum is broken down into partial sums of 256 terms corresponding to the maximum register length of the correlators. For PN codes which exceed the register length of the correlators, i.e., when $N_{os}N_{\text{code}} > 256$ (recall that the data samples in the correlators are separated in time by $\Delta T/N_{os}$ seconds, *not* ΔT seconds), sequential lag sets are accumulated:

$$A(i,k) = \sum_{j=1}^{N_{acc}} c(N_{acc}\, i + j, k)$$

where the number of accumulations, N_{acc}, is chosen such that $256\, N_{acc}$ approximately spans the period of the code, i.e., $256\, N_{acc} \approx N_{os}\, N_{\text{code}}$. In this case, the accumulated correlation lag data, $A(i,k)$, is input to the system computer. For short PN codes such that $N_{os}\, N_{\text{code}} < 256$, N_{acc} is set to 1.

The system computer calculates the range-Doppler map data, $RD(n,m)$, by Fourier transforming the lag set data in conjunction with power combining, i.e.,

$$RD(n,m) = \sum_{j=1}^{N_{sa}} |Y_i(n,m)|^2, \qquad 0 \leqslant m \leqslant 255$$

$$-N_{\text{bins}}/2 \leqslant n \leqslant N_{\text{bins}}/2$$

where N_{sa} is the number of spectra accumulated, N_{bins} is the number of Doppler bins, and $Y_i(n,m)$ represents the Fourier transformed correlation data:

$$Y_i(n,m) = \sum_{k=-N_{\text{bins}}/2}^{N_{\text{bins}}/2} A(k + iN_{\text{bins}}, m)\, e^{-2\pi jkn/N_{\text{bins}}}$$

The performance of the system can be conveniently expressed in terms of the output signal-to-noise ratio, SNR_o, which is defined by:

$$SNR_o \equiv \frac{\langle R\rangle_{S+N} - \langle R\rangle_N}{\sqrt{\{\langle (R - \langle R\rangle_N)^2\rangle_N\}}}$$

where $\langle\cdot\rangle_N$ denotes the average background noise level and $\langle\cdot\rangle_{S+N}$ denotes the average signal-plus-noise level. The ratio $PG = SNR_o/SNR_{in}$ is the system processing gain where SNR_{in} denotes the input signal-to-noise ratio (in the front-end low-pass filter bandwidth). The theoretical system processing gain, ignoring quantization and sampling effects, is the product of the coherent and incoherent processing gains:

$$PG = 2BTN_{bins}\sqrt{N_{sa}}$$

where B is the bandwidth of the front-end low-pass filters. The factor $2BTN_{bins}$ represents the coherent processing gain and $\sqrt{N_{sa}}$ is the incoherent gain realized by the power combining [5]. In the next section, we present the results of computer simulations of the digital acquisition system which can be compared directly with the above theoretical results for system processing gain.

III. Simulation Results

In evaluating system performance, we have developed a computer simulation test bed which models the digital high-speed data acquisition system depicted in Fig. 1. The simulator program, written in FORTRAN 77, is portable and has been run with minimal modifications on both the Communications Systems Research Section (Section 331) Radar VAX 11/780 computer (without making use of the FPS 5000 array processor) and Cydrome's new Cydra computer (currently on loan to Section 331). The run times for the Cydra are all approximately 7 times faster than the 11/780 run times, and thus the results presented in this section were obtained with the Cydra computer.

The simulation input parameters, corresponding to the upcoming S-band monostatic BPC Mars experiment, include (1) the system (A/D) sample rate (set at 40 MHz); (2) the bandwidth, B, of the front-end low-pass filters which are modeled as 6th-order digital Butterworth filters (B is set at 6 MHz); (3) the total number of Doppler bins, N_{bins} (set at N_{bins} = 128); (4) the number of spectral power accumulations, N_{sa} (set at either N_{sa} = 1 or 50); (5) the number of accumulations, N_{acc}, used in computing the correlation lags (set at 1); (6) the total number of correlation lags computed per set (255); (7) the number of samples integrated in the post-baud filters (N_{baud} = 24); (8) the number of bits, N_{bits}, used in computing the correlation lags (N_{bits} = 4 will be used in the Mars experiment, but we have also used N_{bits} = 8 in our performance analysis); (9) the PN code baud, ΔT (set at 6 μsec); (10) the signal Doppler offset frequency, $\Delta\omega$ (set at $\Delta\omega$ = 0 Hz); (11) the PN code period, N_{code} (set at N_{code} = 127); (12) the input RMS system noise level (which was set at 1/3 of the full scale A/D voltage); (13) the DC bias offset of the A/D converters (nominally set at 0 but varied in the simulation experiments to measure the impact on system performance); and (14) the input signal-to-noise ratio, SNR_{in} (which was set at either -30 dB or -55 dB to model the range of expected input SNRs for the S-band BPC Mars observations). The above values for the system clock rate, the PN code baud, and the number of post-baud integration samples correspond to N_{os} = 2 computed correlation lags per code baud.

The output from each simulation experiment is a sample range-Doppler map, $RD(n,m)$, as defined above in Section 2, consisting of 2560 data points (128 Doppler bins X 20 range bins). Given this map, sample values for SNR_o are computed and compared against the theoretical limit:

$$SNR_o = SNR_{in}\, 2BTN_{bins}\sqrt{N_{sa}}$$

The first set of simulation experiments consisted of high input SNR tests (SNR_{in} = -30 dB), all corresponding to one power accumulation (N_{sa} = 1). For these cases and using the input parameters as specified above, the theoretical limit on system output SNR is given by:

$$SNR_o = SNR_{in}\, 2BTN_{bins} \approx 30.7 \text{ dB}$$

The average sample output SNRs from the simulation experiments corresponding to different noise realizations and using both N_{bits} = 4 and 8 are tabulated in Table 1. As is seen, the current system (with N_{bits} = 4) is within 1.5 dB of theoretical performance. Increasing the correlator input data paths to 8 bits improves system performance by approximately 1 dB.

The second set of tests was conducted to assess the impact of a DC bias offset at the A/D converters on system performance. All of these tests were again run at the high input SNR level (SNR_{in} = -30 dB) with N_{sa} = 1 and N_{bits} = 4 and 8. The results of these experiments are presented in Figs. 2 and 3. As is seen, at least in terms of output SNR, the system is remarkably robust to A/D bias offsets. For N_{bits} = 4 (Fig. 2), the sample output SNR varies by only approximately 2 dB up to DC bias offset levels of 0.1, above which system performance degrades dramatically. This bias level (0.1) corresponds to 10 percent of the A/D full scale input level or, equivalently, to approximately 13 quantization levels of the A/D converters. For N_{bits} = 8 (Fig. 3), output SNR again drops dramatically at a DC bias offset in excess of 0.1, but the variation in output SNR below this offset level is less than that for N_{bits} = 4.

The final set of system tests consisted of low-input SNR tests (SNR_{in} = -55 dB) corresponding to both 1 power accumu-

lation and 50 power accumulations. For these cases, the theoretical limits on system output SNR are given by:

$$SNR_o = SNR_{in}\, 2BTN_{bins} \approx 5.7 \text{ dB } (N_{sa} = 1)$$

and

$$SNR_o = SNR_{in}\, 2BTN_{bins}\sqrt{50} \approx 14.2 \text{ dB } (N_{sa} = 50)$$

Slices of the range-Doppler output maps evaluated at the maximum signal bin and spanning a total of ±16 Doppler bins are plotted in Fig. 4 for both N_{sa} = 1 and 50. As is seen, the signal peak is clearly detectable for N_{sa} = 50. For N_{sa} = 1, the signal is visible but cannot be unambiguously detected (a number of noise peaks exceeded the signal peak over the entire 2560-point range-Doppler map computed for this case). The computed output SNR for these cases were $SNR_o \approx 6.3$ dB (N_{sa} = 1) and $SNR_o \approx 12.6$ dB (N_{sa} = 50). The former case is anomalous due to the high level of system noise (relative to the signal level). The latter case, corresponding to 50 power averages, is within 1.6 dB of theoretical performance which corresponds closely to the results presented in Table 1 for the high SNR case.

IV. Conclusions

The simulation results presented here suggest that system performance should be within approximately 1.5 dB of theoretical over the nominal range of system operating parameters which will be utilized in the upcoming Mars BPC experiments. Furthermore, the incorporation of 8-bit input data to the correlators will only increase performance by approximately 1 dB. Finally, the system appears to be robust against A/D bias offsets at least for the short code bauds used in the Mars BPC experiments. (The impact of DC bias offset will be more severe as the code baud increases due to the increased post-baud integration required.)

It should be noted that although these simulations do take into account the finite digital precision effects inherent in this system, other effects such as A/D nonlinearities will further limit system performance over what has been predicted by this performance analysis.

References

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[2] S. Brokl, "Polynomial Driven Time Base and PN Generator," *TDA Progress Report 42-75*, vol. July–September 1983, Jet Propulsion Laboratory, Pasadena, California, pp. 84–90, November 15, 1983.

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[4] K. Farazian and R. Jurgens, "Programmable Digital Baud Integrators for the Radar High-Speed Data Acquisition System," *TDA Progress Report 42-79*, vol. July–September 1984, Jet Propulsion Laboratory, Pasadena, California, pp. 142–151, November 15, 1984.

[5] H. Van Trees, *Detection, Estimation, and Modulation Theory, Part I*, New York: Wiley Press, 1968.

Table 1. High input SNR test results

SNR_o: simulation experiments, dB		SNR_o: theoretical limit, dB
$N_{bits} = 4$	$N_{bits} = 9$	
29.3	30.4	30.7

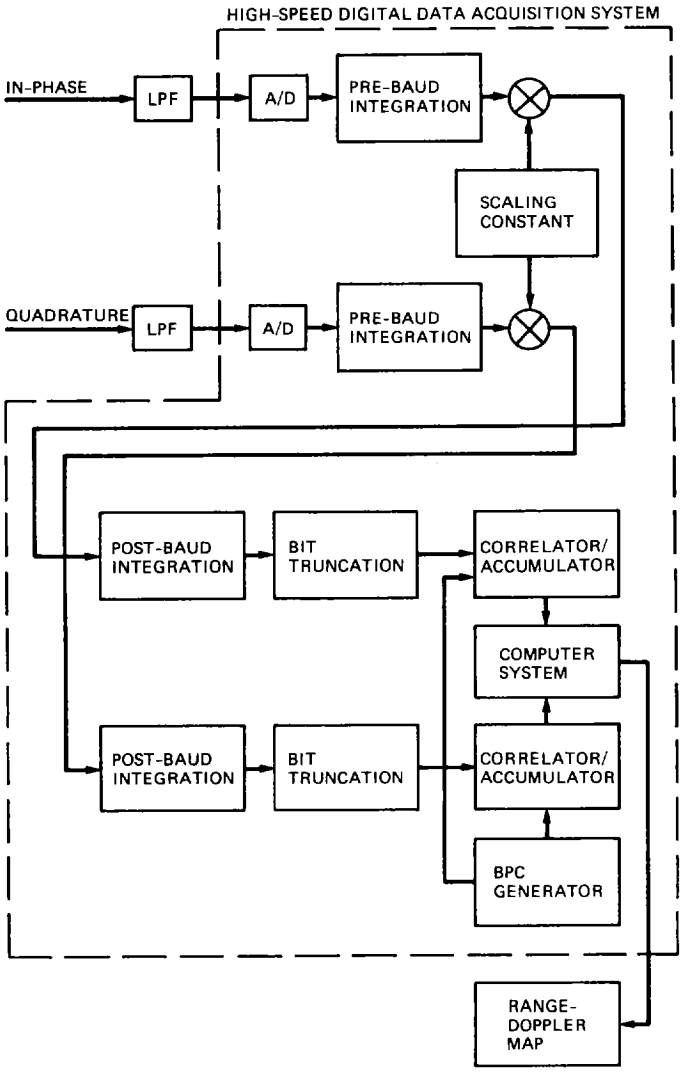

Fig. 1. System block diagram

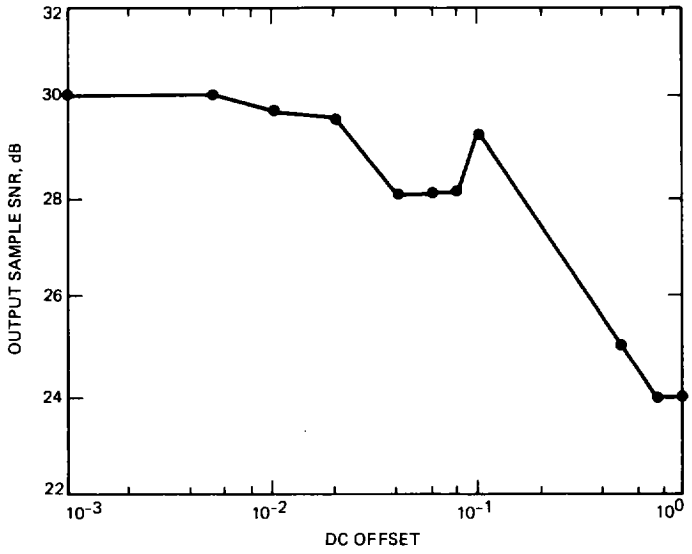

Fig. 2. System output SNR for $N_{bits} = 4$

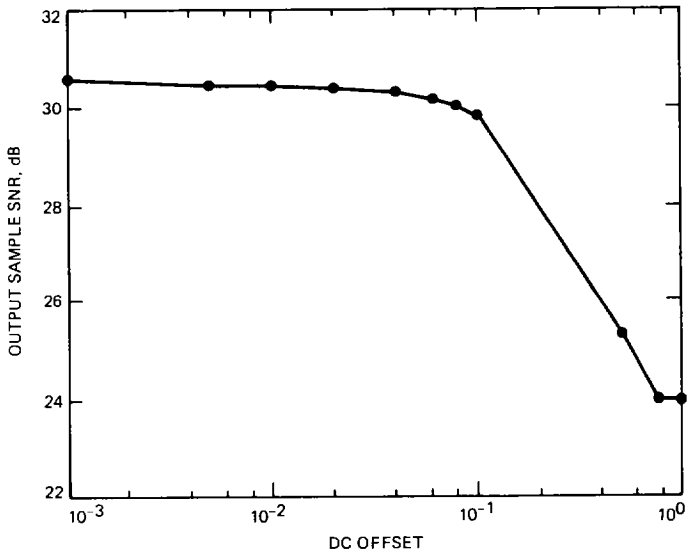

Fig. 3. System output SNR for N_{bits} = 8

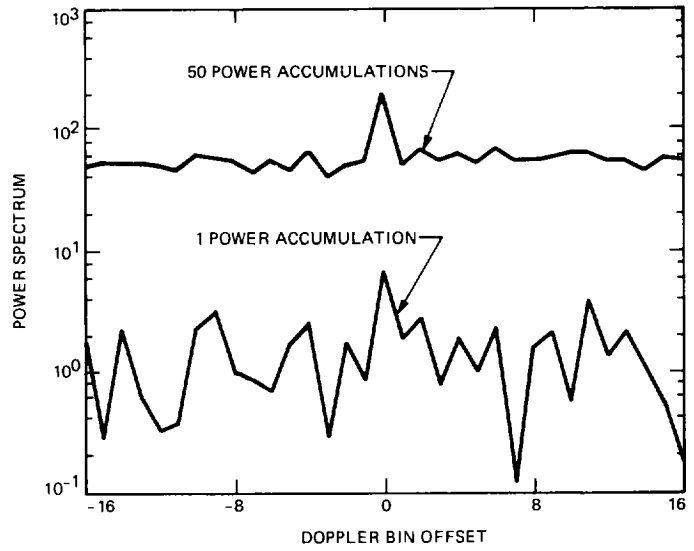

Fig. 4. Output range-Doppler data for SNR_{in} = −55 dB