Block Diagrams of the Radar Interface and Control Unit

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The Interface and Control Unit is the heart of the radar module, which occupies one complex channel of the High-Speed Data Acquisition System of the Goldstone Solar System Radar. Block diagrams of the interface unit are presented as an aid to understanding its operation and interconnections to the rest of the radar module.

I. Introduction

The Goldstone Solar System Radar contains eight radar modules. Each module processes data from a complex channel of the High-Speed Data Acquisition System [1]. The heart of each radar module is a collection of digital control circuits called the Interface and Control Unit. Because of its complexity, the interface unit is poorly understood. This article provides a systematic analysis of the interface unit through block diagrams and shows how the radar module's two main processing parameters, correlation lag length and accumulation depth, are controlled.

Understanding the interface unit's operation provides confidence in its proper operation (and by extension, confidence in overall radar processing), plus the ability to correct faults that occur in the interface unit or radar module. A further motivation occurs from time to time as the need for improved processing becomes apparent. For instance, there is a current requirement to increase the number of radar range bins from 256 to 2048. This parameter is controlled by the interface unit.

Figure 1 (from [1]) shows the functions of the radar module. Data and control signals into and out of each radar module pass through the module's Interface and Control Unit. The interface unit is commanded by a VAX 11/780 computer via a DR11-C interface, which resides on the VAX Unibus. One DR11-C serves all eight radar modules. Complex input data comes from an analog-to-digital (A/D) converter, which may include a digital integrator, at data rates up to 10 megasamples per second for each axis. The interface unit feeds this input data to one of two demodulator/correlators. Output data from each demodulator is fed directly to an accumulator. The correlation lag length and number of accumulation samples are controlled by the interface unit, and are programmable from the VAX computer. (Each radar module has four wire-wrapped boards: two demodulator/correlator boards, one board containing both accumulators, and the Interface and Control Unit board.) Output data from the accumulators go to the VAX computer through a general purpose input/output processor (GPIOP) and Floating Point Systems FPS 5210 array processor. These units are outside the radar module. An overview of the entire radar processor is given in [2].

II. Demodulator/Correlator and Accumulator Functions

The digitized radar echo signal, corrupted with noise, is correlated with a delayed version of itself or with a locally generated version of the maximal length pseudorandom noise

(PRN) code which was transmitted. In each case, the correlation is between a four-bit representation of the signal and a single-bit representation of either the delayed signal or PRN code.

Let the signal data be divided into n sets, with each set consisting of 256 samples. Then the ith sample from the nth data set is

$$S(i,n) = s_3(i,n) \cdot 2^3 + s_2(i,n) \cdot 2^2$$

$$+ s_1(i,n) \cdot 2^1 + s_0(i,n) \cdot 2^0$$

where each s_i is either a 1 or 0, and $i = 0, 1, \ldots, 255$.

The output of the correlator/demodulator at instant i, using 256 lagged values of $S(i,n)$, is

$$Y(i,n) = \sum_{k=0}^{255} S(i-k,n)\,C(k,n)\,M(k)$$

$$n = 0, 1, 2, \ldots \qquad (1)$$

where $C(k,n)$ is binary-valued, and represents either the most significant bit of the signal $S(k,n)$ or the PRN code. The $M(k)$ represent binary-valued mask bits (properly called "unmask" bits) used to prevent undesired terms from appearing in the sum. The mask bits set the upper value of the summation index if fewer than 256 terms are desired, that is,

$$M(k) = 1 \ , \quad k = 0, 1, \ldots, m \leqslant 255$$

$$M(k) = 0 \ , \quad m < k \leqslant 255$$

Each $Y(i,n)$ occupies a time bin, i.e., a radar range bin. There are 256 bins in each radar module. Since the correlator/demodulator sums 256 samples, each containing four bits, each $Y(i,n)$ occupies 12 bits.

The Y are further filtered at the accumulator by summing values from different sets, $n = 0, 1, 2, \ldots$, with the same subscript i. The summation can occur for up to 2^{16} sets. If the number of accumulations of each term is N_a, then the output of the accumulator, after N_a additions, is an array of 256 terms with each term given by

$$A(i) = \sum_{n=0}^{N_a-1} Y(i,n) \ , \quad i = 0, 1, \ldots, 255 \qquad (2)$$

where

$$1 \leqslant N_a \leqslant 2^{16}$$

Since up to 2^{16} values of $Y(i,m)$, each 12 bits wide, are summed, the $A(i)$ occupy 28 bits.

A new array of accumulator outputs is available for every $256N_a$ samples at the input of the demodulator. For 10^7 samples/sec and $N_a = 65535$, this occurs at approximately 1.68-sec intervals.

In the evaluation of Eqs. (1) and (2), three cases are of interest, depending on the nature of the $C(k,n)$ factor in Eq. (1).

A. Case 1: Autocorrelation

In Case 1, the received signal is correlated with itself.

$$C(i,n) = s_3(i,n)$$

$$M(i) = 1, \quad i = 0, 1, \ldots, 255$$

$$1 \leqslant N_a \leqslant 2^{16}$$

The transmitted signal is a continuous wave. $C(i,n)$ is the most significant bit of the returned signal. All demodulator lags are unmasked. The number of accumulations can be any value from 1 to 2^{16}.

In the second and third cases, the received signal is cross-correlated with the PRN code which generated the transmitted signal.

B. Case 2: Cross-Correlation with Long Code

The PRN code length $L > 256$. Then N_a is set to approximately $L/256$ [3], as illustrated in Fig. 2(a). The $M(i)$ mask bits are set to 1 for all 256 values of i. This maximizes the correlation between received signal and locally generated code. (This assumes that the code has been correctly delayed to make signal and code line up. This is done through the polynomial-driven time base and PRN generator module outside the radar module, and a software loop.)

C. Case 3: Cross-Correlation with Short Code

The PRN code length $L \leqslant 256$. Then, N_a is set to 1, corresponding to one accumulation in Eq. (2), as shown in Fig. 2(b). The $M(i)$ are set to 1 for the duration of the PRN code word.

The actual implementation of Eqs. (1) and (2) is as follows:

The mask bits $M(k)$ are serially loaded into four correlators. After loading, they remain stationary. Each bit of the signal and the single code bit are serially loaded into one of the correlators, at the signal sample rate (<10 megasamples/sec). At each sample instant, the correlation $Y(i, n)$ is computed.

In order to maintain a running partial sum for the ith value of the summations, the accumulators must store 256 values of $Y(i)$, which grow to 28 bits. Therefore, the accumulator must have a 256 X 28 memory for each set of $A(i)$, and data must be stored and retrieved at the signal sample rate. There are separate memories for the I and Q channels. In addition, the GPIOP reads the data from one set, while a new set is being formed. Therefore, the accumulator board has four memories with 256 X 28 bit capacity, and read/write access time capable of handling 10-megasample/sec data.

The interface unit also contains a memory which is used to provide test data, plus mask and code bits for the two demodulators. Each demodulator requires four bits of data, plus one mask bit and one code bit for 256 lag positions. Therefore the memory size is 256 X 12 for the two demodulators. Although this memory is loaded by the relatively slow DR11-C, it must be downloaded to the demodulators at the signal sample rate.

III. Interface and Control Unit Operation

Figures 3, 4, and 5 present details of the interface unit in block diagram form. The drawings show considerably less detail than the 10-page Radar System Interface Unit schematic.[1] Concentration here is focused on bussed data, important signals, and clusters of circuit elements. For instance, groups of integrated circuit counters are condensed to single blocks, and all integrated circuit packages have been reduced to five types: three-state buffers, registers, counters, multiplexers/demultiplexers, and random-access memory. The details of combinational gating, often a hindrance in understanding controllers, appear as notes on the block diagrams.

A. Interface with DR11-C

Figure 3 shows the connections between the DR11-C and the interface unit. The DR11-C interface consists of two 16-bit unidirectional busses named OUT ⟨0:15⟩ and IN ⟨0:15⟩. At the interface unit, the signals pass through three-state buffers. The busses are accompanied by the following control signals [4]:

CSR0, CSR1. These are user-programmable bits supplied by the DR11-C, used here to select whether DR11-C data is written to Broadcast Register in each interface unit or written to/read from Function Register in the selected interface unit.

INIT. Indicates Unibus reset.

ODTRAN. Same as DR11-C's Data Transmitted. This is a 400-nsec positive pulse indicating that the DR11-C has received data FROM the interface unit. The trailing edge is used.

ONDRDY. Same as the DR11-C's New Data Ready. This is a 400-nsec positive pulse indicating that the DR11-C has transmitted data TO the interface unit. The trailing edge is used.

Each of the eight interface units contains eight Function Registers which can be written from, or read by, the DR11-C interface. Thus the DR11-C must be able to address 64 locations.

A 16-bit Broadcast Register in each interface unit is programmed with a pointer which selects the interface unit and the Function Register to be written or read (see [5]).

The DR11-C has two user-defined bits, CSR0 and CSR1. When CSR0, CSR1 = 00, the data from the DR11-C bus is written to the Broadcast Register. When CSR0, CSR1 = 10, data is written to the Function Register pointed to by the Broadcast Register. (The other two combinations for CSR0, CSR1 are presently unused.) The formats of these eight registers plus the Broadcast Register (from [1]) are shown in Fig. 6.

The particular interface unit (one of eight units) is selected by a three-bit subfield in the Broadcast Register, while the Function Register (one of eight registers) is selected by another three-bit subfield.

The unit address is decoded to form a signal called MODEN (Module Enabled). MODEN gates either the write or read signal from the DR11-C (ODTRAN or ODTRDY) to a demultiplexer/decoder, to form a set of clocks called $\overline{\text{RDFR}n}$ and $\overline{\text{CKFR}n}$ where n is a digit from 0 to 7. (A bar is used in a signal name to indicate that it is active in the zero- or 0-state.)

The $\overline{\text{CKFR}n}$ clock writes data from the DR11-C bus to Function Register n in the enabled interface unit. The clock is a negative-going pulse with 400-nsec width, which is determined by ONDRDY. Writing takes place on its trailing edge for most of the Function Registers.

The $\overline{\text{RDFR}n}$ clock reads data from Function Register n, and gates this data to the DO bus. It is a negative-going pulse with 400-nsec width, which is determined by ODTRAN. The data is placed on the bus while $\overline{\text{RDFR}n}$ is at a low level.

[1] Radar System Interface Unit Schematic (internal document), Communications Systems Research Section, Jet Propulsion Laboratory, Pasadena, California, June 22, 1987.

B. Interface with Demodulator

Figure 4 shows how the interface unit controls the demodulator. Signal data for the demodulator comes from the A/D converters, or may be simulated from test data stored in a random-access memory in the interface unit. The signal data consists of four bits plus a one-bit code bit (or "reference bit"). The single code bit is either the MSB of the unshifted signal or the pseudonoise code.

A system clock (SYSCLK) is supplied from the A/D to the interface unit, which relays it to the correlators and to the accumulators.

The mask bits $M(i)$ from Eq. (1) are downloaded by the DR11-C to the interface unit's memory, and downloaded from there to the correlators where they are stored. They only need be downloaded to the demodulators once for a particular set of lags.

Function Registers 0 to 4 (see Fig. 6) specify the sources for the correlator signal and code bits. Function Register 0 uses bits 0 to 7 to point to the current memory address, and bits 8 and 9 to specify whether the address is to be incremented after a memory read or write.

Data is written to memory using an address counter clocked by CKBM (Load Addresss Counter, Fig. 4). The memory is preloaded with a starting address, using bits 0 to 7 from the DR11-C bus when $\overline{\text{CKFR0}}$ is active. If $\overline{\text{CKFR0}}$ is active, data is written to Function Register 0. (In other words, the counter is Function Register 0, at least for bits 0 to 7.) The counter output assumes this value until a positive-going clock edge is received at CKBM.

Referring to the first note in Fig. 4,

$$\overline{\text{CKBM}} = \overline{(\text{FR008} + \overline{\text{RDFR1}})} * \overline{(\text{FR009} + \overline{\text{CKFR1}})}$$

both $\overline{\text{RDFR1}}$ and $\overline{\text{CKFR1}}$ are negative-going pulses which occur whenever a memory read/write operation occurs. Therefore, CKBM has a positive-going transition only if FR008 or FR009 (which are bits 8 and 9 of function register 0) is true.

Bits 0, 1, and 2 of Function Registers 2 and 3 determine whether the correlator data or mask or code are loaded from memory or from the A/D unit. IBE and QBE (which are derived from these three bits) select a path from the A/D units or from memory (Fig. 4).

If correlator data is to be dumped from memory, then IBE and/or QBE is active and the memory is read at the system clock rate and transmitted to the correlators. Data can also be dumped from memory back to the DR11-C by reading Function Register 1, which enables buffers (Fig. 3). Reading occurs at the address loaded into the Load Address Counter.

C. Interface with Accumulators

Figure 5 shows how the interface unit controls the accumulators. One accumulator has been shown in some detail so the reader can see how the control signals are used.

Twelve-bit data words enter the accumulator at the system clock rate. The accumulator has two 28 X 256 memories for each axis, designated A and B. Partial sums (which can grow to 28 bits in length) for each demodulator lag time are stored in one memory, while complete sums are read from the other memory by the GPIOP. This double-buffering requires external circuitry which is housed in the interface unit. Each memory's address is controlled by an address counter, which is periodically preloaded with all zeros. The interface unit controls the clocking of this counter (which occurs at the system clock rate) and the load time, and selects which counter and which side of the double-buffer are enabled.

The maximum memory address is determined by the maximum lag length in the demodulator. This data is loaded into Function Register 4 (Fig. 5). Eight bits are used for each demodulator. The maximum accumulation length is set in Function Register 5 for I data and 6 for Q data.

These registered values are compared with counters which are preset to zero. Since address-stepping must occur at the incoming data rate from the demodulator, a counter (Fig. 5) is clocked at the system clock rate.

When the counter outputs equal the registered values, another data set of partial sums has been completed. This event clocks another counter which tracks the number (denoted N_A) of data sets. A D-flip-flop with a delay element feedback creates a pulse for this secondary clocking. These counters are compared with a preloaded value of N in Function Registers 5 and 6.

The four comparator output signals, plus CKFR7 and RDFR7 and the system clock, create the necessary control signals. The circuits involve a number of combinational and synchronous gates which are too complex to generalize here. The outputs of the combinational block consist of four sets of signals, one set for each address counter on the accumulator board (Fig. 5).

Accumulator output data is fed to the GPIOP. The device address, as seen from the GPIOP, is determined by an 8:1

multiplexer arrangement, similar to the one used with the DR11-C interface (compare Figs. 3 and 5).

IV. Functional Testing of the Interface and Control Unit

The programmable features of the demodulators and accumulators (in particular, the correlation length and number of samples to be accumulated) are controlled by the interface unit. A simple test is proposed here to ensure that these controls work properly.

The test consists of moving an impulse function through each of the radar module's 256 range bins. An impulse can be created by correlating a maximal-length ($\leqslant$255) pseudonoise sequence code with itself at the demodulator input. Such a code is available at the output of the polynomial-driven time base and PRN generator which is housed in another part of the radar processor [6]. Alternately, the code can be loaded into the interface unit's memory.

The conceptual test setup is shown in Fig. 7. The programmable delay is set to produce a delay kT_s where T_s is the sample period of data at the input of the correlator, and k ranges from 0 to 255. (This delay is programmable at the coder's control registers.)

At the output of the accumulator, the autocorrelation is

$$R_x(t) = -a \qquad t \neq kT_s$$

$$= La \qquad t = kT_s$$

where a is a scale factor, and L is the length of the PRN sequence.

The test can be made quite vigorous by "exercising" each part of the radar module separately. Suppose, for instance, that range bins at one end of the 256-bin range have unexpectedly low values using real data for long range codes (corresponding to Case 2 described in Part II). Assuming that a test impulse also exhibits the same problem, then the accumulation number N_a can be set to different values, beginning with zero. According to Eq. (2), the output impulse (which is actually observed at the output of the FPS 5210 array processor) should increase linearly with N_a at the affected bin. Failure to do so would isolate the accumulator as the source of the problem, or possibly the part of the interface unit which controls the accumulator's address counters. If the signal did increase linearly, but had different values than for other bins, then the problem lies in the demodulator or its controls in the interface unit.

The mask bits can be used to turn the impulse on or off. This verifies that the interface unit's memory and address counters are working properly.

Finally, the test can be used to prove performance for a longer lag length, and under any desired operating condition. It could also be expanded to include the baud-integrating A/D converters which precede the radar module.

V. Summary

This article has presented block diagrams of the Interface and Control Unit, a digital processor that controls functions inside the radar module and provides interconnections between the module and the outside world.

A simple test was proposed which completely verifies operation of the interface unit controls. This test can be further expanded to verify operation under different configurations.

References

[1] S. S. Brokl, "Controller and Interface Module for the High-Speed Data Acquisition System Correlator/Accumulator," *TDA Progress Report 42-83*, vol. July–September 1985, Jet Propulsion Laboratory, Pasadena, California, pp. 113–124, November 15, 1985.

[2] L. J. Deutsch, R. F. Jurgens, and S. S. Brokl, "The Goldstone R/D High-Speed Data Acquisition System," *TDA Progress Report 42-77*, vol. January–March 1984, Jet Propulsion Laboratory, Pasadena, California, pp. 87–96, May 15, 1984.

[3] E. Satorius and S. S. Brokl, "Goldstone Solar System Radar Performance Analysis," *TDA Progress Report 42-93*, vol. January–March 1986, Jet Propulsion Laboratory, Pasadena, California, pp. 302–308, May 15, 1988.

[4] DR11-C General Device Interface User's Manual, Publication EK-DR11C-OP, Digital Equipment Corporation, Maynard, Massachusetts.

[5] S. S. Brokl, "A General Monitor and Control Interface to the VAX Unibus by Way of DR11-C I/O Port," *TDA Progress Report 42-83*, vol. July–September 1985, Jet Propulsion Laboratory, Pasadena, California, pp. 125–133, November 15, 1985.

[6] K. H. Farazian and R. F. Jurgens, "Programmable Digital Baud Integrator for the Radar High-Speed Data Acquisition System," *TDA Progress Report 42-79*, vol. July–September 1984, Jet Propulsion Laboratory, Pasadena, California, pp. 142–151, November 15, 1984.

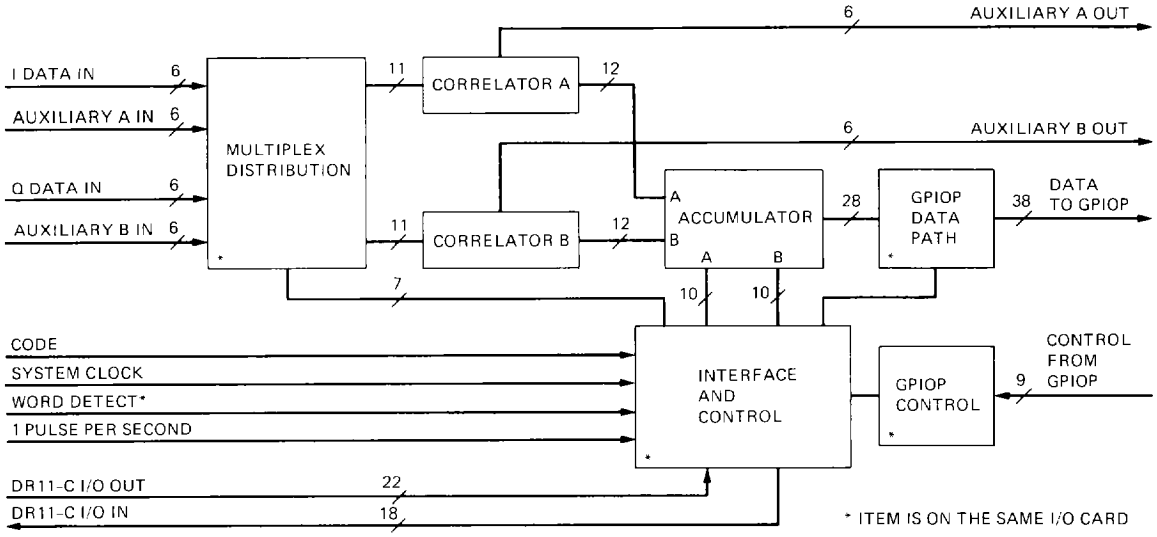


Fig. 1. Radar module block diagram.

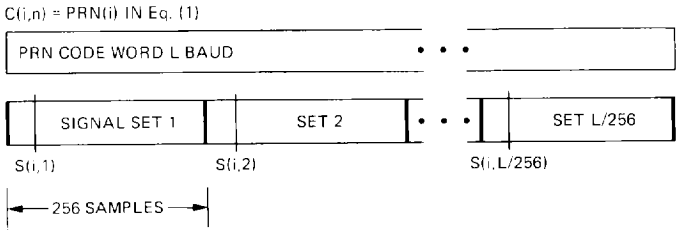


Fig. 2(a). Cross-correlation with long code.

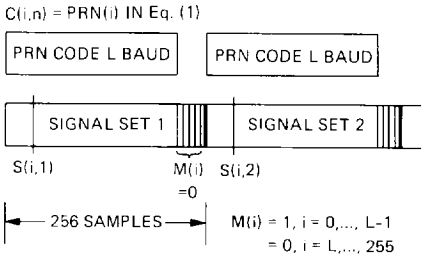
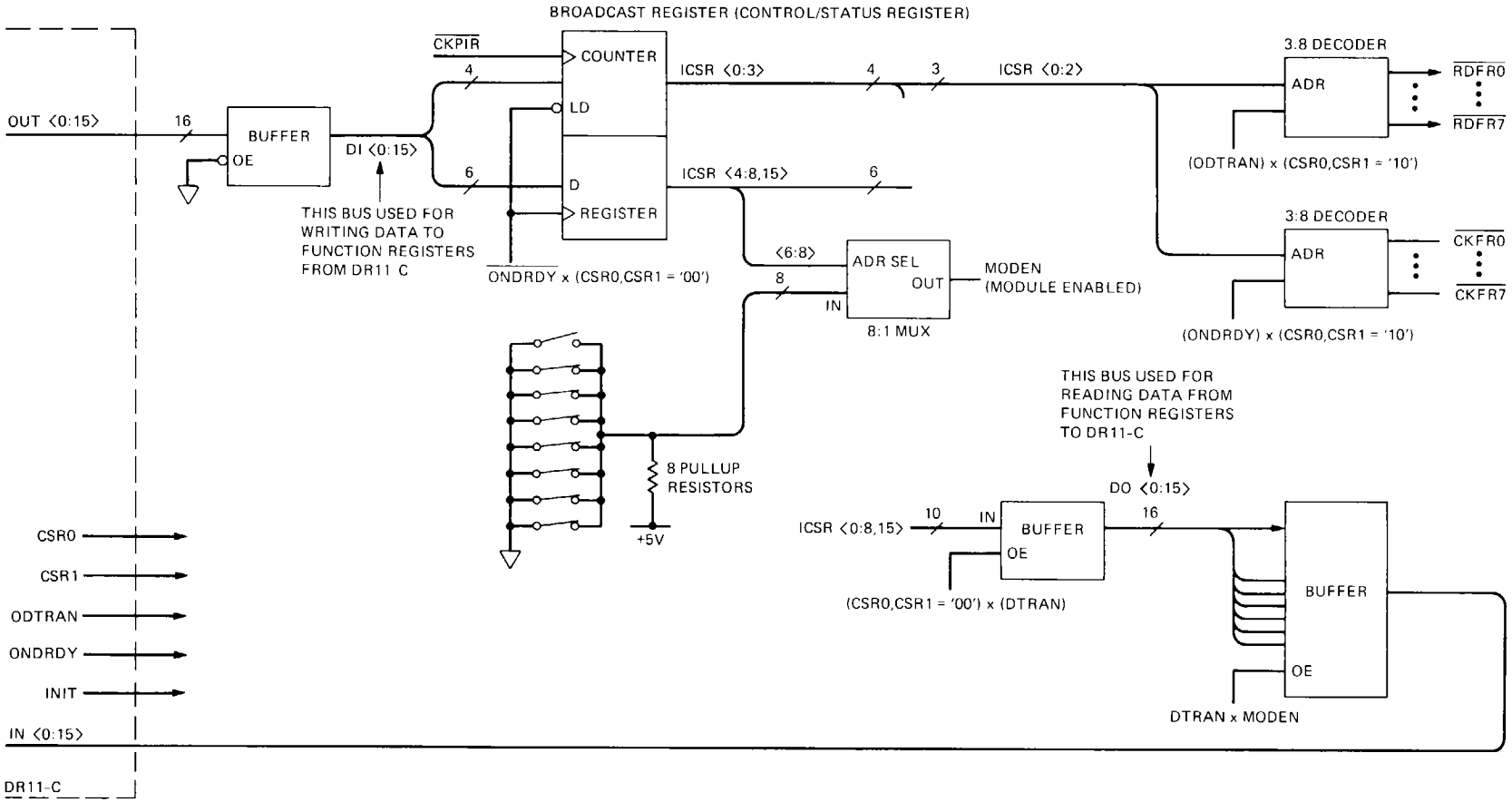


Fig. 2(b). Cross-correlation with short code.



$\overline{CKPIR}$ = (FR008 + $\overline{ICSR04}$ + $\overline{ODTRAN}$) * (FC009 + $\overline{ICSR05}$ + $\overline{ONDRDY}$)

FR008,FR009 = BITS 8,9 OF FUNCTION REGISTER 0

(THE INTENT IS TO INCREMENT FUNCTION REGISTER POINTER IF ICSR04 OR ICSR05 = '1', BUT TO INHIBIT THIS IF FR008 OR FR009 IS '1'.)

Fig. 3. Block diagram of interface with DR11-C.

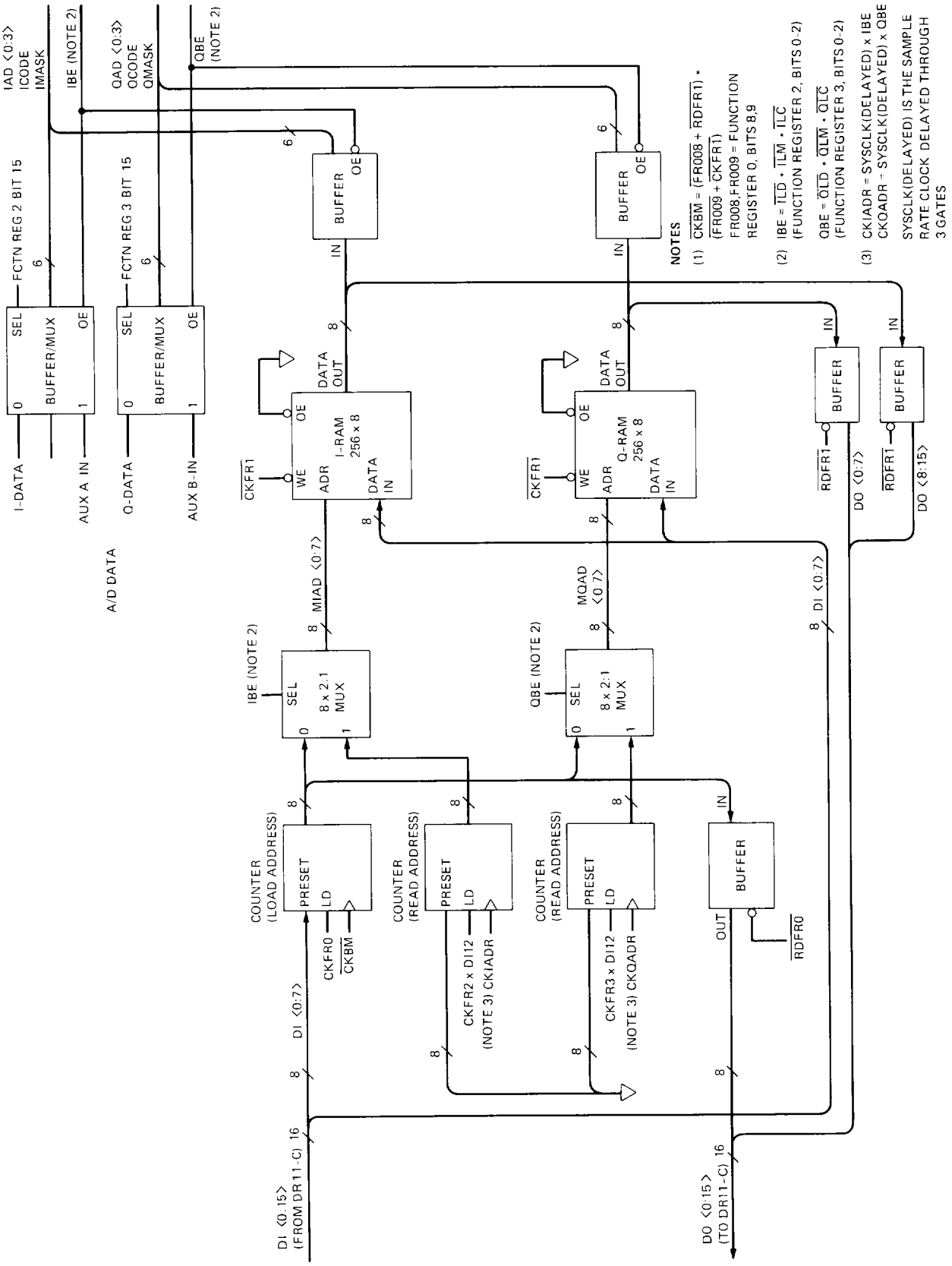


Fig. 4. Block diagram of interface with demodulator.

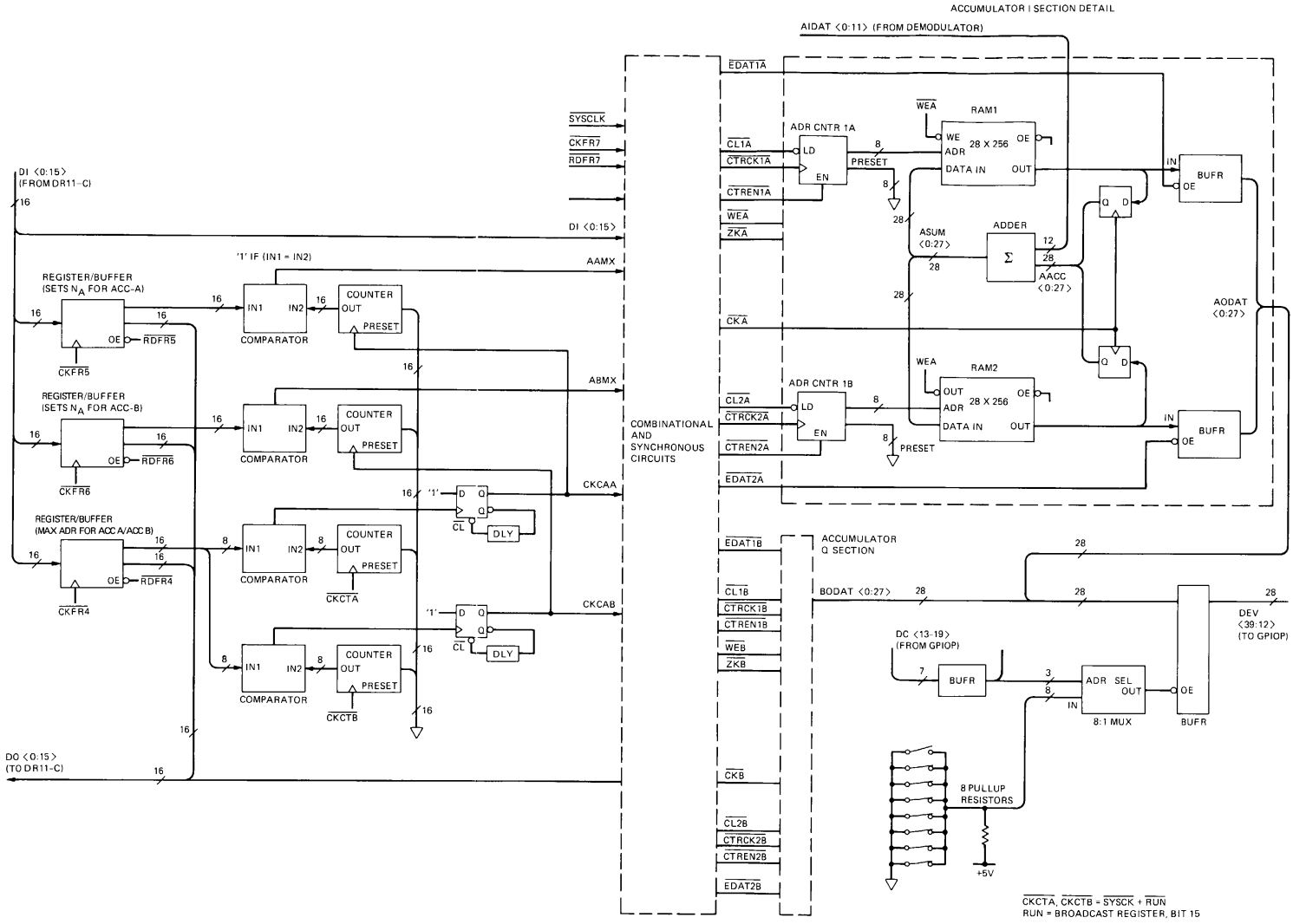


Fig. 5. Block diagram of interface with accumulator.

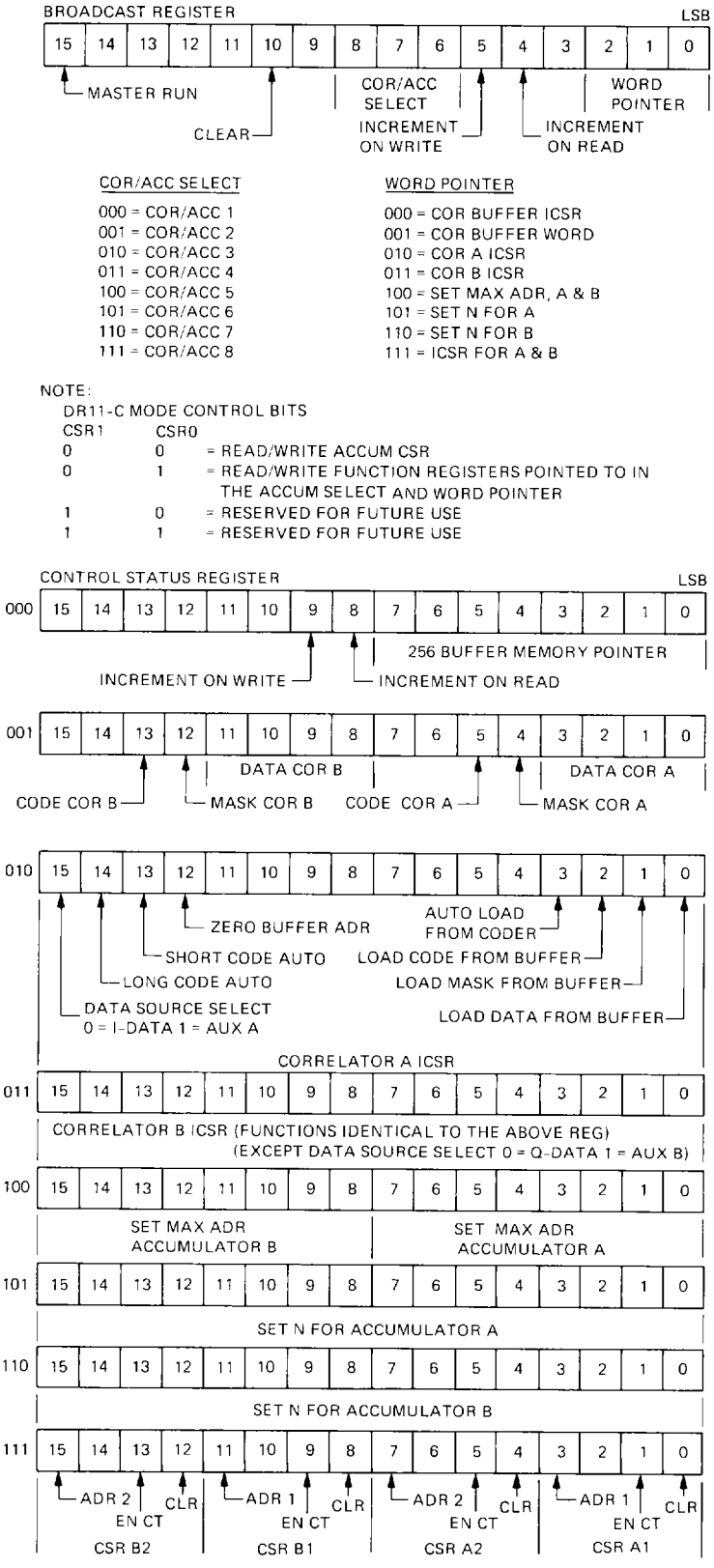


Fig. 6. Interface and Control Unit Function Registers.

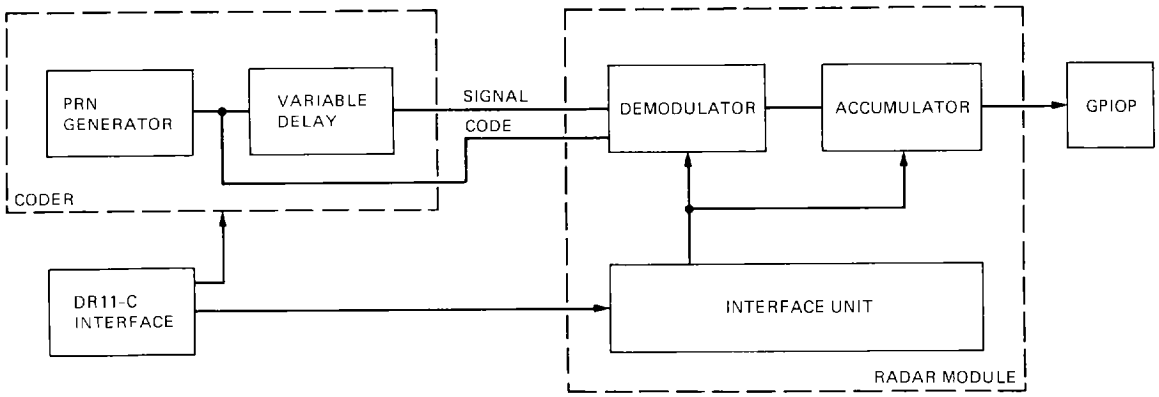


Fig. 7. Setup for radar module test.