Wideband Phase-Locked Angular Modulator

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A phase-locked loop (PLL) angular modulator scheme has been proposed which has the characteristics of wideband modulation frequency response. The modulator design is independent of the PLL closed-loop transfer function H(s), thereby allowing independent optimization of the loop's parameters as well as the modulator's parameters. A phase modulator implementing the proposed scheme was built to phase modulate a low-noise phase-locked signal source at the output frequency of 2290 MHz. The measurement results validated the analysis by demonstrating that the resulting baseband modulation bandwidth exceeded that of the phase-locked loop by over an order of magnitude. However, it is expected to be able to achieve much wider response still.

I. Introduction

Phase-locked loops (PLL) are sometimes designed to mechanize the generation of phase modulation (PM) or frequency modulation (FM) signals. In a synthesized signal generator, the same frequency synthesis loops are often also used for providing PM and/or FM capability. As such an angular modulator, the PLL has the following desirable characteristics: the modulated carrier frequency can be stabilized by a stable reference signal; and a large modulation index can be obtained by suitable phase compression in the loop [1]. In a typical phase-locked angular modulator, shown in Fig. 1, the modulating signal is added to the appropriate baseband points in the loop to produce the desired PM or FM [2]. An analysis of this scheme shows that the modulation transfer function relating the output phase to the input phase modulating voltage is propor-

tional to the PLL closed-loop transfer function $H(s)$ (a low-pass function), whereas the function relating the output instantaneous frequency to the input frequency modulating voltage is proportional to the complementary high-pass of $H(s)$. This dependence of the modulation transfer function on the PLL closed-loop characteristics has the following consequences:

(1) The configuration of Fig. 1 does not lend itself to easy implementation of both PM and FM using the same loop. For PM, a sufficiently wide loop bandwidth is required to accommodate the high frequency modulating signal, whereas for FM a narrowband loop is needed to prevent the loop from tracking out the low frequency modulating signal.

(2) Wideband modulation frequency response is often not possible since the design is usually constrained by considerations such as spurious signal rejection, loop stability, settling time, and noise performance that place upper and lower limits on the loop bandwidth.

(3) The loop introduces phase distortion to the output modulating envelope because of its band-limited nature.

A phase-locked modulator scheme is proposed that eliminates the above limitations. It will be shown that the modulation transfer function resulting from this scheme, which has the characteristics of wideband frequency response, is independent of the PLL transfer function. An experimental phase modulator was built. The measured data substantiate the analysis by demonstrating that the resulting baseband modulation bandwidth exceeded that of the PLL by over an order of magnitude.

II. Analysis

Figure 2 shows the generalized block diagram of the proposed modulator scheme. A noise-free and linearized model of a PLL consisting of a phase detector, loop filter, and a voltage-controlled oscillator (VCO) is assumed. The following notation will be used:

$\Theta_R(s)$ = reference phase, rad

$\Theta_0(s)$ = output phase, rad

$\Theta_M(s)$ = output phase modulation, rad

$\Omega_M(s)$ = output frequency modulation, rad/sec

K_D = phase detector gain, volt/rad

K_0 = VCOs gain constant, rad/sec/volt

$F(s)$ = loop filter

$P(s), Q(s)$ = modulation filters

$V_M(s)$ = input modulating signal, volt

The output phase for the loop in Fig. 2 is given by

$$\Theta_0(s) = \frac{K_0}{s}\left\{ P(s)V_M(s) + F(s)\Big[Q(s)V_M(s) \right.$$

$$\left. + K_D\Big(\Theta_R(s) - \Theta_0(s)\Big)\Big]\right\} \tag{1}$$

Simplifying yields

$$\Theta_0(s) = \frac{K_0 K_D F(s)}{s + K_0 K_D F(s)}\Theta_R(s)$$

$$+ \frac{K_0 P(s)}{s + K_0 K_D F(s)}V_M(s)$$

$$+ \frac{K_0 F(s)Q(s)}{s + K_0 K_D F(s)}V_M(s) \tag{2}$$

The quantity $K_0 K_D F(s)/[s + K_0 K_D F(s)]$ is the closed-loop transfer function, denoted $H(s)$. Thus,

$$\Theta_0(s) = H(s)\Theta_R(s) + \frac{K_0 P(s)}{s + K_0 K_D F(s)}V_M(s)$$

$$+ \frac{K_0 F(s)Q(s)}{s + K_0 K_D F(s)}V_M(s) \tag{3}$$

$\Theta_R(s)$ defines the reference phase for the loop to maintain lock and is constant as far as the modulation is concerned. So, the output phase modulation due to the input modulating signal is

$$\Theta_M(s) = \frac{K_0 P(s)}{s + K_0 K_D F(s)}V_M(s)$$

$$+ \frac{K_0 F(s)Q(s)}{s + K_0 K_D F(s)}V_M(s) \tag{4}$$

which can be rearranged to yield

$$\Theta_M(s) = \frac{s}{s + K_0 K_D F(s)}\frac{K_0 K_D}{s}P(s)\frac{V_M(s)}{K_D}$$

$$+ \frac{K_0 K_D F(s)}{s + K_0 K_D F(s)}Q(s)\frac{V_M(s)}{K_D} \tag{5}$$

or

$$\Theta_M(s) = \left\{ \Big[1 - H(s)\Big]\frac{K_0 K_D}{s}P(s) + H(s)Q(s)\right\}\frac{V_M(s)}{K_D} \tag{6}$$

The output instantaneous frequency is the derivative of the phase. Hence the output frequency modulation is

$$\Omega_M(s) = s\Theta_M(s)$$

$$= \left\{ \left[1 - H(s)\right] P(s) + H(s)\frac{s}{K_0 K_D} Q(s) \right\} K_0 V_M(s) \tag{7}$$

It is evident from Eqs. (6) and (7) that the design strategy is to choose the correct modulation filters $P(s)$ and $Q(s)$ that would enable the appropriate compensations to eliminate the terms involving $H(s)$ and thus allow the modulation response to be independent of the PLL transfer function parameters. That is, it is desirable to choose $P(s)$ and $Q(s)$ such that the sums inside the brackets of Eqs. (6) and (7) simplify to unity. The two cases of PM and FM are considered.

A. Phase Modulation

Choose $P(s) = s/K_0 K_D$. This is the transfer function of a differentiator where the time constant equals $1/K_0 K_D$, and choose $Q(s) = 1$. Then Eq. (6) becomes

$$\Theta_M(s) = \left\{ \left[1 - H(s)\right] \frac{K_0 K_D}{s}\frac{s}{K_0 K_D} + H(s) \right\}\frac{V_M(s)}{K_D} \tag{8}$$

or

$$\Theta_M(s) = \frac{1}{K_D} V_M(s) \tag{9}$$

The output phase is thus proportional to the input modulating signal, scaled by the constant $1/K_D$. This is the desired result.

B. Frequency Modulation

Choose $P(s) = 1$, and choose $Q(s) = K_0 K_D/s$. This is the transfer function of an integrator with the time constant equal to $1/K_0 K_D$. Then, Eq. (7) becomes

$$\Omega_M(s) = \left\{ \left[1 - H(s)\right] + H(s)\frac{s}{K_0 K_D}\frac{K_0 K_D}{s} \right\} K_0 V_M(s) \tag{10}$$

or

$$\Omega_M(s) = K_0 V_M(s) \tag{11}$$

The output instantaneous frequency is thus proportional to the input modulating signal, scaled by the constant K_0. This is the desired result.

III. Discussion

Equations (9) and (11) demonstrate that the output PM and FM frequency responses are independent of the PLL transfer function $H(s)$. Specifically, the detail of the loop filter $F(s)$ is completely irrelevant as far as the overall modulation process is concerned. To the extent that the linearized model of the PLL is valid, and to the degree that $P(s)$ and $Q(s)$ can be realized, the design of the modulator can be completely independent from the PLL closed-loop characteristics; the important parameters, as shown by the analysis, are the phase detector and the VCO gain constants. This independence of the modulation frequency response from the transfer function $H(s)$ is extremely desirable. Since Eqs. (9) and (11) are implied, the proposed modulator scheme is a wideband configuration and therefore does not suffer from the inherent limitations associated with the configuration of Fig. 1 as mentioned above.

It is possible to obtain wideband response in the configuration of Fig. 1 by introducing the appropriate compensation networks to the input modulating signal prior to the PLL modulation terminals and external to the PLL. These networks would be in the form of $1/H(s)$ or $1/[1 - H(s)]$ for PM or FM, respectively. The drawback is that $H(s)$ must be accurately known. Also, if a high-order loop is required, the resulting high-order compensation network could be difficult to design. Furthermore, the loop would invariably have spurious poles contributed by the loop filter network. This would make extremely difficult the task of fully characterizing $H(s)$ to the degree required for wideband compensation.

Based on the results of Eqs. (9) and (11) it is possible to propose an entirely new modulator configuration which is shown in Fig. 2. This scheme takes advantage of the feedback loop and applies the modulation to both baseband positions before and after the loop filter such that the modulator design is free from the effect and constraint of $F(s)$. The compensation networks are simply the differentiator and the integrator whose time constants are solely determined by the product $K_0 K_D$. They remain unchanged regardless of the specific detail of $F(s)$, and hence the loop order. In particular, as far as the modulator design is concerned, any spurious poles of $F(s)$ or of any networks in the signal path from the phase detector output to the VCO input are lumped together with $F(s)$ as part of an equivalent loop filter. This also applies to any time delay functions in that path. However, as will be shown in the experimental results discussed in Section IV, the design is not free of the effect of spurious poles in the loop that are not made part of the loop filter.

This scheme is ideal since $H(s)$ is self-negating to unity as shown by Eqs. (8) and (10) and obviates the necessity for an accurate external loop compensation to $H(s)$ or the need to compromise between the PLL and the modulator performance.

Figures 3 and 4 show block diagrams of the proposed phase modulator and frequency modulator. It is evident from the diagrams that the frequency modulator can be derived from the phase modulator by inserting one integrator in each of the phase-modulating signal-injection arms (one of which nullifies the differentiator).

The linearity requirement constrains the peak modulation index seen at the phase detector, hereafter denoted β_p. This means that the sum of the peak phase error in the absence of modulation and β_p must be within the linear range of the phase detector. For a sinusoidal phase detector transfer function, this sum should not exceed 30 deg for good linearity. Also, since the PLL is a carrier tracking loop, the design must prevent the range of modulation index from causing a carrier-null at the phase detector input. The constraint on β_p can be mitigated by judicious choice of the phase compression factor N in the feedback loop that would permit a broader range of modulation index at the loop output.

Linearity of the integrator and the differentiator also constrains β_p. In the PM case, it can be shown that β_p must satisfy $\beta_p < K_0 V_{SAT}/(2\pi f_{max})$, where V_{SAT} is the saturation voltage of the differentiator and f_{max} is the highest input modulating frequency. Similarly in the FM case, β_p must satisfy $\beta_p < V_{SAT}/K_D$, where V_{SAT} is the saturation voltage of the integrator (here β_p is the ratio of the maximum frequency deviation and the lowest input modulating frequency).

It would appear from Eq. (11) for the FM case that it would be possible to apply modulation at very low frequency all the way down to DC. Then, one could generate a constant frequency shift at the VCO output by applying a constant DC voltage at the modulating input. However, a DC response is not possible in reality because the integrator (in Fig. 4) would eventually saturate. Secondly, the phase error would eventually exceed the dynamic range of the phase detector and the loop would then no longer remain linear or in lock. However, by careful design to prevent component saturation and to remain within the linear range of the PLL, it is possible to modulate the frequency as close to DC as desired.

IV. Experiments

A phase modulator implementing the proposed scheme was built to verify the analysis. It was designed to phase modulate a phase-locked signal source whose design emphasis is for phase-noise and spurious signal power spectral density performance. A block diagram of the circuit is shown in Fig. 5. Basically, the loop is a second-order PLL and is of the mix-down-and-divide design for low-noise performance. The VCO is a cavity oscillator operating at a frequency of 2290 MHz. The ×24 multiplies the 95-MHz phase-locked crystal oscillator output frequency to 2280 MHz. The 2280-MHz signal downconverts the cavity oscillator output at 2290 MHz to an IF of 10 MHz. The ÷2 frequency divides the 10-MHz IF to 5 MHz and effects a phase compression by a factor of 2. A temperature-stabilized low-noise crystal oscillator provides the 5-MHz reference signal. From the phase-noise data of the 95-MHz phase-locked crystal oscillator and the free-running cavity oscillator, the loop parameters were designed for optimum phase noise performance at the output, with the constraint of adequate rejection of the 5-MHz reference signal feed-through. The loop natural frequency was selected to be about 35 kHz and the damping ratio to be 0.707. Measured gain constants of the sinusoid phase detector and the VCO are 0.30 volt/rad and 300 kHz/volt, respectively, which yields the time constant $1/K_0 K_D$ of 1.77 μsec. An op-amp differentiator with a 3-dB bandwidth of about 14 MHz was used. A gain adjustment was included as part of the differentiator to effectively provide the adjustment of the time constant.

To test the circuit, a baseband sinusoidal signal from a signal generator was applied to phase modulate the 2290-MHz carrier output. To assure linearity at the phase detector and not to exceed the linear range of the differentiator at high modulation frequency, the modulation index was kept small, at about 3 deg. The output was then observed on a spectrum analyzer while sweeping the input modulating signal frequency. The spectrum analyzer thus displays the magnitude of the modulation transfer function being measured at the carrier frequency.

Figure 6 shows the result when the modulating signal is applied to the loop filter input only. As would be expected, the output modulation spectrum is symmetrical about the carrier frequency. Note that in this case the display spectrum envelope is proportional to $|H(jw)|$. It can be seen that the actual natural frequency is about 40 kHz, and the damping ratio is about 0.50. The 3-dB bandwidth of the loop is about 75 kHz. Figure 7 shows the result when the modulating signal is applied to the differentiator input only; here the spectrum envelope is

proportional to $|1 - H(jw)|$. These two cases correspond to the configuration in Fig. 1, and the results in Figs. 6 and 7 demonstrate the band-limited nature of that circuit.

Figure 8 shows the spectrum analyzer display when the modulating signal is applied to both inputs of the loop filter and the differentiator. Note that the previous high- and low-frequency roll-offs in Figs. 6 and 7 as well as the amplitude peakings occurring at the loop's natural frequency have disappeared. The flat spectrum indicates that wideband frequency response has been achieved as predicted by the analysis. Figure 9 shows the same results but with the spectrum analyzer set at a 10-MHz span. As can be seen by comparing Figs. 6 and 8 (or 9), the phase modulation transfer function bandwidth has increased by more than an order of magnitude over that of the PLL. Specifically, the baseband modulation 3-dB bandwidth as shown in Fig. 9 is about 1.50 MHz in comparison with the 3-dB bandwidth of only 75 kHz for the loop as shown in Fig. 6. The rolling-off of the output modulation spectrum in Fig. 9 (instead of its remaining flat as it should) was puzzling at first. It was later realized that this is because the driving circuit of the VCO varactor diode as seen from the output of the differentiator network approximates an RC lowpass function with a 3-dB bandwidth of about 1.50 MHz. This forms a spurious pole as discussed in Section III. Suffice it to say that this part of the circuit must be designed properly or be lumped as part of the loop filter network in order to improve high frequency modulation performance.

V. Conclusion

A phase-locked angular modulator scheme has been proposed which has the characteristics of wideband modulation frequency response. The modulator design is independent of the PLL closed-loop transfer function $H(s)$, thereby allowing independent optimization of the PLL parameters as well as the modulator's parameters. A phase modulator implementing the proposed scheme was built to phase modulate a phase-locked signal source that was designed for low-noise performance at 2290 MHz. The measurement results validated the analysis by demonstrating that the resulting baseband modulation 3-dB bandwidth exceeded that of the PLL by over an order of magnitude. With an additional implementation effort and measurements to improve the high frequency performance, it is expected that flat wideband modulation response from DC well into the MHz regions can be achieved.

Acknowledgment

References

[1] G. R. Vaughan and E. Osborne, "Phase Locked Phase Modulator," *IEEE International Communications Conference Record, Digest of Papers*, New York, pp. 206–207, 1966.

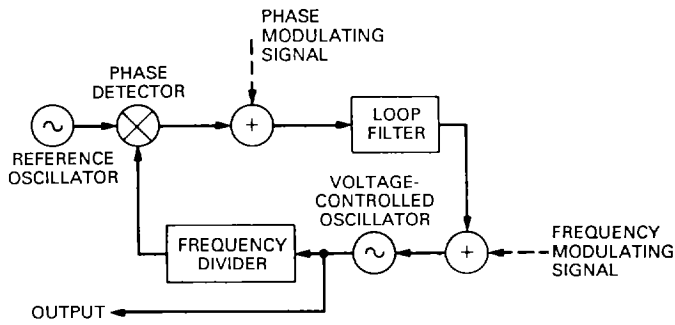[2] F. M. Gardner, *Phaselock Techniques*, New York: John Wiley & Sons, 2nd edition, 1979.
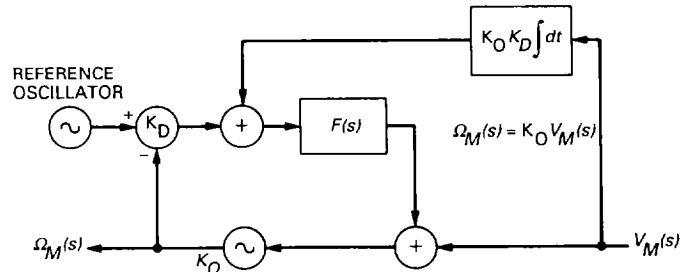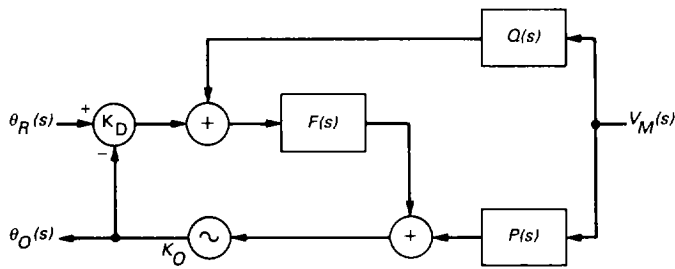
Fig. 1. Typical phase-locked modulator [2].
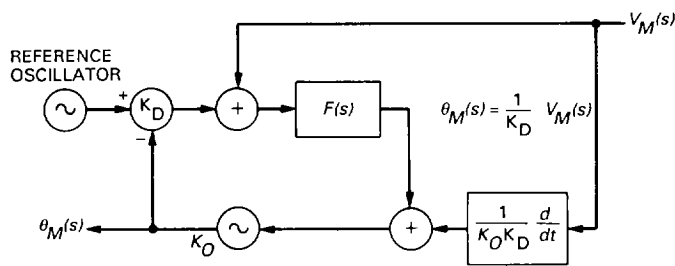

Fig. 2. Proposed phase-locked modulator.

Fig. 3. Proposed wideband phase modulator.
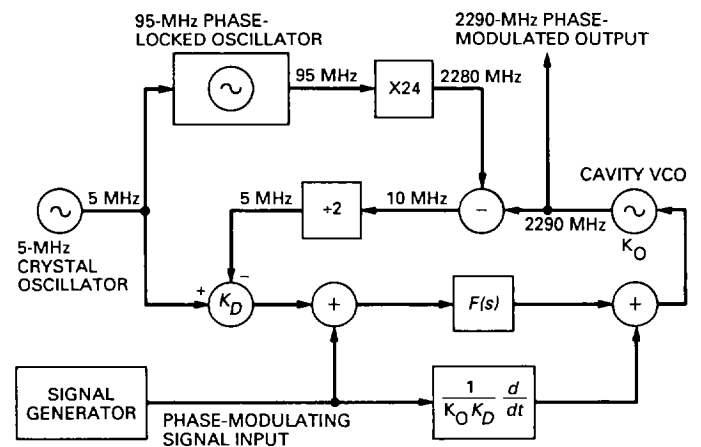

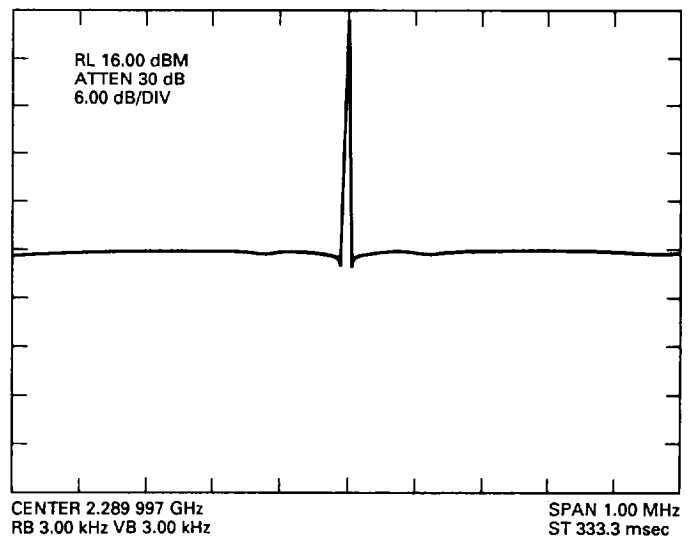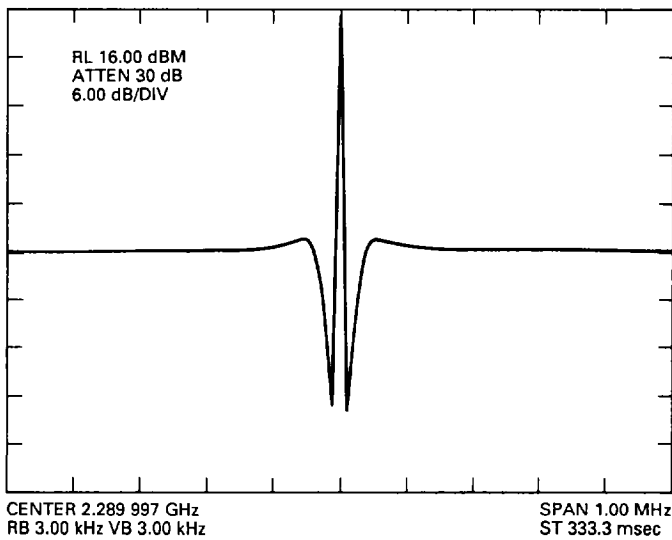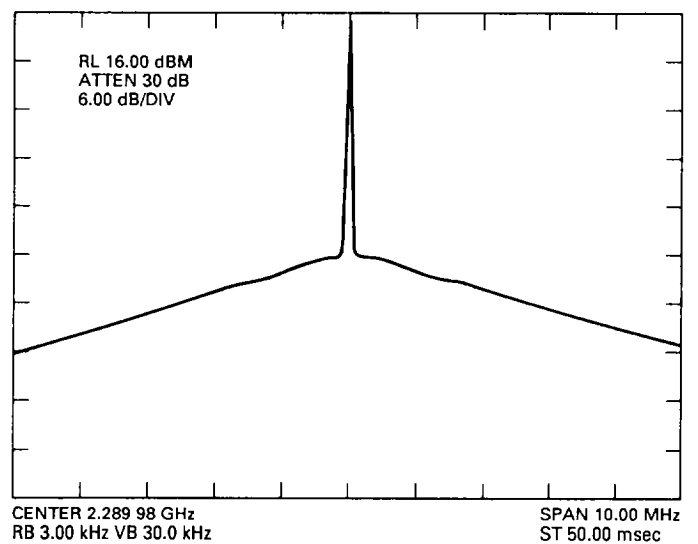Fig. 4. Proposed wideband frequency modulator.

Fig. 5. Experimental wideband phase modulator.

RL 16.00 dBM
ATTEN 30 dB
6.00 dB/DIV

CENTER 2.289 997 GHz
RB 3.00 kHz VB 3.00 kHz
SPAN 1.00 MHz
ST 333.3 msec
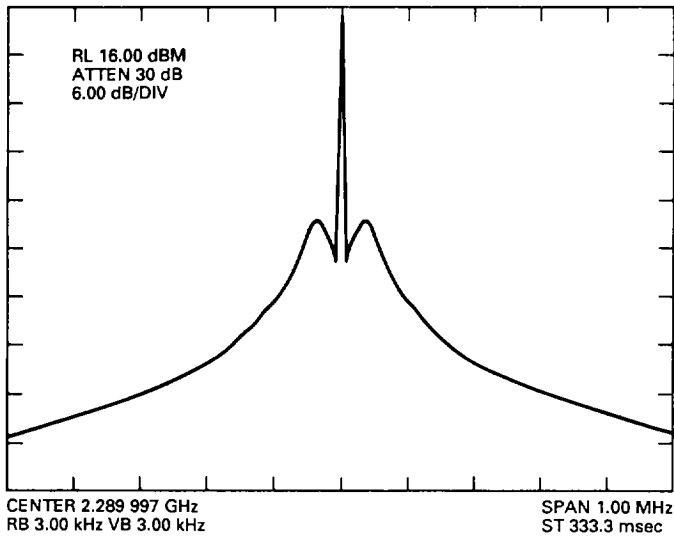
Fig. 6. Output phase modulation spectrum without compensating differentiator.

RL 16.00 dBM
ATTEN 30 dB
6.00 dB/DIV

CENTER 2.289 997 GHz
RB 3.00 kHz VB 3.00 kHz
SPAN 1.00 MHz
ST 333.3 msec

Fig. 8. Output phase modulation spectrum of the proposed wideband scheme.

RL 16.00 dBM
ATTEN 30 dB
6.00 dB/DIV

CENTER 2.289 997 GHz
RB 3.00 kHz VB 3.00 kHz
SPAN 1.00 MHz
ST 333.3 msec

Fig. 7. Output phase modulation spectrum with compensating differentiator only.

RL 16.00 dBM
ATTEN 30 dB
6.00 dB/DIV

CENTER 2.289 98 GHz
RB 3.00 kHz VB 30.0 kHz
SPAN 10.00 MHz
ST 50.00 msec

Fig. 9. Output phase modulation spectrum of the proposed wideband scheme at 10-MHz span.