IBM 360/75 Computer Time Interface

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The IBM 360/75 computer time interface and the capabilities of two custom-feature modifications of the IBM 360/75 are described. The modified IBM 360/75 accepts signals from an existing time reference, provides GMT with 10-μs resolution, includes an interval timer, and provides programmable interrupts.

I. Introduction

The inclusion of a GMT clock interface in the Mark IIIA central processing system (CPS) (Ref. 1) is a direct continuation of Mark II CPS support. Mark II programs that utilized the GMT reference have been converted for Mark IIIA use. The current GMT clock also is an improvement, requiring significantly fewer memory cycles to make its data available to the programmer.

The implementation technique for the GMT clock was influenced by the existing configuration of the first IBM 360/75 computer transferred to JPL. It included a custom-feature modification, an interval timer, which satisfied all the Mark IIIA requirements but one—the number of lines for the GMT day limited the day of the year to 39.

To take advantage of the large investment represented by the interval timer feature, a second modification was added. This increased the number of lines for the GMT day to 10, allowing the full range of 366 days. Both modifications were added to the second IBM 360/75 computer to provide the capabilities described below.

II. Timer

The GMT timer is a real-time clock that specifies Greenwich Mean Time. The clock is composed of two parts: (1) GMT expressed in days, hours, minutes, and seconds in BCD format as received from the SFOF time reference, and (2) the fractional part of a second in binary format (to 10-μs resolution). The central processing unit (CPU) may sample the GMT (including the fractional part) whenever the GMT is valid. The fractional part is incremented at a 100-kpps rate from the time reference and is reset to *one* every second by a 1-pps signal from the time reference. The 1-pps signal is also used to start a blocking pulse in the CPU which inhibits the GMT from being sampled while the GMT is changing. Figure 1 shows the double word (64-bit) format of the GMT clock.
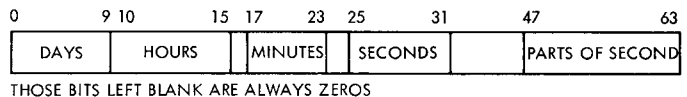

Fig. 1. GMT clock word format

The interval timer is a one-word, 32-bit, binary register that is decremented at a 100-kpps rate by a signal from the time reference or from an internal 100-kpps source. The interval timer runs continually and requests an external interrupt every time it changes from all *zeros* to all *ones*. In addition, the interval timer may be loaded by a load timer instruction, providing the ability to request external interrupts at predetermined times. The timer contents may be stored by a store timer instruction.

III. One-Second Interrupt

A 1-pps signal is furnished to the CPU from the time reference, providing an external interrupt every second, under program control.

IV. Interface

The first word of the GMT clock is obtained by sensing the state of 30 lines from the time reference. The 30 lines are used as follows:

2 lines	hundreds of days of the year
4 lines	tens of days of the year
4 lines	units of days of the year
2 lines	tens of hours
4 lines	units of hours
3 lines	tens of minutes
4 lines	units of minutes
3 lines	tens of seconds
4 lines	units of seconds

The second word of the GMT clock represents the contents of a 17-bit binary counter that is incremented by a 100-kpps signal from the time reference. The 15 high-order bits of this word are always *zeros*.

The 30 lines of GMT from the time reference will be updated once each second. Immediately prior to the GMT being updated, a 1-pps signal (pulse width of 100 ms) is received from the time reference. This signal will lead the change of the GMT lines by 0.75 μs (nominal).

The 1-pps signal blocks the model 75 CPU from sampling the GMT lines while the GMT is changing. This is done by initiating a 10.0-μs delay. During this 10.0-μs period, the CPU is inhibited from performing a store timer 1 (store GMT) instruction. The time reference should start changing the GMT lines 0.75 μs from the leading
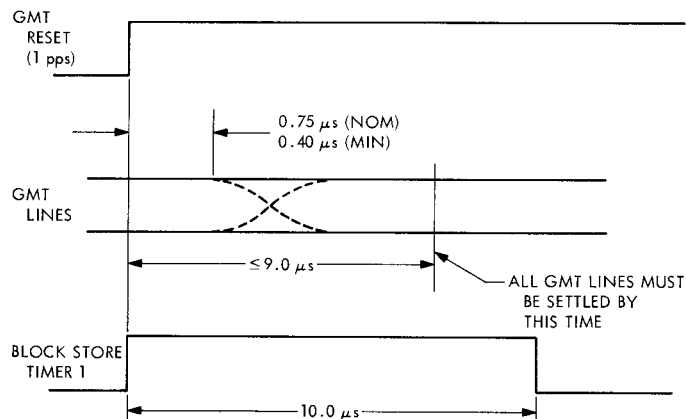

Fig. 2. Timing relationship

edge of the 1-pps signal. Figure 2 shows the timing relationship between the 1-pps reset pulse and the GMT lines.

The 32-bit interval timer is decremented by *one* every 10 μs by a 100-kpps signal (pulse width = 2.5 μs) from the time reference or from an internal oscillator; this is selectable by switch setting. Facilities are also provided to disable the interval timer so that it will not step.

The interval timer will request an external interrupt when it rolls over from *zeros* to *ones*. A bit in the program status word will enable this interrupt. The timer interrupt is also requested if a load timer instruction is issued when the timer is disabled (by switch setting) or is in the maintenance mode.

An external interrupt is requested at a rate of 1-pps (pulse width of 100 ms) by a signal from the time reference. A bit in the program status word will enable this interrupt.

V. Conclusion

With the inclusion of the modified features in the IBM 360/75, GMT and a variety of timing and interrupt techniques are available to programmers. Since the lines are sampled only when requested versus loading a core location every millisecond, few memory cycles are required. Using IBM designs also allows continued customer engineer support for the CPU. This approach is technically feasible for other IBM 360 models, in particular models 65, 67, and 85.

Reference

1. Stiver, R. A., "Mark IIIA IBM 360/75 Computer Configuration," in *The Deep Space Network*, Space Programs Summary 37-66, Vol. II, pp. 71–75. Jet Propulsion Laboratory, Pasadena, Calif., Nov. 30, 1970.