Improved Frequency Dividers

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I. Introduction

Frequency dividers with improved phase stability were recently developed for use in the hydrogen maser frequency standard. The commonly used methods of frequency division were found to have excessive phase noise and long-term drift and would seriously degrade the inherent stability of the frequency standard.

The improved frequency dividers consist of a digital divider in parallel with an analog gate. The analog gate is opened by the digital divider allowing the input frequency to pass through the gate at the exact time and interval to achieve the desired division.

II. Configuration

A block diagram of the improved frequency divider is shown in Fig. 1.

The first amplifier, A1, is an isolation amplifier which provides a constant 50-Ω input impedance and a voltage gain of approximately seven. The output of A1 is im-
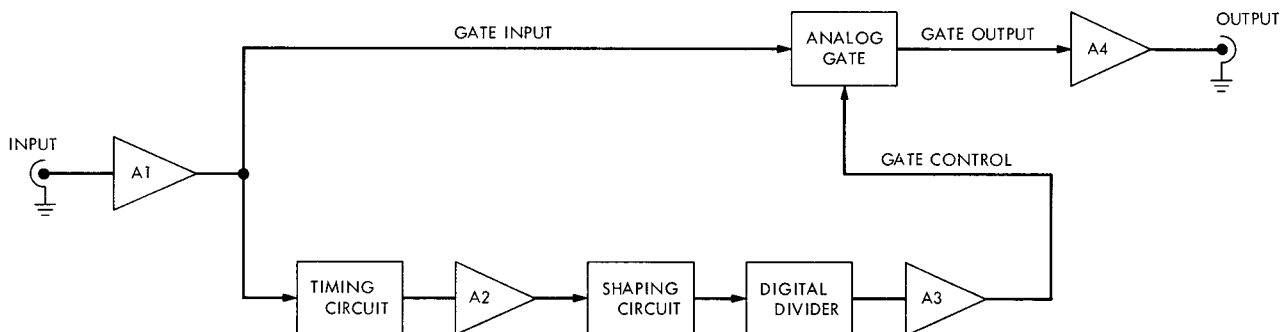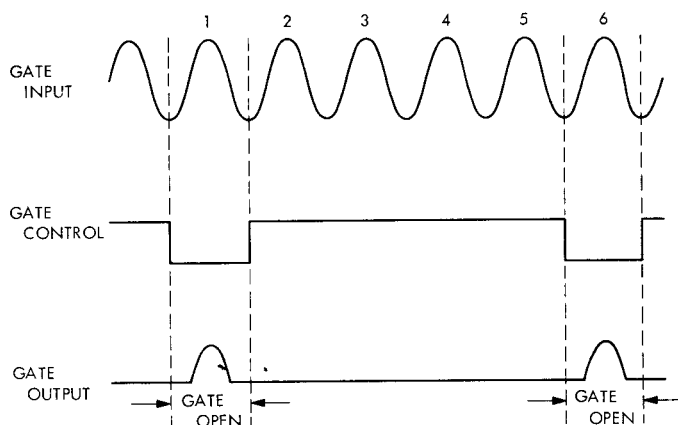

Fig. 1. Frequency divider block diagram

Fig. 2. Divide-by-5 analog gate waveforms

Fig. 3. Comparison of phase noise

pressed on an analog gate which is opened by a digital signal to allow one half cycle of the signal from A1 to pass through the gate every nth cycle, where n is the division ratio.

The clock for the digital divider is taken from the output of A1 and goes through a timing circuit which is used to set the time relationship between the analog signal and the digital signal at the analog gate (Fig. 2). The signal is then amplified by A2 and shaped properly to drive the digital divider. The output of the digital divider is one pulse every nth cycle of the input frequency and has a pulse width of one cycle, as shown in Fig. 2.

The output pulse from the digital divider goes through an inverting amplifier, A3, which drives the analog gate. The gate is opened and allows the positive part of the input signal to pass through. This results in a signal at the input of the tuned amplifier, A4, which is the positive half sine wave every nth cycle of the input signal (Fig. 2). The output of the tuned amplifier drives a distribution amplifier which is not shown.

III. Operation

The phase noise of the improved frequency dividers was compared to several other modules presently in use. An improvement in phase noise of nearly two orders of magnitude over a typical frequency divider now in use is indicated by the graph of Fig. 3. This graph shows the single sideband phase noise density relative to the carrier as a function of frequency for the modules which were compared. The measurement method is described in Ref. 1.
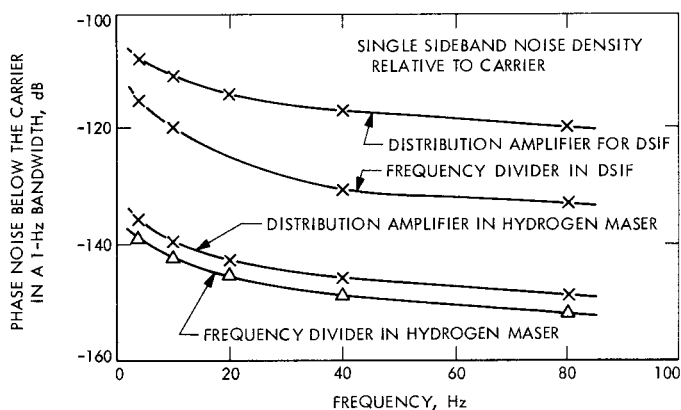
The bandwidth of the prototype is approximately 10%. Much wider bandwidths could be achieved since it is limited only by the timing circuit and the tank circuit of the tuned amplifier, A4. Other test results are shown in Table 1.

This type of divider does not have the problems associated with more commonly used designs, such as spurious modes of operation, unreliability, sensitivity to power supply variations and temperature effects.

This design utilizes the reliability of a digital divider but eliminates the phase noise inherent in digital circuitry. A considerable improvement in frequency dividers is indicated by the test results, which show substantially better phase stability, reliability, temperature stability, reproducibility, bandwidth capability, and insensitivity to power supply variations.

Table 1. Test results

Measurement	Nominal	Measured
Input Z	50 Ω	$<$1.1:1 VSWR
Output Z	50 Ω	$<$1.1:1 VSWR
Bandwidth	See text	10%
Phase shift with temperature	—	$\pm$10 from 0 to 50°C
Amplitude variation with temperature	—	$<$0.5 dB from 0° to 50°C
Distortion	$<$5% THD	$<$3% THD
Power supply	$\pm$15 and $+$5 V	
THD = total harmonic distortion.		

Reference

1. Meyer, R., and Sward, A., "Frequency Generation and Control: The Measurement of Phase Jitter," in *The Deep Space Network*, Space Programs Summary 37-64, Vol. II, pp. 55–58. Jet Propulsion Laboratory, Pasadena, Calif., Aug. 31, 1970.