GCF High-Speed Data System Design and Implementation for 1971–1972

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The Deep Space Network (DSN) Ground Communications Facility (GCF) high-speed data system capabilities were significantly upgraded to meet the 1971–1972 era requirements. In general, those requirements doubled the data transmission rate to 4800 bps, added block demultiplexing at the remote stations, provided for block synchronous outbound transmission from the SFOF, and provided positive labeling of error-free blocks. This article discusses the major detail design problems encountered in implementing these requirements.

I. Introduction

This article discusses the hardware design and implementation problems in upgrading the Ground Communications Facility (GCF) High-Speed Data System (HSS) capabilities to meet the new functional design requirements set forth in Ref. 1 for the 1971–1972 era. Numerous design problems were encountered from the initial systems design conceptual stage to the detailed hardware and wiring implementation of the various assemblies. The problems concerning the general system design concepts are discussed in Ref. 2. The major detail design problems encountered with implementing the various new functions in the high-speed data assemblies (HSDAs) of the HSS are the subjects of this article.

The major tasks and new functional design requirements, to provide the DSN support required of the GCF HSS in the 1971–1972 era, are discussed in the sections that follow. Figure 1 depicts the GCF HSS and the new interface capabilities as discussed in this article.

II. Design and Implementation

A. Upgrading of the Data Transmission Rate From 2400 bps to 4800 bps

Throughout the DSN/GCF, the HSD circuit interface with the NASA Communications Network (NASCOM) is on the digital side of the data transmission equipment which NASCOM provides. In this case, NASCOM provided new Western Electric Co. (WECo) 203A Data Sets, which operate at the 4800-bps speed.

It was soon evident that the replacement of the 205B (2400 bps data set) with the new 203A would significantly impact the mechanical and electrical design of the HSDAs. Additionally, the operation of the HSS and

the data flow control aspect (affecting the data source/sink HSS users) would also be significantly affected.

The 203A Data Sets have a timed "training"[1] sequence feature to compensate for imperfect amplitude and envelope delay response of the line.

The timed training sequence, after its initiation by manual or automatic means, is controlled by the transmitter.

The Data Set Request to Send (RS) signal control lead is wired in the ON condition in all GCF HSD assemblies. Therefore, the initial training start time after circuit connection is controlled by the remote receiver. After the initial training, the receiver will signal for a "retrain"[2] automatically when it detects a loss of carrier which exceeds an allowable hold-over time, or when the signal quality falls below threshold. The receiver, after a preset time delay, will signal through the associated transmitter by phase shifting an auxiliary signal to the remote data set. The phase shift will immediately cause a momentary OFF interrupt of the remote transmitter RS signal and that transmitter will go through the timed training sequence; thereby the automatic retrain of the troubled side of the full duplex (FDX) circuit is completed. The other receiver would signal for and receive a retrain in the same manner over its own signaling and retrain loop.

The transmitter, whose RS signal lead has been momentarily turned OFF to initiate a training sequence, will turn OFF the Clear to Send (CS) signal to its associated data source which stops the flow of data from that source immediately and *without any warning*. At the conclusion of the training sequence (nominally 7.9 sec), the CS signal will be turned back ON. This clearly demonstrates that the 203A CS signal can be affected by the remote receiver—automatically—and without any warning. The GCF HSS, due to this new data set feature, then placed this additional design constraint on all HSS users. It was essential that all users reexamine their data flow control mechanisms and consider the probability of backlogging due to this added "system" control factor.

[1]Training: Five different time sequenced signal modes are automatically sent by the transmitter to permit the remote receivers' automatic equalization and timing synchronization features to fine adjust prior to transmission of data. The training period for the data sets used is a nominal 7.9 sec.

[2]Retrain: Same as training, but occurs after initial startup (training).

In order to provide the HSDA operator with the necessary indicators and controls to monitor the data set performance, and to manually initiate and observe the time-sequenced training events, a Data Set Control Panel was designed. This new Data Set Control Panel provides a momentary action indicator switch for interrupting the RS signal from normal ON to OFF. An ON/OFF indicator switch was included to inhibit the Automatic Retrain feature if desired, and ON/OFF indicators were provided for the CS, Data Set Ready (DSR), Carrier Off Delayed (COD), and Signal Quality (SQ) signals.

The last, but not least, design impact was the mechanical packaging problem of mounting the 203A Data Set in a DSS Comm Equipment Subsystem (DCES) HSDA. The DSIF standard rack design provides for 48-cm (19 in.) rack mounting space only; the 203A requires 58-cm (23-in.) mounting space. The 203A could not be operated in an "on-end" position. By special agreement with the DSIF, a deviation from the standard rack design was granted; and a new GCF-DCES rack was designed to accommodate two data sets in the bottom half. The top half was designed for standard 48-cm equipment mounting to accommodate the new BDXR equipment units.

B. Addition of BDXRs on Both the Prime and Backup Channels at CTA 21 and Each DSS Except DSS 13

(The GCF high-speed data block demultiplexer design and implementation is discussed in Ref. 3.)

The BDXR equipment is used in the DCES HSDAs located at CTA 21 and the DSSs. Previous to this upgrade to meet the 1971-1972 era requirements, the HSDA signal interface with the on-site computers (OSCs) for both the Transmit (TX) and Receive (RX) data functions was through the BMXRs.

Two BDXRs (one each for the prime and backup channels) along with their associated BDXR patch and test panel were mounted in the top half of the new rack as previously mentioned. The *receive* data and clock signal leads from the error detection decoders were rerouted to the BDXRs in the new rack.

The BDXRs, described in Ref. 3, operate in conjunction with the BDXR patch and test panel which is designed to provide ready access to all signal leads for monitoring, test, and substituting of through connections via patchcords. Only the prime channel BDXR

ports are cabled through from the BDXR patch and test panel for interface to the OSCs. The backup channel *receive* equipment can be substituted for the prime channel by application of patchcords. The patchcord method was a "value engineering" judgment so that the GCF mean time to restore requirement could be met in the simplest manner.

Value engineering considerations also reduced the functions that the BDXR was to perform. Since adequate HSDA self-test capability existed elsewhere, its need in the BDXR was not mandatory. However, it was required that the BDXR contain a simple test mode (front panel accessible) to check the programmed data block routing codes.

C. Provide for Block Synchronous Outbound HSD via BMXRs From the SFOF Comm Terminal Subsystem (SCTS) HSDA

The design of the BMXRs, although originally designed together with the BMXR switch and test panel (S&TP) for exclusive use in the DCES HSDA, was unchanged for its application in the SCTS HSDA. However, a new BMXR patch and test panel was designed to eliminate the BMXR "select" switch function of the S&TP but provide the required "test/operate" switch function. The new patch and test panel accommodates all four ports of three BMXRs providing test, monitor, and patch jacks; and the required "test/operate" switch and switch function for each port.

Past experience in interfacing with the SFOF had shown that various mission-dependent requirements occur from time to time to support Complementary Analysis Teams (CATs) with HS capability. Also, as the GCF and DSN monitoring systems become more sophisticated, the HSDA design must follow these changes.

The SCTS HSDA interfacing schemes are therefore designed to accommodate relatively large numbers of receive-data and monitor signal lead interfaces, along with the four transmit-data source interfaces provided through each BMXR.

A new high-speed data interface module (HIM) was designed. The HIM provides an isolated and controllable point of flexible interconnection between all HSDA signal leads and the data source/sinks. Inputs and outputs of the line driving and distribution amplifiers are also interconnected in the HIM.

It was necessary to insure that the electrical characteristics specified in EIA Standard RS 232-C were met at the points of interface. To assure RS 232-C requirements would be met, all interface cables used were designed and provided as part of the HSDA. All interfacing cables are therefore under centralized design control, and the HSDA wire line interface is remoted to the connector panel in the data source/sink users cabinet.

D. Provide Positive Labeling of Error-Free Blocks Received Throughout the GCF

The error detection decoders, as originally designed, labeled only those blocks that were received with errors detected while the decoder was in the lock mode (decoder "invalid"). The error status bits of error laden blocks received while in the non-lock "search" mode were unchanged and appeared to the data sink the same as error-free blocks.

The advent of the DSN multi-mission command system required positive error-free transmission of the command data from the SFOF to the DSSs through the GCF HSS. The decision was made that the decoder would be modified to label only those blocks received error-free. The DSIF computers, when operating under the DSN multi-mission command system mode, would be required to examine each block received for the positive error-free label. The DSIF computer would call for retransmissions of those blocks not containing the positive label until all command data blocks were received error-free.

Modification kits and instructions were sent to all field locations where the modification was accomplished by field personnel.

E. Provide Three Channels of HSD Equipment to the Simulation Center (SIMCEN), Each Capable of Independent Operation

The DCES HSDA that was installed in the SIMCEN was configured and wired the same as those provided at the DSSs, but was installed in standard SFOF-type cabinets. The DCES HSDA provided in these cabinets for use with the SIMCEN took on a unique appearance when rewired and reconfigured to provide simultaneous operation over three channels.

The same new BMXR patch and test panel previously described was used with the new three channel capabilities to provide three separate channel connections to the SIMCEN data source/sink interface. The cables

connecting the HSDA to the interface connector panel were provided as part of the HSDA and were of the special new design previously mentioned. Every effort was made to keep cabinet wiring changes to a minimum and all installation and modification effort was completed with the racks installed in their SIMCEN location.

The reconfiguration design and documentation effort was a sizeable task requiring new rack and wiring diagrams, a special cabling design package, and a new Operations and Maintenance Manual.

F. Provide a HSD Regeneration Assembly (HSRA) at the Area Comm Terminal (ACT) Located at the Goldstone Deep Space Communications Complex (DSCC)

The Area Comm Terminal Subsystem (ACTS) located at the Goldstone DSCC previously did not contain any HSD equipment. With respect to the HSS, the ACT was simply the point of interconnect where off-complex HSD circuits were interconnected to HSD circuits from DSSs 11, 12, and 14. To satisfy the flexible interconnect requirements normally attributed to such a trunking center, the transmission characteristics of each data circuit should, as a minimum, meet equivalent American Telephone and Telegraph Co. C-2 specifications. A specific long-term error rate can be expected when operating 203A data sets over a single C-2 grade circuit: if two C-2 grade circuits are interconnected with a 203A regenerator, the error rate can be expected to increase by a factor of two. Therefore, an ACTS HSRA was installed at the ACT. The HSRA is sized to regenerate, simultaneously, three full duplex HSD circuits. Additionally, landline (cable) HSD circuits interconnecting DSS 14 and DSS 11 to the ACT were equipped with custom-designed line equalization equipment to meet the C-2 specifications.

III. Summary

The effects of upgrading the GCF HSS to meet the requirements set forth for the 1971–1972 era are summarized as follows:

(1) The number of HSDAs was increased by one with the new installation of the HSRA at the Goldstone DSCC ACT.

(2) The DCES HSDAs equipped at CTA 21 and all DSSs except DSS 13 are fully and identically equipped with prime and backup channel equipment, including the new Block Demultiplexer equipment.

(3) The DCES HSDA equipped at the DSN SIMCEN is now a unique three-channel assembly. The three channels are configured for independent use through a new BMXR patch and test panel. This is the only DCES HSDA not equipped with the block demultiplexer capability.

(4) The SCTS HSDA has been changed significantly. Not only are the additional DSN-GCF interface requirements discussed herein accommodated, but the new NASCOM West Coast Switching Center requirements are also integrated.

(5) More details on the various types of HSDAs appear in succeeding articles.[3]

[3]For related articles covering more details on the HSDAs, see articles by Yinger, Brunder, and Rothrock in this issue.

References

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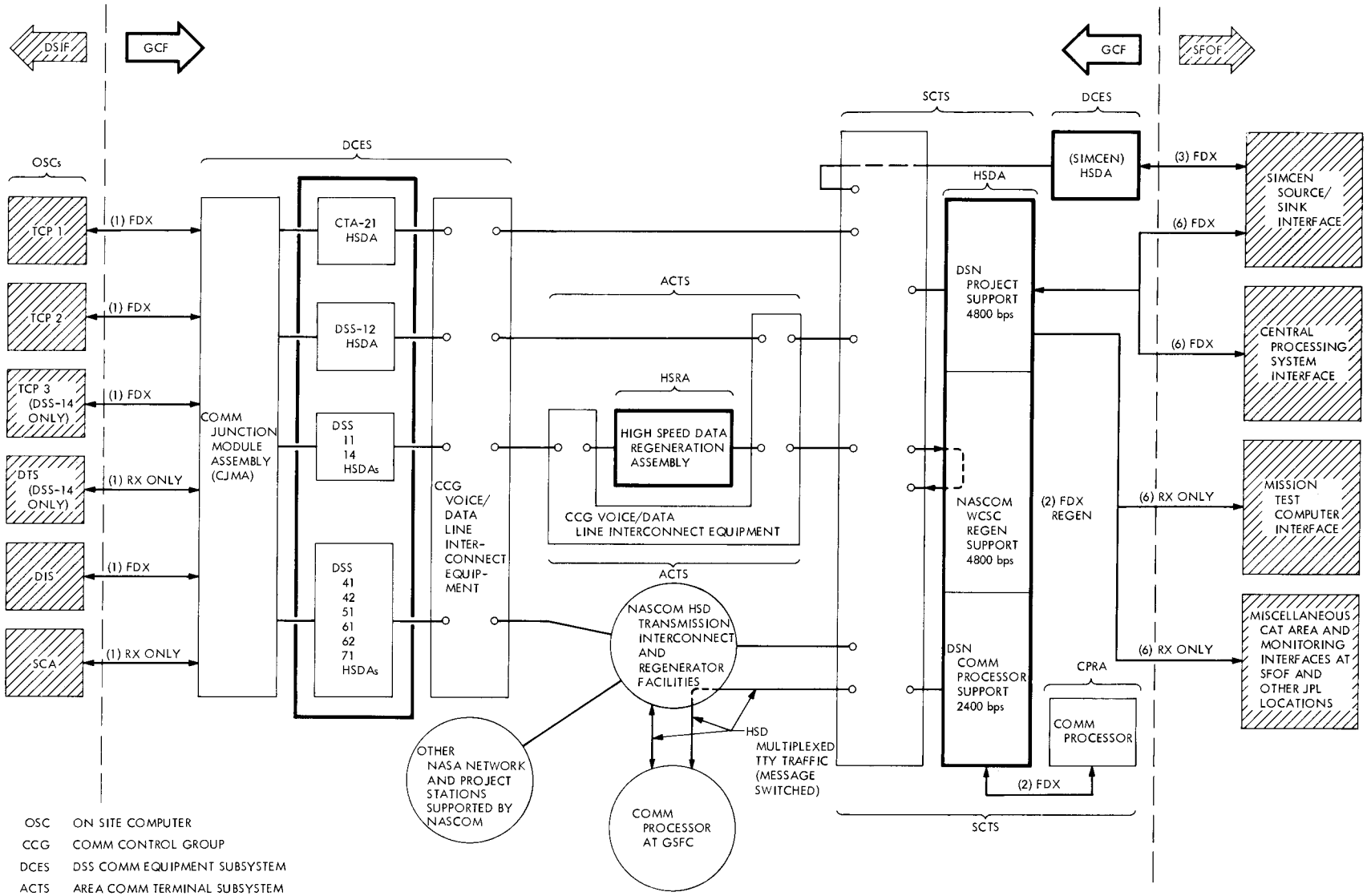

OSC	ON SITE COMPUTER
CCG	COMM CONTROL GROUP
DCES	DSS COMM EQUIPMENT SUBSYSTEM
ACTS	AREA COMM TERMINAL SUBSYSTEM
SCTS	SFOF COMM TERMINAL SUBSYSTEM
CPRA	COMM PROCESSOR ASSEMBLY
WCSC	WEST COAST SWITCHING CENTER
HSDA	HIGH SPEED DATA ASSEMBLY
CAT	COMPLIMENTARY ANALYSIS AREA
CTA-21	COMPATIBILITY TEST AREA No. 21
FDX	FULL DUPLEX
RX	RECEIVE

Fig. 1. DSN–GCF high-speed data system general interfaces 1971–1972 configuration