GCF SFOF Communications Terminal Subsystem High-Speed Data Assembly

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New capabilities and equipment have been incorporated into the Space Flight Operations Facility Communications Terminal subsystem high-speed data assembly as a result of the 1970–1971 upgrade in support of the Deep Space Network. The distinct capabilities of the high-speed data assembly are discussed and the new 4800-bps high-speed data circuits and equipment are described on a functional level.

I. Introduction

The Space Flight Operations Facility Communications Terminal Subsystem (SCTS) high-speed data assembly (HSDA) is a full duplex data communication terminal that provides the necessary interface between the SFOF computers and the voice frequency data channels of the intersite transmission subsystem (ITS). Reference 1 provides information concerning the general configuration of the GCF 1971–1972 high-speed system. Reference 2 discusses equipment presently in operation in the SCTS high-speed data assembly.

The SCTS HSDA consists of 17 racks of equipment arranged to transmit, receive, process, test, monitor, switch, and distribute high-speed data.

The high-speed digital data is transmitted to and from three distinct entities, in audio form, over properly conditioned voice-grade circuits. The three external facilities connected to the SCTS high-speed data assembly are:

(1) The deep space station communications equipment subsystems (DCES). The transmission path utilized between the deep space stations and the SCTS high-speed data assembly is via the intersite transmission subsystem (ITS).

(2) Non-DSN project dependent locations. The transmission paths are GCF National Aeronautics and Space Administration Communications Network (NASCOM) circuits.

(3) Goddard Space Flight Center (GSFC) communications processor. NASCOM circuits and the SCTS high-speed data assembly interconnect the JPL and GSFC communications processors. Reference 3 discusses the functional capabilities of the JPL communications processor.

The intent of this article is to describe the general functional capabilities of the SCTS high-speed data assembly with particular emphasis on the new equipment and functional capabilities that have been incorporated into the assembly during the 1970–1971 upgrade.

II. SCTS High-Speed Data Assembly Configuration

A. 4800-bps High-Speed Data Circuits

Figure 1 depicts the general configuration and interface relationships of the 4800-bps HSD circuits used in support of the DSN. The upgrade of the data transmission rate from 2400 to 4800 bps is discussed in "GCF High-Speed Data System Design and Implementation," by R. H. Evans in this issue. The six full-duplex circuits provided by the HSD assembly are described below:

1. Transmit path. Each of the six transmit circuits can accept digital data from up to four different SFOF computers (data sources). All data sources are interfaced at the new HSD interface module (HIM).

a. HSD interface module. The HIM is JPL-designed equipment providing a highly flexible isolated distribution point for both HSD assembly data source and data sink signals. The HIM utilizes standardized connector panels, mounted in two racks, employing feed-through poke-home type Bendix connectors. The HIM is designed to accommodate many interface configurations due to the changing nature of the SCTS high-speed data assembly interface requirements.

b. Block multiplexer patch and test panel. From the HIM, the transmit signals are distributed to the new block multiplexer (BMXR) patch and test panel where connector ports can accommodate up to four data sources for each HSD circuit. Each panel provides for three HSD circuits. The panel also accesses the signals to patch, monitor and test jacks. A test/operate switch is provided to loop, in the "test" position, test signals through the BMXR patch and test panel and back to the BMXR, thus making the panel act as a data source for testing purposes. In the "operate" position the data source signals proceed to the BMXR input ports.

c. Block multiplexer. The BMXR permits up to four SFOF computers to time-share the transmit side of HSD line. This is accomplished on a priority basis, by multiplexing the block formatted data generated by the SFOF computers. When the SFOF computers are all idle the BMXR generates filler blocks to provide synchronous transmission on the HSD circuit.

The block formatted digital signals are transmitted to the encoder through a dc patch rack which provides signal access to patch, monitor and test jack facilities.

d. Encoder. The encoder performs the data block encoding for the error detection/encoding decoding (ED/ED) scheme. The ED/ED scheme provides for a positive method of monitoring the transmission of data between end terminals at the GCF.

The encoder affixes a 36-bit error detection pattern to the end of each data block before it is transmitted to the data set. The first 3 bits of the 36-bit pattern are an error status code and are always transmitted as binary zeros. The last 33 bits comprise a special coded polynomial derived from the encoding process.

e. Data set. The 203A data set is a Western Electric Co. full duplex unit. It converts the serial binary block-formatted data from the encoder into audio signals appropriate for the transmission circuit. Transmission is at a synchronous four-level amplitude modulated 4800-bps rate over four-wire C2-conditioned circuits. During the upgrade, 203A data sets replaced older 2400-bps 205B data sets in all six HSD channels.

f. Data set control panel. The JPL-designed data set control panel operates with the 203A data set. It provides visual monitoring of the operating status of the data set by displaying all the control signals at the data set digital interface. It also provides a switch to manually control the retrain initiation on the data circuit as described by Evans in this issue.

g. Attenuator panel. The audio signals are transmitted from the data set to a JPL-designed attenuator panel provided for use with both the transmit and receive sides of the data set audio circuit.

The attenuator panel contains pads that can accommodate plug-in resistors of variable values. Resistors thus can be selected to set the level of signal attenuation of the data set audio interface. The characteristics of the transmission path determine the signal levels to be selected.

The audio signals are then routed via audio patch, monitor and test jack facilities installed in a separate rack in the HSD assembly. Leaving the HSD assembly the signals are cabled to the audio switch assembly and are thence routed via the circuit distribution assembly (CDA) to the intersite transmission subsystem.

2. *Receive path.* The HSD audio signals received at the SFOF from an external location are routed to the audio switch assembly in the SFOF. The signals then enter the SCTS high-speed data assembly at the audio patch rack. Here the signals are accessible via patch, monitor and test jacks. The audio signals appear at the

203A data set after undergoing signal level adjustment in the attenuator panel discussed earlier in this article.

a. Data set. The 203A data set receiver demodulates, amplifies and automatically equalizes the incoming audio signal to compensate for the amplitude and delay distortions of the transmission facilities. The signal is then applied to an analog-to-digital converter, the output of which is transmitted to the decoder via dc patch, monitoring and test facilities in the dc patch rack.

b. Decoder. The decoder monitors the HSD received from the data set and performs a continuous decoding and error detection function within the error detection/encoding decoding scheme.

The decoder examines the complete data block, including the special 36-bit error detection pattern at the end of each block to determine whether or not the data block is error free. An error free block will pass the decoding process. This, together with sync pattern recognition, is used to validate the data block immediately prior to its output to the BMXR via dc jack access facilities.

If the decoder detects an invalid block (one containing errors), or cannot correctly identify the sync pattern, it performs a process obtaining a positive error status indication, discussed by Evans in this issue by changing the condition of the 3-bit error status code from binary "zeros" to binary "ones."

The decoder also informs the search alarm unit as to whether it recognizes a valid or invalid condition.

c. Search alarm unit. The search alarm unit was designed by JPL for use in the 1970–1971 upgrade to audibly and visually warn operations personnel of a loss of valid data or sync pattern recognition in the decoders. The loss must exceed a predetermined 5-sec time period while the decoder is in a "search" mode for an alarm condition to be initiated. The unit presently monitors all six SCTS HSDS high-speed data circuits simultaneously.

d. Block multiplexer. The BMXR receives the high-speed digital data from the decoder and drives four outputs, in parallel, through the BMXR patch and test panel jacks to the HSD interface module distribution interface.

e. HSD interface module. The HSD interface module distributes the received data, in parallel, to the central processing system, mission test computer, and the Simulation Center. A fourth parallel output is distributed to the line driver amplifier (LDA) rack.

f. Line driver amplifiers. The line driver amplifiers receive the digital input signals and drive three parallel output lines for each signal.

The LDA rack also has patch panels with patch, monitor and test jacks accessing each LDA input and output signal. The outputs are transmitted back to the HSD interface module where they are distributed to the GCF monitor areas, mission complimentary analysis team (CAT) areas, and to the teletype (TTY) character generators.

g. TTY character generator. The TTY character generator rack contains six on-line TTY character generators, one operational spare and related control panels, power supplies and test equipment.

Specific monitor signals are extended from the BMXR to the character generator. The character generator examines the status of the monitored signals for each data block and outputs one or two 8-level teletype characters to the communications processor. One 8-level character contains information indicating receipt of a valid data block, or detection of an invalid data block. Two 8-level characters, when sent, indicate degradation of the carrier and the loss of decoder block synchronization.

The JPL Communications Processor utilizes these data to drive a real-time display of high-speed data status. This display is provided on a digital TV format, via the SFOF internal communication subsystem (SICS), throughout the SFOF.

B. 4800-bps Full-Duplex Data Regeneration Circuits

Figure 2 represents the SCTS HSD assembly data terminal facilities provided for 4800-bps data regeneration of NASCOM data, in support of the West Coast Switching Center.

The facility consists of four Western Electric Co. 203A data sets arranged to provide two full-duplex (simultaneous two-way transmission of data) regeneration circuits. An additional 203A data set is provided as spare and may be substituted in place of a failed data set by the use of patchcords.

Data set control panels are also provided to display the operating status of each of the regeneration data sets and provide the means to select the receive timing signal from one data set to be used as the externally supplied transmit timing signal of the other data set.

The attenuator panel, previously discussed in this article, permits level adjustment of the audio transmit and receive signals at the data set audio (line) interface.

The dc and audio signals are also accessible at jack facilities to provide patch, monitor and test capability.

C. 2400-bps High-Speed Data Circuits

Three (including one spare) 2400-bps Western Electric Co. 205B data sets serve as data terminal facilities for high speed data circuits carrying multiplexed teletype data between the GSFC Communications Processor and the JPL Communications Processor.

At JPL, the digital data is transmitted through selected HSD line transfer relay paths to communication line terminals in the communications processor assembly.

The relays are controlled by a transfer switch panel that can select either the on-line or off-line status of each HSD data circuit.

III. Summary

The 1970–1971 update of the SCTS high-speed data assembly provides an equipment configuration having the following capabilities:

(1) Six 4800-bps HSD circuits serving the DSN.

(2) Two 4800-bps full-duplex data regeneration circuits serving NASCOM West Coast Switching Center requirements.

(3) Three (including one spare) 2400-bps HSD circuits serving the JPL communications processor.

References

1. McClure, J. P., "Ground Communications Facility Functional Design for 1971–1972," in *The Deep Space Network*, Space Programs Summary 37-66, Vol. II, pp. 99–102. Jet Propulsion Laboratory, Pasadena, Calif., Nov. 30, 1970.
2. Nightingale, D., "High Speed Data Communications for *Mariner* Mars 1969," in *The Deep Space Network*, Space Programs Summary 37-57, Vol. II, pp. 127–129. Jet Propulsion Laboratory, Pasadena, Calif., May 31, 1969.
3. Turner, J. A., "JPL Communications Processor," in *The Deep Space Network*, Space Programs Summary 37-57, Vol. II, pp. 130–134. Jet Propulsion Laboratory, Pasadena, Calif., May 31, 1969.

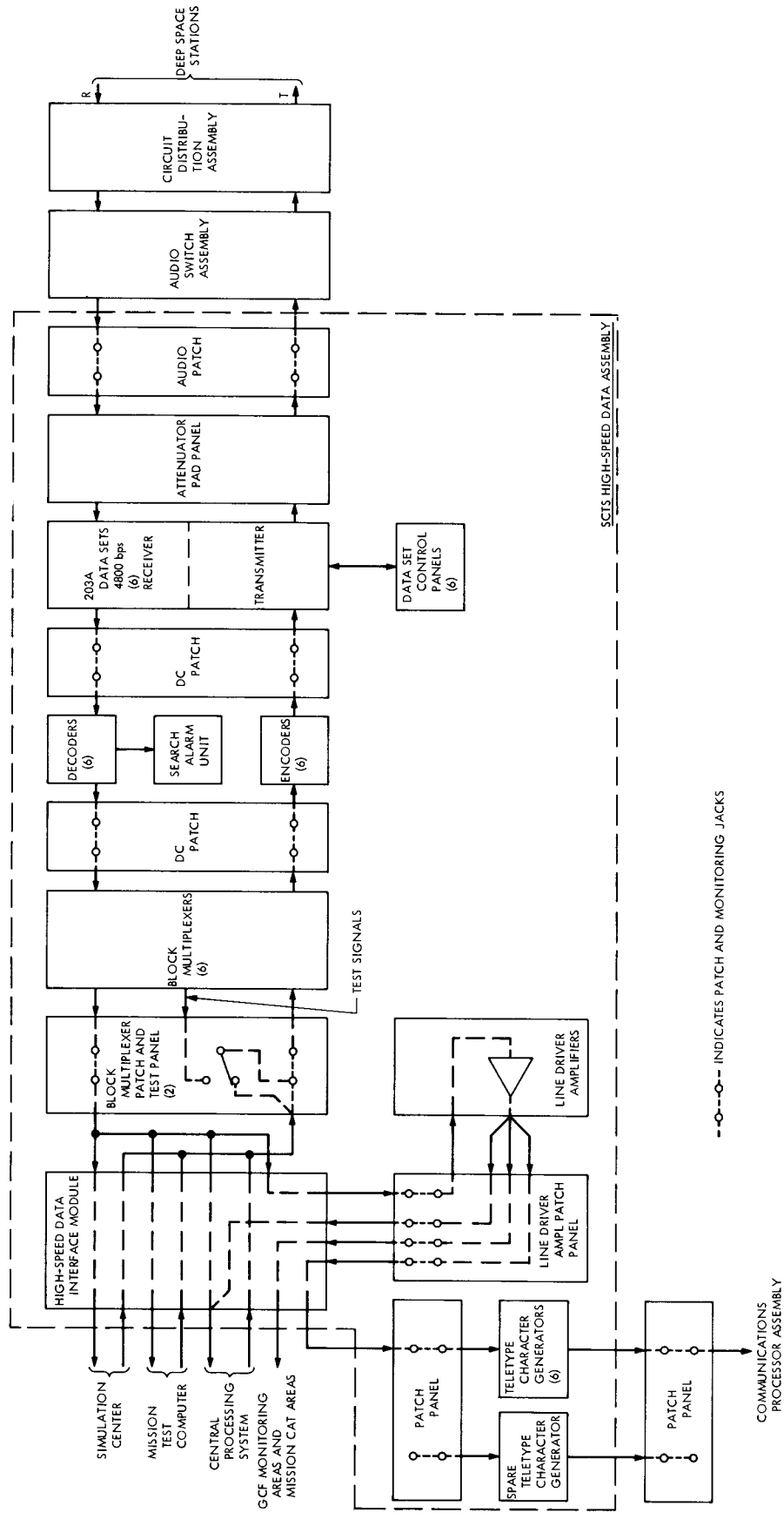

Fig. 1. SCTS HSDA 4800-bps high-speed data circuits functional block diagram

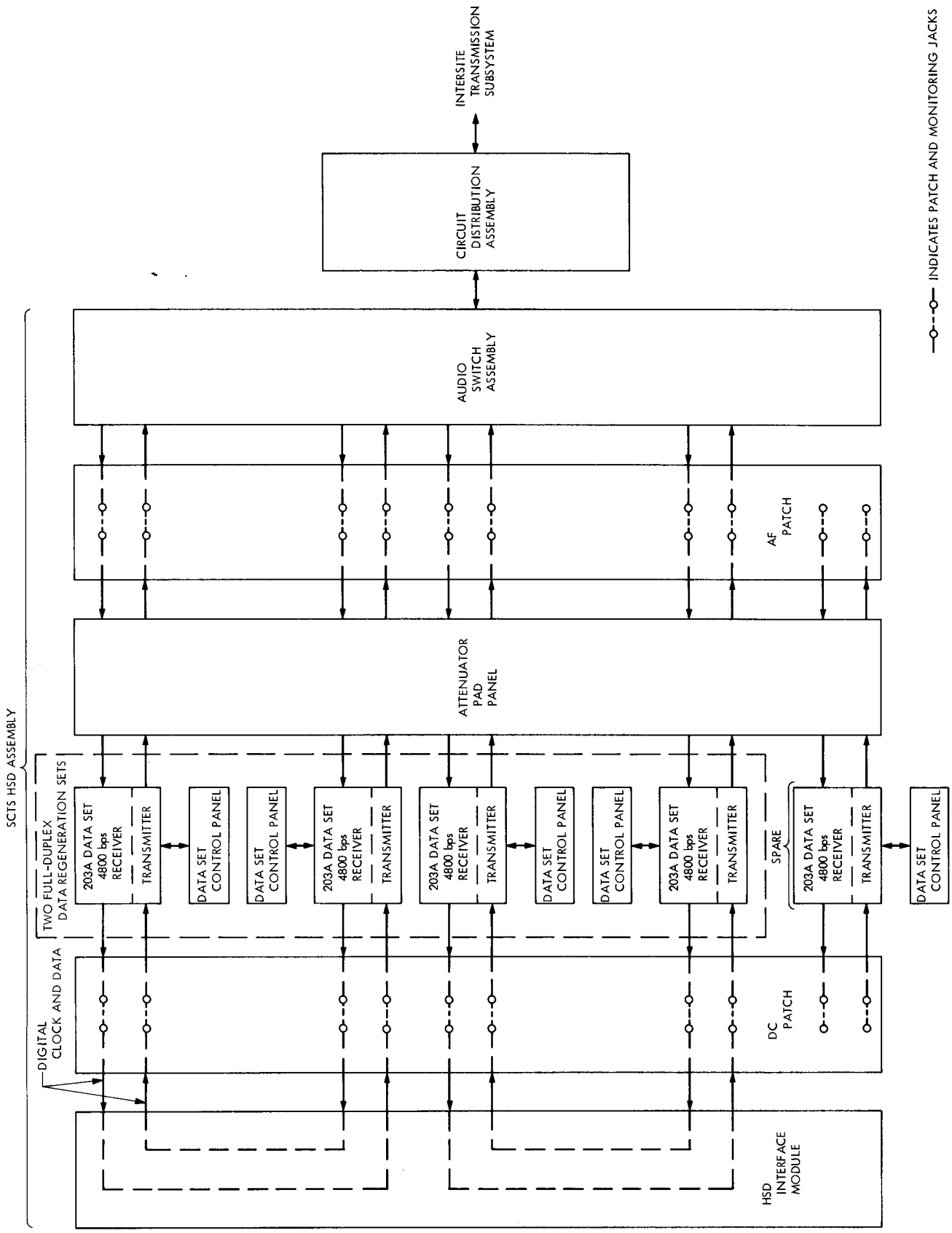

Fig. 2. SCTS HSDA 4800-bps data regeneration, functional block diagram

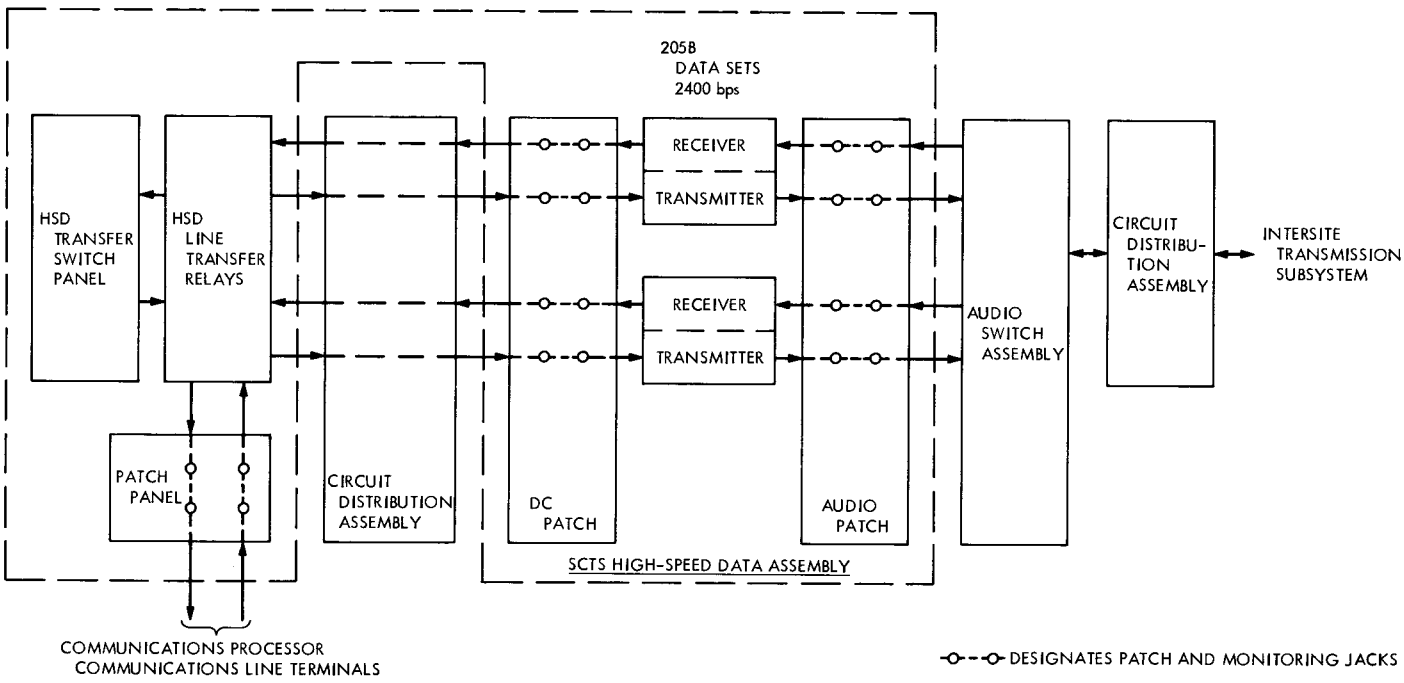

Fig. 3. SCTS HSDA 2400-bps HSD circuits functional block diagram