Efficient Implementation of a Multichannel High-Speed Correlator

T. O. Anderson
Communications Systems Research Section

The correlator presented in this article is an all-digital or sampled real-time signal processing system. It is intended for applications requiring wide bandwidth and high resolution such as measurement of spacecraft spectra or the close scrutiny of a wide bandwidth for interference to validate performance of the new dual S/X DSN system. The detection of signals in noise upon reception of radio astronomy signals is yet another application for which the present instrumentation would be useful.

I. Introduction

Earlier DSN correlators were of the serial type such as described in Refs. 1 and 2. These were generally slow but efficient as to component count. Other DSN correlators have been designed and constructed of parallel designs. These were generally very fast but their high cost often limited the number of channels. The present correlator design combines some of the cost efficiency of the serial correlator, yet it operates at the speed of the parallel designs.

The input signal is sampled at a 20-MHz rate and quantized to one bit. The correlation function involves time separation. One thousand twenty-four (1024) time lags or channels are considered. The efficiency in implementation is derived from novel design strategies coordinated with the most efficient functional components presently available. As the switching rates of the more significant bits of the accumulators decrease, the accumulators are sampled via a multiplexer, and continued accumulation is performed using a random access memory (RAM). The multiplexer, which must operate at the maximum rate, is implemented using a parallel-in–serial-out shift register. This design also separates the time base between the input and output systems.

II. Background

For an autocorrelation function, the processing operation compares a waveform with a time shift of itself. For a cross-correlation function, two different waveforms are compared. In the continuous domain,

$$\text{(Auto)} \qquad R_{xx}(\tau) = \frac{1}{T}\int_0^T x(t)\,x(t+\tau)\,dt$$

$$\text{(Cross)} \qquad R_{xy}(\tau) = \frac{1}{T}\int_0^T x(t+\tau)\,y(t)\,dt$$

In the discrete domain, the formulas become

$$R_x(r) = \frac{1}{N}\sum_{k=1}^{N} x_k x_{k+r}$$

$$R_{xy}(r) = \frac{1}{N}\sum_{k=1}^{N} x_k y_{k+r}$$

One particular system, a computer preprocessor, is described here in detail.

The present implementation derives its efficiency from novel design strategies coordinated with the most efficient functional elements presently available.

III. Basic Design

As shown in the block diagram (Fig. 1), the input signal is assumed quantized to one bit. The binary waveform is entered, at its clock rate, serially into a 1024-bit shift register. The register has an output or tap for each bit, each corresponding to one-bit time lag. Each such output from the shift register is multiplied, or added mod-2, with the reference signal. In the case of autocorrelation, the input signal is the reference signal. The output from each mod-2 circuit feeds an integrator or accumulator, each with a capacity of 2^n counts ($8 \leq n \leq 12$). The most significant bits of the accumulators are sampled via a digital multiplexer, and its single-term output feeds the low-speed accumulator system which contains the random access memory.

IV. Detail Design

Once the block diagram (Fig. 1) has been established, the design reduces to the selection of the most efficient high-speed functional components. In cases where ideal components were not available, special design measures have been considered. The most important of such special cases occurred in the design of the high-speed high-capacity accumulator.

V. Data Entry

A high-speed shift register (20–30 MHz) with one parallel output for each bit is required in the data entry section. Eight-bit 20-MHz shift registers in 16-pin packages are available from several manufacturers, 8 being a convenient binary integer for efficient physical groupings. One manufacturer also markets a 10-bit serial-in–parallel-out shift register.

VI. Multiplier

Four regular mod-2 circuits are the most that can be contained in a 14- or 16-pin package that is readily available. Six circuits could be contained in a 16-pin package if one term were common as is the present case. Such an element is, however, not yet made. Another design problem in conjunction with the mod-2 circuit is that the presently available high-speed high-capacity accumulators are not equipped with clock inhibit terms. Again only four clock gates per package are available, while six would be possible with one term common.

If one, however, examines the logic of 74H87 (shown in Fig. 2) and the mod-2 arithmetic,

$$C(A \oplus B) = AC \oplus BC$$

$$\overline{A \oplus B} = \overline{A} \oplus B = A \oplus \overline{B}$$

$$\overline{A} \oplus \overline{B} = A \oplus B$$

one finds that 74H87 will perform the combined function of mod-2 and clock gating for four channels.

VII. High-Speed Accumulator

No single package capable of accumulating at 20 MHz with a capacity of 2^{16} bits or higher is presently available. The most suitable is the dual 8-bit shift register which can be connected as a cascaded "Johnson-counter" with a total accumulator capacity of 2^8. The one package per accumulator described above will be referred to as the *high-speed accumulator*. If one would have to resort to two packages per accumulator, the complete correlator would be large in size and cost. Having accumulated up to 2^8, the switching rate of the most significant bit is reduced accordingly and continued accumulation can be performed in a more efficient manner, as will be discussed in the following.

VIII. Low-Speed Accumulator

The design of the low-speed accumulator exhibits the major novelty of this correlator design. For its description and explanation, reference is made to the right side of Fig. 1.

A multichannel low-speed accumulator may be designed using a multiplexer and a random access memory with the multiplexer and the memory being commonly ad-

dressed. Assume that the input to a low-speed accumulator channel is the most significant bit of a high-speed accumulator. This bit is sampled, via the multiplexer, and if the sample is affirmative, the count stored in the RAM is accessed, augmented, and the augmented count restored. It goes without saying that the speed of the multiplexer must be adjusted to the speed of the RAM's access–augmentation–store operation and that the number of multiplexed channels for input to one RAM must be such that all channels can be processed in the time between two events of the highest rate channel. An event in this case is the high-speed accumulator reaching full scale. The augmentation circuit is a passive parallel adder.

The event of the high-speed accumulator reaching full scale is the input to a low-speed accumulator. Detection of a high-speed accumulator full scale requires that a storage bit be set upon the transition of the most significant bit (MSB) of the accumulator from a one to a zero and that this storage bit be reset upon an affirmative sample. The design of the low-speed accumulator outlined above becomes especially attractive, because the high-speed accumulator transition detection storage bit may be located on the output side of the multiplexer in the already available RAM. A single bit in the RAM is used to store the condition of the MSB of each high-speed accumulator as detected at sample time. Upon an address, the previous condition of its MSB is accessed. If the previous condition is a *one* and the present condition a *zero, full scale* has occurred in the high-speed accumulator and its count at that address is augmented and restored. The present condition of the MSB, which is now a *zero*, is also stored.

The augmentation circuit consists of a passive parallel adder followed by a hold register. The RAM read/write control is a single term. A word is available at the output of the RAM for the duration of the read cycle which is half the clock cycle. During the read cycle the word is augmented through the passive adder. An intermediate hold register is required to hold the augmented word during the write cycle, which is the second half of a clock cycle. Reset of the intermediate hold register for one multiplexer cycle will assure that the RAM is initially cleared.

IX. Multiplexer

A number of addressable multiplexer packages, designed as 16 to 1, 10 to 1, 8 to 1 switching networks, are readily available. A large tree of such multiplexer packages exhibits a considerable propagation delay. This type of multiplexer samples the inputs sequentially. The operation of such a multiplexer requires that the input and the output, namely, the high-speed accumulators and the RAM, be operated on the same time base, or special sync circuits must be inserted between the multiplexer output and RAM input.

A simpler and more efficient multiplexer consists of a string of parallel-in–serial-out shift registers. All channels are then sampled simultaneously, and the multiplexer clock system is entirely independent from the input clock system.

This is especially important because the multiplexer and the RAM interface with the computer and operate on the computer time base.

X. Random Access Memory

Little else need be discussed about the random access memory except its size and/or grouping of packages to form the required total capacity. The memory and its associated multiplexer are dimensioned so that in the time it takes a high-speed accumulator to reach full scale, all channels are able to be sampled and updated, i.e., their content read out from memory, augmented if called for, and rewritten in memory. Popular memory sizes are 16×4, 64×4, 256×1, 1024×1 per 16-pin dual in-line package (DIP). The access time is typically 75 ns and the write-pulse width is of the same order.

XI. Speed of Operation and Component Grouping

With eight bits in the high-speed accumulator, at 20-MHz input rate, 64 channels can be multiplexed and updated in the time it takes to reach full scale. For 1024 channels, 16 such multiplex MUX/RAM entities must then be multiplexed for output. Regular sequential multiplexer packages are used for this purpose.

With nine bits in the high-speed accumulator, only eight MUX/RAM entities are required, and with ten only four, i.e., one per 256-channel chassis.

With a 12-bit accumulator, only a single RAM is required and no output MUX. RAMs are conveniently available in 1024×1, requiring one package per low-speed accumulator bit. The entire 1024 channel low-speed accumulator section with eight bits per accumulator, ex-

cepting the multiplexer, can then be implemented with only 13 packages.

XII. Packaging

The 1024-channel correlator can be packaged in four 7.6 cm (3 in.) high standard 48.3 cm (19 in.) cabinet drawers, each containing a checker-board pattern of 32×20 sixteen-pin wire-wrap DIP sockets. The detail design of the drawer may not be of any particular interest here but is described in Ref. 3.

XIII. Conclusion

An all digital design and implementation of a 1024-channel 20-MHz correlator has been presented which coordinates novel design strategies with the most efficient presently available circuit packages. Such a coordination, for example, is the high-speed accumulator which uses a dual 8-bit shift register package connected as a cascaded "Johnson counter" resulting in a counting capacity of 2^8. Another is the "true/complement" element used as a combined mod-2 input and clock inhibit gate.

The digital multiplexer, yet another coordination, uses a parallel-in–serial-out shift register. This is an especially important innovation as it assures simultaneous sampling of all channels. It also forms a partition between the input and output system so that these systems can be operated on individual and independent time basis with no other sync measures required.

The most important innovation in the correlator design presented is the low-speed accumulator design. Two very attractive design coincidences have been capitalized on. One is the requirement for an output multiplexer, which makes possible the use of a RAM for accumulation. The second is that once a multiplexer and a RAM are included in the system, the status (most significant bit) of the high-speed accumulators can most conveniently be stored in the RAM.

References

1. "Nine-Channel Autocorrelator," in *The Deep Space Instrumentation Facility*, Space Programs Summary 37-25, Vol. III, pp. 33–38. Jet Propulsion Laboratory, Pasadena, Calif., Jan. 31, 1964.
2. "Nine-Channel Autocorrelator," in *The Deep Space Instrumentation Facility*, Space Programs Summary 37-26, Vol. III, pp. 33–38. Jet Propulsion Laboratory, Pasadena, Calif., Mar. 31, 1964.
3. Anderson, T. O., and Bodkin, D., *Low Profile Drawer for Electronic Equipment*, JPL NTR-2596/NPO-11953, July 27, 1971.

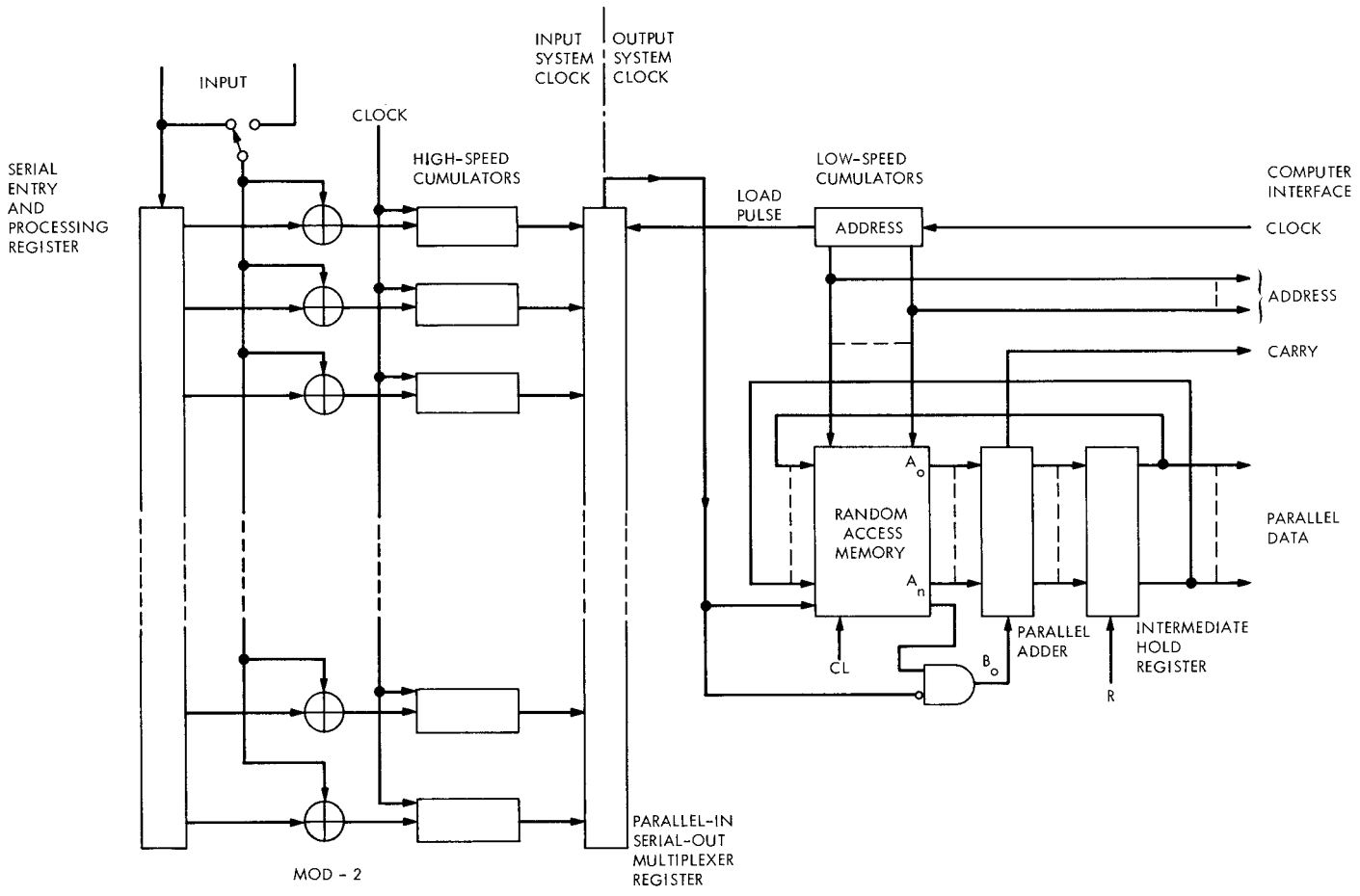

Fig. 1. Block diagram of a multichannel high-speed correlator

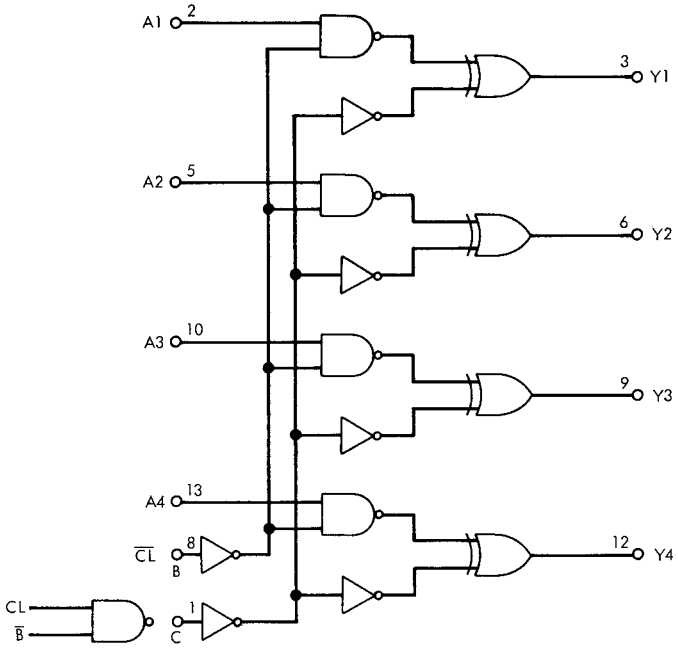

Fig. 2. Logic diagram of combined mod-2 and clock gate