CPS Sustaining Engineering

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The Sustaining Engineer Program for the Central Processing System (CPS) of the Mark IIIA Space Flight Operations Facility is based on optimizing flight support capabilities. This is being achieved by testing hardware responses during simulated critical conditions, by supporting software development, and by monitoring system performance. This article defines the major hardware/software problem areas and reports the results of studies made to resolve these problem areas.

I. Introduction

The Sustaining Engineer activities are a continuation and refinement of the results of the SFOF Mark IIIA Development. The SFOF Mark IIIA consists of two similar 360/75's (IBM computers), shared interfaces with NASA Communications Network (NASCOM) via the GCF, and extensive user areas (Ref. 1). The required capabilities necessitated the inclusion of many special devices and the use of a special operating system.

Most of the problems with the interaction of special equipment and software were anticipated but solutions were deferred since JPL Operating System (JPLOS) and the Project programs were not solidified. Sustaining Engineer efforts to resolve hardware/software problems have been concentrated in four major areas:

(1) System Recovery Facility studies.

(2) Device switching studies.

(3) Improvement of existing equipment.

(4) System refinement.

In addition, maintenance and operation of the 360/75's are observed to detect possible design and implementation errors.

II. System Recovery Capability Studies

System Recovery Facility (SRF)[1] is a part of JPLOS that attempts to recover from hardware and software errors. With the inclusion of remote devices, it was possible for

[1]System Recovery Facility is IBM's terminology for the software for this function.

a device to lose power while the rest of the system was unaffected. However, the failing device could have interacted with the Central Processing Unit (CPU) if the device was in a signal sequence with the CPU.

Initial studies simulated a power loss in a device and confirmed that the CPU is left in the WAIT state. Investigation revealed that although an interrupt was requested to clear the channel, logic was not ready within the channel to complete the operation. A design change in the logic was installed with IBM concurrence to completely clear the channel once an interrupt has been requested.

Further studies are required to determine if the SRF capabilities can be extended to include more device abnormalities. These activities are currently waiting the resolution of the device switching studies.

III. Device Switching Studies

Since the key to continuous flight support for the Projects is redundant 360/75's, the Mission Support Areas (MSAs) are connected via switches to both 360/75's. The unsynchronized transfer of a device from one 360/75 to the other can cause problems in the same manner as if the device loses power. If the device is in a signal sequence with the CPU and is switched, the CPU ends in the WAIT state.

The design change from the SRF study should also allow the channel and CPU to be cleared after switching. However, the reset initiated by honoring the interrupt request is not complete; some of the latches that should be cleared to fulfill the design of the reset are not affected. An acceptable method of resetting all the latches to clear the channel is being developed.

The incomplete reset of the channel prevents useful testing of the SRF since the problem leaves the hardware in lock, out of software control.

IV. Improvement of Existing Equipment

Existing equipment has been improved by replacing logic elements that experienced an abnormal failure rate and by correcting logic to be consistent with design specifications. A major source of system failures in the 360/75's was the core storage units. The excessive failure rate was confirmed by IBM and treated by replacing most of the logic elements. The failure rate following the replacement is about 30% of the previous rate.

A major Sustaining Engineer effort has been detecting and resolving errors in design implementation. These are usually undetected until software using instruction sequences different from the device diagnostics is executed. Most of these problems have been in the 2909-3 Asynchronous Data Channel (ADC) since it is both a new and special device containing many special subchannels. In addition, the 2909 ADC is being used with standard IBM devices in a manner not previously attempted. The following problems of this nature have been resolved.

(1) *490 input subchannel.* An *end of message* signal was generated on the next to last and last data transfers which allowed only two bytes of the next block to be received.

(2) *490 input subchannel.* The *ready to receive* (RTR) line is propagated by two separate paths but only one was affected by the reset logic. The uncleared RTR would cause an interface control check when clock was received.

(3) *All general purpose input subchannels.* A *no operation* instruction chained to a *store subchannel status* instruction proved to be an illegal sequence not identified in the specification.

V. System Refinement

The operating system, program load, and number of user devices are subject to change but currently there is no measure of system performance to indicate if changes are improving support capabilities. A future Sustaining Engineer function will provide the needed information. All devices, multiple-control unit subchannels, and channels will be monitored to determine usage and conflict as a function of time and machine loading.

VI. Conclusion

The Sustaining Engineer Program is a valuable connection between the development engineer and the system programmer. The foremost concern of the program is implementation of the 360/75's of Mark IIIA consistent with the development design criteria of the Central Processing System (CPS). This has been accomplished to date by

testing hardware responses under critical conditions, by directly supporting software development, and by measuring system performance.

The primary emphasis has been to detect and correct anomalies which could cause interruption to the flight support activity. This effort will continue in support of equipment additions for follow on Mission Support Areas and expanded CPS capability.

Future efforts will concentrate on resolving the problems encountered by unsynchronized device switching and a thorough analysis of equipment performance characteristics. These results will be used to guide configuration and loading modifications in order to optimize system efficiency.

Reference

1. Stiver, R. A., "Mark IIIA IBM 360/75 Computer Configuration," in *The Deep Space Network*, Space Programs Summary 37-66, Vol. II, pp. 71–75. Jet Propulsion Laboratory, Pasadena, Calif., Nov. 30, 1970.