DSS Communications Equipment Subsystem Simulation Center High-Speed Data Assembly

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The 1971–1972 era required expansion of the Simulation Center High-Speed Data Assembly involving extensive modifications. An increase in the number of channels was necessary to provide simultaneous data handling configurations. New data sets were installed to double the data rate as required by the DSN–GCF High-Speed Data System.

I. Introduction

The Mark IIIA requirements for the Simulation Center High-Speed Data Assembly required expansion to three full-duplex data channels as indicated in Ref. 1, which outlines the GCF 1971–1972 requirements. The equipment has been upgraded to accommodate the 4800-bps data rate of the new 203A data set which is used at all stations as mentioned in Refs. 1 and 2 and detailed in Ref. 3. This configuration will support the *Mariner* Mars 1971 and the *Pioneer F* and *G* Projects.

II. Purpose of DCES SIMCEN HSDA

The DSS Communications Equipment Subsystem Simulation Center High-Speed Data Assembly (DCES SIMCEN HSDA) audio interface with the Space Flight Operations Facility (SFOF) is full duplex (FDX) with 4800-bps data rate, which is exactly the same as that used at any Deep Space Station (DSS). The direct current (dc) side of the HSDA is interfaced to the Simulation Center computer. This "long loop" configuration supplies simulation data via the audio interface with the SFOF. The Simulation Center also has a "short loop" dc interface with the six high-speed data channels of the SFOF (Ref. 4).

III. Functional Description

The SIMCEN high-speed data terminal consists of four major full-duplex (FDX) equipment groups as shown in the block diagram of Fig. 1. Each vertical group contains 3 independent full-duplex units which include data sets (DS), error-detection encoders/decoders (EDED), block multiplexers (BMXR), and a BMXR patch and test panel. The horizontal data flow depicts the 3 independent high-speed data channels. Between each group are patch and test jack panels to facilitate rapid electrical substitution by patch cord of any malfunctioning unit.

Figure 1 illustrates the functional block diagram of the SIMCEN HSDA. A brief operational description of this equipment follows. A detailed operational and transmission signal flow description may be found in Ref. 5 and the functional aspect of each piece of equipment is covered in Refs. 3, 4, and 6.

Received data enters the assembly via conditioned telephone lines and is fed to the Western Electric 203A Data Set in the form of a 4-level, amplitude-modulated, suppressed-carrier, vestigial-sideband signal. The data set demodulates, automatically equalizes, and converts analog 4-level (parallel) data to digital (serial) output data.

The decoder has a 1200-bit (one data block) storage register which is used as a delay line to allow a validity check of the data block prior to its output. On the receive side, the BMXR is used only as a 4-port line driver for the received data, feeding it to the data processing equipment through the BMXR patch and test panel.

Data transmission from the data processing equipment through the BMXR patch and test panel and the BMXR does not at present depend on the priority selection capability of the BMXR since only one of the four transmission ports is used at the SIMCEN giving each channel exclusive priority. Block synchronous data transmission is maintained by the automatic insertion of self-generated filler blocks on line between data source transmissions.

The BMXR patch and test panel contains three-channel capability in one unit (Ref. 6). The encoder, as described in Refs. 4 and 5, performs sync word recognition, polynomial division encoding, and error code insertion for each block of data.

The block of serial digital data (4800 bps) is fed to the transmit section of the 203A Data Set where it is converted from serial to parallel and digital to analog by means of a 4-level encoding format. This provides efficient use of available voice channel bandwidth for 4800-bps data rate at a transmission speed of 2400 baud.

IV. Human Engineering Design

Within the physical and electrical constraints of the assembly, the cabinet layout is arranged to provide segregated channel grouping of the EDED–BMXR equipment, which contains the visual status indicators. This may be seen in Fig. 2, where each channel group is outlined for identification. The design also groups all test equipment and patch panels at a convenient operating height.

V. Summary

The DCES SIMCEN HSDA was upgraded to meet the 1971 *Mariner* and *Pioneer F* and *G* Projects as follows:

(1) The data rate was doubled (2400 to 4800 bps) by changing from Western Electric Co. 205B to 203A Data Sets.

(2) Three independent data channels were installed to simultaneously carry FDX simulation data and maintain a hot backup channel.

References

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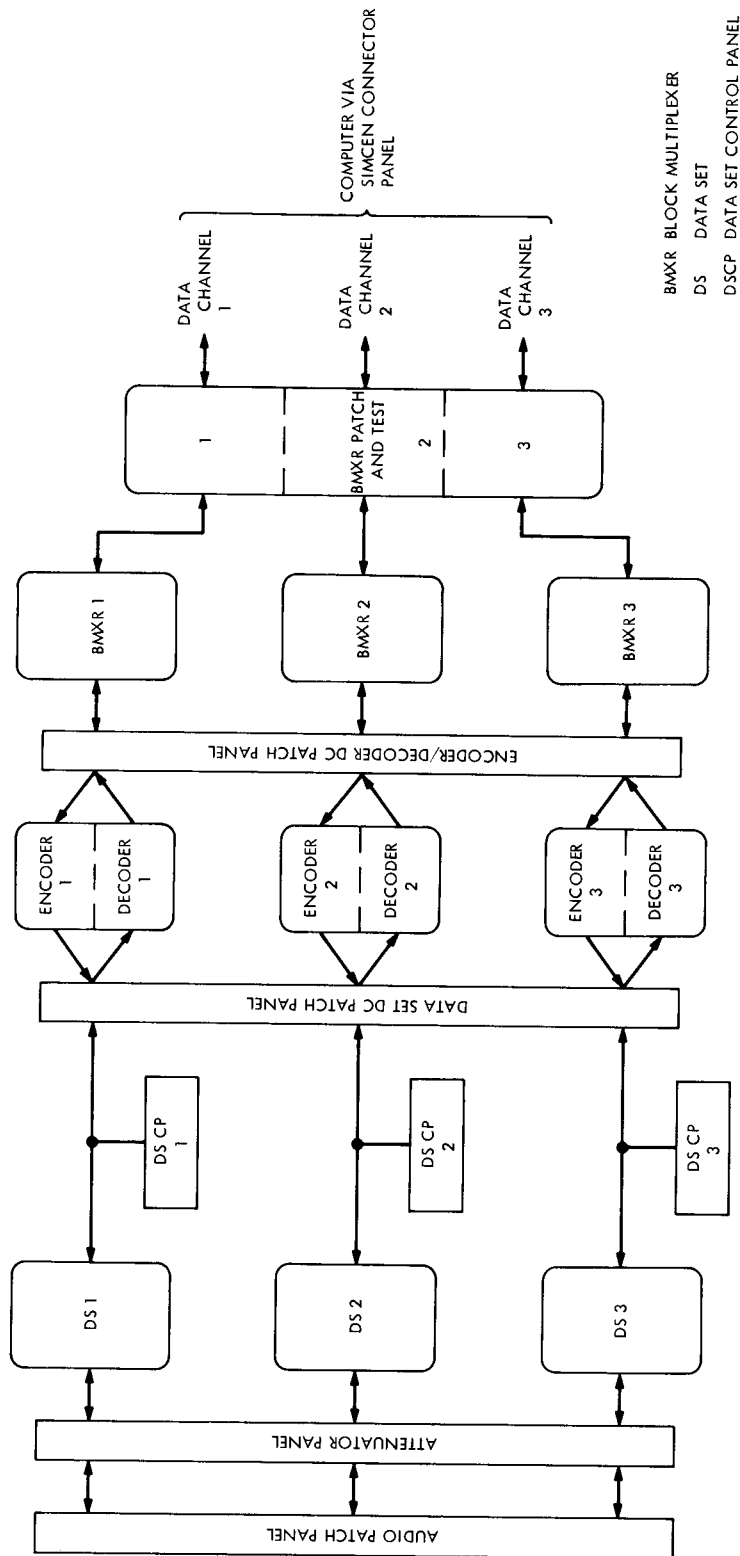
Fig. 1. DCES SIMCEN HSDA block diagram

DATA CHANNEL 1
DATA CHANNEL 2
DATA CHANNEL 3

COMPUTER VIA SIMCEN CONNECTOR PANEL

BMXR PATCH AND TEST
1   2   3

BMXR 1
BMXR 2
BMXR 3

ENCODER/DECODER DC PATCH PANEL

ENCODER 1 | DECODER 1
ENCODER 2 | DECODER 2
ENCODER 3 | DECODER 3

DATA SET DC PATCH PANEL

DS CP 1
DS CP 2
DS CP 3

DS 1
DS 2
DS 3

ATTENUATOR PANEL

AUDIO PATCH PANEL

BMXR   BLOCK MULTIPLEXER
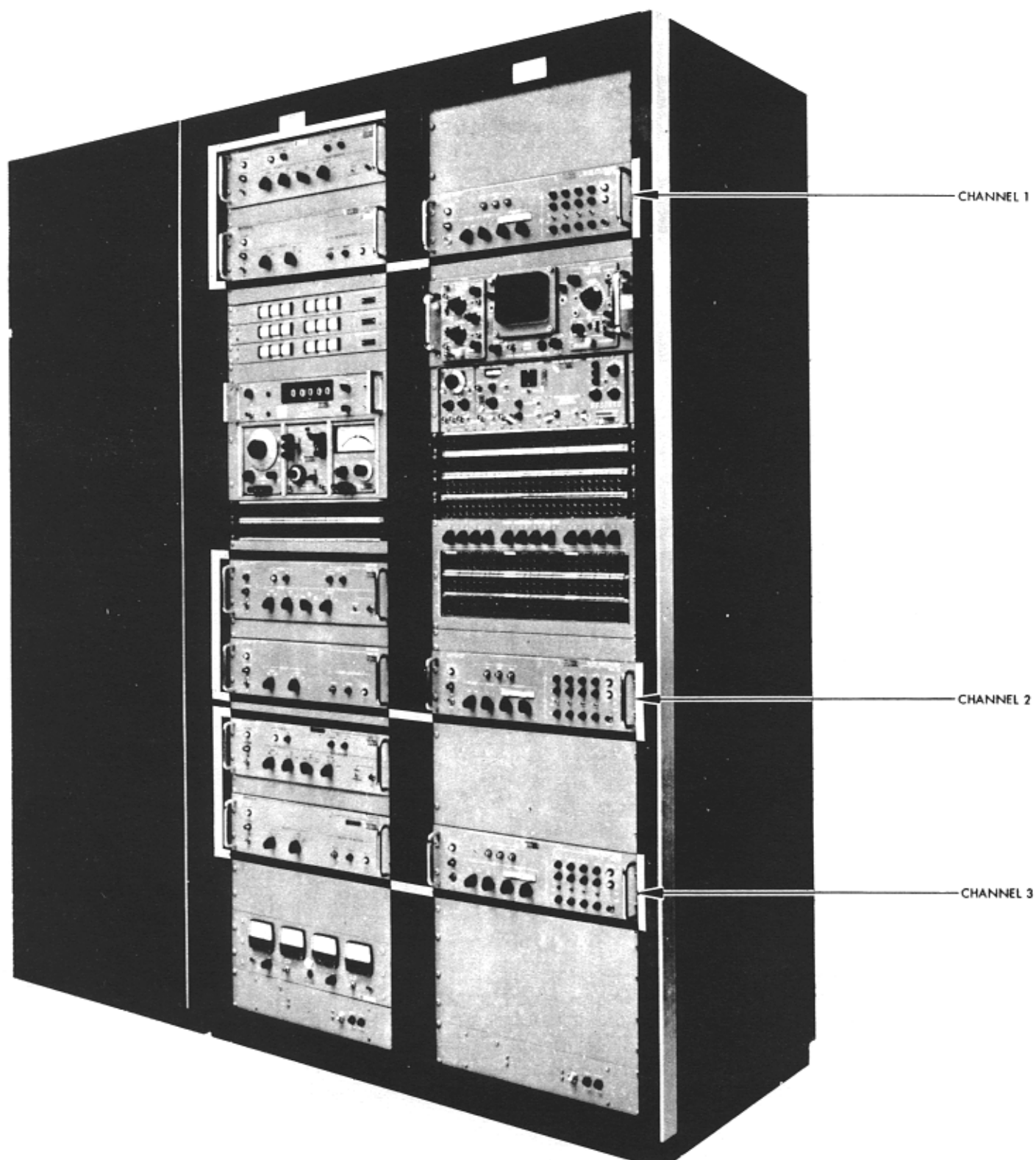DS   DATA SET
DSCP   DATA SET CONTROL PANEL

CHANNEL 1

CHANNEL 2

CHANNEL 3

Fig. 2. Simulation Center High-Speed Data Assembly